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US Patent Numbers: 4,746,877 • 4,827,223 • 4,837,523 • 4,833,424 • 4,935,704 • 4,910,477 • 5,128,564 • 4,878,034 • 4,963,802 • 5,179,355 • 5,321,371 • 5,334,883 • 5,341,047 • 5,352,987 • 5,352,389 • 5,351,012 • 5,374,898 • 5,389,840 • 5,418,495 • 5,426,396 • 5,420,542 • 5,430,670 • 5,469,104 • 5,469,106 • 5,479,133 • 5,475,343 • 5,528,303

UK Patent Numbers: 2217135 • 2217134 • 2261786
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Introduction
Mission

"To be a leading supplier of high performance analog solutions for the video/multimedia, data processing, communications and instrumentation markets."

Elantec, Inc., founded in 1983 and located in Milpitas, California, is a fully integrated semiconductor company focused on providing high performance analog intensive functions for growing markets. These markets are driven by the rapid advances in digital technology which in turn creates a demand for high speed and low power analog functions to complete the overall system. Elantec serves these markets with standard and application specific standard products (ASSP) using advanced bipolar and CMOS technologies.

Our strategy is to provide effective and timely solutions through market knowledge, advanced technologies, design expertise and close customer interface.

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<th>Market</th>
<th>Typical Applications</th>
<th>Representative Elantec Products</th>
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<td>Video/Multimedia</td>
<td>Displays, Personal Computer Add-on Boards, Set Top Converters, Special Effects Generators, Studio Equipment, Switchers/Routers, Video Distribution Networks, Workstations, Video Cameras</td>
<td>Cathode Ray Tube Drivers, Video ASSPs, Faders, DC Restoration, Video ASSPs, Faders, Amplifiers, Video ASSPs, Multipliers, PLL, Faders, Video Amplifiers, Faders, Multiplexers, Multiplexers, Power Amplifiers, High Power Amplifiers, Video Timing Circuits, CCD Drivers, Amplifiers</td>
</tr>
<tr>
<td>Instrumentation</td>
<td>Analyzers, Automatic Testers, Measuring Instruments, Medical Instrumentation, Recorders, Portable Instrumentation</td>
<td>High Speed Amplifiers, Comparators, Pin Drivers/Receivers, High Speed Amplifiers, Comparators, Mosfet Drivers, High Speed Amplifiers, Low Power Amplifiers</td>
</tr>
<tr>
<td>Data Processing</td>
<td>Copiers, Document Scanners, Magnetic Disk Drives, Optical Disk Drives, Personal Computers, Power Supplies</td>
<td>Video Amplifiers, Video Amplifiers, Servo Motor Drivers, High Speed Amplifiers, Laser Drivers, Video ASSPs, DC to DC Converters, System Managers, Mosfet Drivers</td>
</tr>
<tr>
<td>Communications</td>
<td>Fax Machines, Modems, Transmission Line Drivers, Transmission Line Receivers, Networks</td>
<td>High Speed Amplifiers, High Speed Amplifiers, Power Amplifiers, High Speed Amplifiers, Transceivers, Twisted Pair Drivers</td>
</tr>
</tbody>
</table>
Markets and Products
Elantec has over 125+ products in its catalog to serve the target markets. Many of the standard products, such as amplifiers, are used in multiple markets while the application specific products are targeted for specific applications and group of customers.

The preceding table outlines the ranges of markets, applications and products which the company serves.

Technology
The company uses a variety of technologies for its products. In particular, Elantec has focused on developing an advanced complementary bipolar technology using dielectric isolation and silicon on insulator techniques for its high speed circuits. Complementary bipolar technology allows high speed analog signals to be processed efficiently in either signal polarity which greatly simplifies design methodology and substantially improves power dissipation. Because of the dielectric isolation technique, Elantec’s complementary process has the additional inherent advantages of low capacitance, low crosstalk, no latch-up, high voltage, high temperature operation and improved speed.

For low power, analog switching and mixed signal applications, Elantec uses a variety of advanced CMOS technologies featuring dual poly and dual metal.

Advances in technology together with outstanding design expertise will continue to provide superior solutions for Elantec’s target markets.

Design Capabilities
Elantec’s engineering team has many years of experience defining, designing, manufacturing and testing analog and mixed signal devices, utilizing both Bipolar and CMOS technologies.

Functions we currently supply are: current and voltage feedback amplifiers, multipliers, video specific standard products, pin drivers and receivers, C.R.T. drivers, buffers, servo electronics, MOSFET and IGBT drivers, DC converters, instrumentation amplifiers, and precision amplifiers. Elantec also designs customer specific products where the unique technical and volume requirements of the system make this more desirable. Customers can discuss their challenging system requirements with our talented technical team of field and factory applications engineers.

Elantec provides each circuit designer and layout artist with the most up to date workstations at their desk. All stations are networked together to a server. Extra ”computing engines” are also available on the network. Elantec uses Cadence and MicroSim design software and Cadence IC layout software and design verification tools. The design tool suite can use the computing capability of the entire network to allow extensive simulations covering the variations of the wafer fabrication process, based on data derived from capability studies.
Test Automation/Equipment Capability
Elantec utilizes automatic test stations for primarily DC testing operational amplifiers, buffers, comparators, and other linear devices. In general, custom socket adaptors have been developed for unique devices such as current feedback amplifiers, DC restored video amplifiers, sync separators and disk drive servo motors. A wide range of automatic handlers allow high speed, room temperature and extended range temperature testing of Dual in Line (DIP), Small Outline (SO) packages, and special packages.

The DC test capability is augmented with AC test systems which are integrated into the main test system. The time domain systems, which are used to measure very fast rise times, slew rates and propagation delays, are comprised of programmable pulse generators and 1 GHz digitizing oscilloscopes and are capable of measurements under 10 pS. The frequency domain systems which are used to measure band-width, differential phase, differential gain, phase linearity, gain flatness, distortion, etc. are composed of programmable signal sources and network analyzers and are capable of measurements to 500 MHz.

Packaging Capability
Elantec supports most industry standard package types. Currently we are manufacturing standard products in the packages shown below:
P-DIP: 8, 14, 16, 18 Pins
SOIC: 8, 14, 16, 20, 28 Pins
SOT-23: 5 Pins

Additionally, we can supply special packages upon request for volume and special applications. Contact Elantec's marketing department for availability.

Quality and Service
Elantec's commitment to quality begins with the product definition, design and characterization and continues through the complete process. Elantec continually improves its manufacturing and quality methods using SPC, Total Quality Management and ISO 9000 compatible techniques. The company is ISO 9001 certified.

Superior product performance and quality are augmented by a commitment to customer service and technical support in order to make our customers successful. Technical customer support is provided through corporate applications, field applications engineers and technical seminars. Sales support is provided through the Elantec field sales force which directs a worldwide network of technical representatives and distributors.
Amplifiers and Buffers/Broadband/Video

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
## Comparison of Elantec Voltage Mode Feedback to Current Mode Feedback Amplifiers

Current Mode Feedback op amps have inputs similar to voltage mode op amps, but allow control of the bandwidth and offer higher slew rates and video linearity.

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<th>Characteristics</th>
<th>Voltage Mode Feedback</th>
<th>Current Mode Feedback</th>
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</thead>
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<td>Bandwidth (BW)</td>
<td>Bandwidth generally follows the Gain Bandwidth Product Rule.</td>
<td>Bandwidth not defined by gain bandwidth product rule. Bandwidth is defined by the feedback resistor value and internal compensation capacitor. Bandwidth at gain of ten is 50% to 85% of the unity gain bandwidth for a given feedback resistor, which may be reduced to give about the same bandwidth up to a gain of 10.</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>Slew Rate is defined by compensation capacitor and internal bias currents.</td>
<td>Slew rate is not limited by internal bias currents and compensation capacitor. Large Signal BW is 25% to 65% of Small Signal BW. Best with input near LSBW and output up to full output volts. Distortion usually increases rapidly for signals ≥ 35% slew rate limit.</td>
</tr>
<tr>
<td>Small Signal BW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Large Signal BW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bias Current IB +</td>
<td>Bias Current Max range is 1 μA to 20 μA on both inputs, which match and cancel.</td>
<td>+ Input current max range is 3 μA to 20 μA. - Input current max range is 7 μA to 40 μA quiescent with transient peaks to 20 mA from feedback resistor. Input currents do not match nor cancel.</td>
</tr>
<tr>
<td>- Input Current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>$R_{IN}$ differential range is 10 kΩ to 20 MΩ.</td>
<td>+ $R_{IN}$ range is 100 kΩ to 36 MΩ. $R_{IN}$ range is 100 Ω to 50 Ω and is normally the summing node for feedback currents.</td>
</tr>
<tr>
<td>Feedback Resistor</td>
<td>Feedback resistor does not define BW and may be 0 Ω for unity gain connected amp.</td>
<td>Feedback resistor defines BW and must be selected for BW even on unity gain connected amp.</td>
</tr>
<tr>
<td>Feedback Capacitor</td>
<td>May have feedback capacitors from output to $-\text{Input}$ for an integrator, if amplifier is unity-gain stable.</td>
<td>Must not have feedback capacitor from output to $-\text{Input}$. Integrator requires added resistor.</td>
</tr>
<tr>
<td>Offset Voltage $V_{OS}$</td>
<td>$V_{OS}$ Max range is 1.5 mV to 20 mV at 25°C.</td>
<td>$V_{OS}$ Max range is 3 mV to 20 mV at 25°C</td>
</tr>
<tr>
<td>Settling Time</td>
<td>Settling time to 0.1% is medium speed with similar speed for the remainder. Settling time increases with higher gain.</td>
<td>Settling to about 0.1% is fast with slow settling for the remainder from a long thermal tail for (+) gain. - Gain connections have no thermal tails.</td>
</tr>
<tr>
<td>Input Noise</td>
<td>Good for low noise low level input signals.</td>
<td>Noisy at low gains, but quiet for gains ≥ 5.</td>
</tr>
<tr>
<td>RF Amp</td>
<td>Good within 35% of slew rate limit.</td>
<td>Provides lowest distortions.</td>
</tr>
<tr>
<td>Video Amp</td>
<td>Flexible, low distortion.</td>
<td>Best for medium to high signals and for low differential gain and phase errors. Best choice for line drivers.</td>
</tr>
<tr>
<td>Output Current</td>
<td>Output Current from 50 mA to 75 mA. Use limited by Large Signal BW.</td>
<td>Output Current from 30 mA to 80 mA. May be used over wide BW range. Output current of 600 mA on power amp.</td>
</tr>
<tr>
<td>More Help</td>
<td>Tutorial #2 in 1994 Data Book</td>
<td>Application Note #3 in 1995 New Product Supplement</td>
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# Wide Bandwidth/Video Amplifiers

Current Mode Feedback Amplifiers at ±5V and ±15V Supplies.

Listed by decreasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th># of Amps</th>
<th>Bandwidth</th>
<th>Icc at ±5Vs</th>
<th>Slew Rate</th>
<th>Avol (1/gain error*)</th>
<th>Input Offset Volts</th>
<th>Input Bias Current</th>
<th>Output Current 10Ω Load</th>
<th>Supply Voltage Range</th>
<th>Package</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>-3 dB</td>
<td>all Amps</td>
<td>Av + 2</td>
<td></td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
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<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Min</td>
<td>Max</td>
<td></td>
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</table>

## Up to ±5V

**EL2070C**
- Disable
- 1 Amp: 350 MHz, 20 mA, 700 V/μs, 120 V/V, 5 mA, 20 μA, 20 μA, 50 mA, ±4.5 V, ±7 V, 8P-N-S

**EL400C**
- 1 Amp: 350 MHz, 23 mA, 700 V/μs, 120 V/V, 5.5 mA, 25 μA, 25 μA, 50 mA, ±4.5 V, ±7 V, 8P-N-S

**EL2180C**
- Wide BW
- Low Power
- 1 Amp: 250 MHz, 6 mA, 1200 V/μs, 200 V/V, 15 mA, 15 μA, 30 μA, 80 mA, 50 mA, 50 mA, ±1.5 V, ±6.3 V, 8P-N-S-W

**EL2280C**
- 2 Amps: 250 MHz, 12 mA, 24 mA, 1200 V/μs, 200 V/V, 15 mA, 15 μA, 30 μA, 80 mA, 50 mA, 50 mA, ±1.5 V, ±6.3 V, 8P-N-S

**EL2186C**
- Disable
- 4 Amps: 250 MHz, 24 mA, 24 mA, 1200 V/μs, 200 V/V, 15 mA, 15 μA, 30 μA, 80 mA, 50 mA, 50 mA, ±1.5 V, ±6.3 V, 16P-N-S

**EL2071C**
- Disable
- 4 Amps: 150 MHz, 24 mA, 24 mA, 1200 V/μs, 200 V/V, 15 mA, 15 μA, 30 μA, 80 mA, 50 mA, 50 mA, ±1.5 V, ±6.3 V, 8P-N-S

**EL2286C**
- 1 Amp: 85 MHz, 24 mA, 24 mA, 600 V/μs, 97 V/V, 10 mA, 15 μA, 40 μA, 30 mA, ±4.5 V, ±6 V, 8P-N-S

**EL2170C**
- Low Power
- 4 Amps: 70 MHz, 8 mA, 8 mA, 800 V/μs, 200 V/V, 15 mA, 5 μA, 10 μA, 80 mA, 50 mA, 50 mA, ±1.5 V, ±6.3 V, 14P-N-S

**EL2176C**
- Disable
- Low Power
- 2 Amps: 70 MHz, 8 mA, 8 mA, 800 V/μs, 200 V/V, 15 mA, 5 μA, 10 μA, 80 mA, 50 mA, 50 mA, ±1.5 V, ±6.3 V, 14P-N-S

## Up to ±15 V

**EL2160C**
- Wide BW
- 1 Amp: 180 MHz, 20 mA, 20 mA, 1500 V/μs, 890 V/V, 10 mA, 3 μA, 15 μA, 60 mA, ±2 V, ±16.5 V, 8P-N-S

**EL2260C**
- 2 Amps: 180 MHz, 30 mA, 30 mA, 1500 V/μs, 890 V/V, 10 mA, 3 μA, 15 μA, 60 mA, ±2 V, ±16.5 V, 16P-N-S

**EL2360C**
- Disable
- 4 Amps: 180 MHz, 40 mA, 40 mA, 1500 V/μs, 890 V/V, 10 mA, 3 μA, 15 μA, 60 mA, ±2 V, ±16.5 V, 14P-N-S

**EL2175C**
- Precision
- 1 Amp: 142 MHz, 10 mA, 1000 V/μs, 6000 V/V, 3 mA, 6 μA, 7 μA, 80 mA, ±4.5 V, ±16.5 V, 8P-N-S

**EL2030C**
- Low Distortion
- 1 Amp: 120 MHz, 21 mA, 21 mA, 2000 V/μs, 1000 V/V, 20 mA, 15 μA, 40 μA, 60 mA, ±4.5 V, ±18 V, 8P-N

\[
\Delta Av = +20
\]

*Derived from: \( Avol \approx R_{OL}/(R_F + (-R_{IN} \ast Av)) \), for \( R_F \) given in AC specs. \( -R_{IN} \) is 10Ω to 50Ω.
Wide Bandwidth/Video Amplifiers
Current Mode Feedback Amplifiers at \( \pm 5V \) and \( \pm 15V \) Supplies. — Contd.
Listed by decreasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th># of Amps</th>
<th>Bandwidth (-3,\text{dB})</th>
<th>( I_{\text{CC}} ) at ( \pm 5V )</th>
<th>Slew Rate ( \text{Av} + 1 )</th>
<th>( \text{AVOL} ) (1/gain error (^*))</th>
<th>Input Bias Current</th>
<th>Output Current (10\Omega) Load</th>
<th>Supply Voltage Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2166C</td>
<td>Disable 1</td>
<td>115 MHz</td>
<td>10 mA</td>
<td>1500V/(\mu)s</td>
<td>890V/V</td>
<td>10 mV</td>
<td>5 (\mu)A</td>
<td>20 (\mu)A</td>
<td>50 mA</td>
<td>(\pm 4.5V) (\pm 16.5V)</td>
</tr>
<tr>
<td>EL2120C</td>
<td>Disable 1</td>
<td>95 MHz</td>
<td>20 mA</td>
<td>750V/(\mu)s</td>
<td>260V/V</td>
<td>25 mV</td>
<td>15 (\mu)A</td>
<td>40 (\mu)A</td>
<td>50 mA</td>
<td>(\pm 2.5V) (\pm 16.5V)</td>
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<tr>
<td>EL4393C</td>
<td>Disable 3</td>
<td>90 MHz</td>
<td>27 mA</td>
<td>960V/(\mu)s</td>
<td>67V/V</td>
<td>12 mV</td>
<td>5 (\mu)A</td>
<td>65 (\mu)A</td>
<td>40 mA</td>
<td>(\pm 4.5V) (\pm 16.5V)</td>
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<tr>
<td>EL2099C</td>
<td>Power 1</td>
<td>50 MHz</td>
<td>45 mA</td>
<td>1000V/(\mu)s</td>
<td>167V/V</td>
<td>20 mV</td>
<td>15 (\mu)A</td>
<td>35 (\mu)A</td>
<td>600 mA</td>
<td>(\pm 4.5V) (\pm 16.5V)</td>
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<tr>
<td>EL2020C</td>
<td>Disable 1</td>
<td>50 MHz</td>
<td>12 mA</td>
<td>500V/(\mu)s</td>
<td>365V/V</td>
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<td>40 (\mu)A</td>
<td>30 mA</td>
<td>(\pm 4.5V) (\pm 16.5V)</td>
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<td>Precision 1</td>
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<td>500V/(\mu)s</td>
<td>14000V/V</td>
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<td>6 (\mu)A</td>
<td>7 (\mu)A</td>
<td>55 mA</td>
<td>(\pm 4.5V) (\pm 16.5V)</td>
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\( \Delta \text{Av} = +20 \)

\(^*\)Derived from: \( \text{AVOL} \approx \frac{R_{OL}}{(R_F + (-R_{IN} \cdot \text{Av}))} \), for \( R_F \) given in AC specs. \(-R_{IN} \) is 10\(\Omega\) to 50\(\Omega\).
Wide Bandwidth/Video Amplifiers
Voltage Mode Feedback Amplifiers at ±5V and ±15V Supplies.
Listed by decreasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th># of Amps</th>
<th>Bandwidth at Min Gain</th>
<th>$I_{CC\text{ at } \pm5V}$</th>
<th>Min Stable Gain</th>
<th>Slew Rate at Min Gain</th>
<th>$A_{VOL}$</th>
<th>Input Offset $V_{OS}$</th>
<th>Input Bias $I_{B}$</th>
<th>Output Current 100 Load</th>
<th>Supply Voltage Range</th>
<th>Package</th>
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<tr>
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<td></td>
<td></td>
<td>P</td>
</tr>
<tr>
<td>Up to ±5V</td>
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<td></td>
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<td>EL2075C</td>
<td>Wide BW</td>
<td>1</td>
<td>400 MHz</td>
<td>23 mA</td>
<td>+10 $A_{V}$</td>
<td>800V/$\mu$s</td>
<td>500V/V</td>
<td>1 $mV$</td>
<td>6 $\mu$A</td>
<td>50 mA</td>
<td>±3V</td>
<td>±16.5V</td>
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<td>23 mA</td>
<td>+2 $A_{V}$</td>
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<td>500V/V</td>
<td>1.5 $mV$</td>
<td>6 $\mu$A</td>
<td>50 mA</td>
<td>±3V</td>
<td>±6V</td>
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<td>1</td>
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<td>23 mA</td>
<td>+1 $A_{V}$</td>
<td>250V/$\mu$s</td>
<td>500V/V</td>
<td>1.5 $mV$</td>
<td>6 $\mu$A</td>
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<td>±3V</td>
<td>±7V</td>
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<td>Single Supply</td>
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<td>+1 $A_{V}$</td>
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<td>177V/V</td>
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<td>±12.5V</td>
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<td>EL2450C</td>
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<td>14P-N-S</td>
</tr>
<tr>
<td>EL2157C</td>
<td>+ Disable, Clamp</td>
<td>1</td>
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<td>6.5 mA</td>
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<td>8P-N-S-W</td>
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<tr>
<td>EL2257C</td>
<td>+ Disable, Clamp</td>
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<td>13 mA</td>
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<td>14P-N-S</td>
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<tr>
<td>EL2357C</td>
<td>+ Disable, Clamp</td>
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<td>16P-N-S</td>
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<tr>
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<td>Low Cost Single Supply</td>
<td>2</td>
<td>100 MHz</td>
<td>17 mA</td>
<td>+2 $A_{V}$</td>
<td>140V/$\mu$s</td>
<td>160V/V</td>
<td>20 $mV$</td>
<td>15 $\mu$A</td>
<td>75 mA</td>
<td>±10V</td>
<td>±9V</td>
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<tr>
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<td>25.5 mA</td>
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<td>Up to ±15V</td>
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</tr>
<tr>
<td>EL2045C</td>
<td>Low Cost</td>
<td>1</td>
<td>100 MHz</td>
<td>6.3 mA</td>
<td>+2 $A_{V}$</td>
<td>275V/$\mu$s</td>
<td>1500V/V</td>
<td>7 $mV$</td>
<td>8.2 $\mu$A</td>
<td>50 mA</td>
<td>±2.5V</td>
<td>±18V</td>
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<tr>
<td>EL2245C</td>
<td>$V_{IN}$ to 0.1V at +5Vs</td>
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<td>12.6 mA</td>
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<td>8P-N-S-W</td>
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<tr>
<td>EL2445C</td>
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<td>4</td>
<td></td>
<td>25.2</td>
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<td>+1 $A_{V}$</td>
<td>325V/$\mu$s</td>
<td>750V/V</td>
<td>7 $mV$</td>
<td>8.2 $\mu$A</td>
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<td>±2.5V</td>
<td>±18V</td>
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<td>$V_{IN}$ to 0.1V at +5Vs</td>
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<td>EL2444C</td>
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Output Disable Wide Bandwidth/Video Amplifiers
Current Mode Feedback and Voltage Mode Feedback with Clamp at ±5V and ±15V Supplies.
Listed by decreasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th># of Amps</th>
<th>Bandwidth -3 dB</th>
<th>Turn On Time</th>
<th>Turn Off Time</th>
<th>ICC at ±5V all Amps</th>
<th>ICC at ±5Vs Disable</th>
<th>Slew Rate Av + 2</th>
<th>VOS</th>
<th>Feedthrough Cap.*</th>
<th>IOUT into 0Ω Load</th>
<th>Supply Voltage Range</th>
<th>Package</th>
</tr>
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<tbody>
<tr>
<td></td>
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<tr>
<td>Up to ±5V</td>
<td>Current Mode Feedback</td>
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<td>EL2186C</td>
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<td>40 ns</td>
<td>500 ns</td>
<td>6 mA</td>
<td>20 μA</td>
<td>1200V/μs</td>
<td>15 mV</td>
<td>0.48 pF</td>
<td>80 mA</td>
<td>±1.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL2286C</td>
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<td>50 mA</td>
<td>±6.3V</td>
<td>14P-N-S</td>
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<td>1000 ns</td>
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<td>700V/μs</td>
<td>5 mV</td>
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<td>50 mA</td>
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<td>70 ns</td>
<td>21 mA</td>
<td>3 mA</td>
<td>1200V/μs</td>
<td>Δ 6 mV</td>
<td>0.14 pF</td>
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<td>500 ns</td>
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<td>20 μA</td>
<td>800V/μs</td>
<td>15 mV</td>
<td>0.48 pF</td>
<td>80 mA</td>
<td>±1.5V</td>
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<td>50 mA</td>
<td>±6.3V</td>
<td>14P-N-S</td>
</tr>
<tr>
<td>Up to ±15V</td>
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<td>EL2166C</td>
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<td>115 MHz</td>
<td>70 ns</td>
<td>70 ns</td>
<td>10 mA</td>
<td>10 mA</td>
<td>1500V/μs</td>
<td>10 mV</td>
<td>1.5 pF</td>
<td>50 mA</td>
<td>±4.5V</td>
<td>8P-N-S</td>
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<td>50 ns</td>
<td>20 mA</td>
<td>50 mA</td>
<td>750V/μs</td>
<td>25 mV</td>
<td>0.2 pF</td>
<td>50 mA</td>
<td>±2.5V</td>
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<td>30 ns</td>
<td>27 mA</td>
<td>16 mA</td>
<td>960V/μs</td>
<td>12 mV</td>
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<td>±4.5V</td>
<td>16P-N-M</td>
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<td>500V/μs</td>
<td>10 mV</td>
<td></td>
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<td>30 mA</td>
<td>±4.5V</td>
<td>±18V</td>
<td>8P-N-M</td>
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<tr>
<td>Single Supply</td>
<td>Voltage Mode Feedback</td>
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<tr>
<td>EL2157C</td>
<td>+ VOUT Clamp</td>
<td>1</td>
<td>125 MHz</td>
<td>40 ns</td>
<td>40 ns</td>
<td>6.5 mA</td>
<td>20 μA</td>
<td>275V/μs</td>
<td>1.5 mV</td>
<td>75 mA</td>
<td>+3V</td>
<td>±16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL2257C</td>
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<td>2</td>
<td>25 ns</td>
<td>50 ns</td>
<td>13 mA</td>
<td>100 μA</td>
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<td>EL2357C</td>
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<td>50 ns</td>
<td>19.5 mA</td>
<td>150 μA</td>
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</table>

*Feedthrough capacitance is the equivalent capacitance from the signal input to the output of a disabled amplifier.

Δ Av = +10
### Video Buffers

Wide Bandwidth/Video/Distribution

Listed by decreasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Bandwidth -3 dB</th>
<th>Output Current (Peak)</th>
<th># of Loads * 2 Vpp</th>
<th>I_{CC} at V_{S}</th>
<th>Slew Rate</th>
<th>Input Offset Volts</th>
<th>Input Bias Current</th>
<th>Supply Voltage Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
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<td>Typ</td>
<td>Min</td>
<td>150Ω Loads</td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
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<td>EL2072C</td>
<td>Closed Loop</td>
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<td>50 mA</td>
<td>4</td>
<td>20 mA</td>
<td>800V/μs</td>
<td>8 mV</td>
<td>50 μA</td>
<td>± 4.5V</td>
<td>± 7V</td>
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<tr>
<td>EL2002AC</td>
<td>Low Power Low Cost</td>
<td>180 MHz</td>
<td>100 mA</td>
<td>6</td>
<td>7.5 mA</td>
<td>2000V/μs</td>
<td>15 mV</td>
<td>10 μA</td>
<td>± 4.5V</td>
<td>± 18V</td>
</tr>
<tr>
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<td>Video</td>
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<td>105 mA</td>
<td>6</td>
<td>15 mA</td>
<td>1200V/μs</td>
<td>40 mV</td>
<td>25 μA</td>
<td>± 4.5V</td>
<td>± 18V</td>
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<td>EL2009C</td>
<td>Power</td>
<td>90 MHz</td>
<td>1.4A</td>
<td>15</td>
<td>65 mA</td>
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<td>60 mV</td>
<td>125 μA</td>
<td>± 4.5V</td>
<td>± 18V</td>
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<tr>
<td>EL2001AC</td>
<td>Low Power Low Cost</td>
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<td>100 mA</td>
<td>2</td>
<td>2 mA</td>
<td>2000V/μs</td>
<td>10 mV</td>
<td>3 μA</td>
<td>± 4.5V</td>
<td>± 18V</td>
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<tr>
<td>EL2008C</td>
<td>Low Power Low Cost</td>
<td>55 MHz</td>
<td>1.4A</td>
<td>15</td>
<td>22 mA</td>
<td>2500V/μs</td>
<td>40 mV</td>
<td>35 μA</td>
<td>± 4.5V</td>
<td>± 18V</td>
</tr>
</tbody>
</table>

*1 Vpp out on 75Ω Double Matched Loaded Line.

### Power Distribution Amplifiers

Wide Bandwidth/Video/Distribution

Listed by decreasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Bandwidth -3 dB</th>
<th>Output Current (Peak)</th>
<th># of Loads * 15 Vpp</th>
<th>I_{CC} at ±15 V_{S}</th>
<th>Slew Rate</th>
<th>Input Offset Volts</th>
<th>Input Bias Current</th>
<th>Supply Voltage Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typ</td>
<td>Min</td>
<td>150Ω Loads</td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2009C</td>
<td>Buffer</td>
<td>90 MHz</td>
<td>1.4A</td>
<td>15</td>
<td>65 mA</td>
<td>3000V/μs</td>
<td>60 mV</td>
<td>125 μA</td>
<td>± 4.5V</td>
<td>± 18V</td>
</tr>
<tr>
<td>EL2008C</td>
<td>Buffer</td>
<td>55 MHz</td>
<td>1.4A</td>
<td>15</td>
<td>22 mA</td>
<td>2500V/μs</td>
<td>40 mV</td>
<td>35 μA</td>
<td>± 4.5V</td>
<td>± 18V</td>
</tr>
<tr>
<td>EL2099C</td>
<td>Gain Amp</td>
<td>50 MHz</td>
<td>600 mA</td>
<td>6</td>
<td>45 mA</td>
<td>1000V/μs</td>
<td>20 mV</td>
<td>15 μA</td>
<td>± 4.5V</td>
<td>± 16.5V</td>
</tr>
<tr>
<td><strong>EL1501C</strong></td>
<td>Dual Driver/Receiver</td>
<td>63 MHz</td>
<td>2 mA x 75 mA</td>
<td>8</td>
<td>45 mA</td>
<td>1000V/μs</td>
<td>30 mV</td>
<td>10 μA</td>
<td>± 4.5V</td>
<td>± 16.5V</td>
</tr>
</tbody>
</table>

*1 Vpp out on 75Ω Double Matched Loaded Line.

**For datasheet see Communications Section of Databook.
### Instrumentation Wide Bandwidth/Video Amplifiers
Listed by increasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Input Offset</th>
<th>Input Bias</th>
<th>Diff. Input</th>
<th>Common Mode Range</th>
<th>Bandwidth -3 dB at Min Gain</th>
<th>Min Stable Gain</th>
<th>Slew Rate at Min Gain</th>
<th>Diff. Gain*</th>
<th>Diff. Phase*</th>
<th>$I_{OUT}$ 10Ω Load</th>
<th>$I_{CC}$ at ±15Vs</th>
<th>Supply Voltage Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Volt</td>
<td>µA</td>
<td>Volt</td>
<td>V/µs Typ</td>
<td>V/µs Typ</td>
<td>% Typ</td>
<td>% Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Min Max</td>
<td>P = Pins</td>
</tr>
<tr>
<td>Up to ±15V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N = PDIP</td>
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<tr>
<td>EL4431C</td>
<td>8</td>
<td>20</td>
<td>2</td>
<td>12</td>
<td>80</td>
<td>+2</td>
<td>380</td>
<td>0.02</td>
<td>0.02</td>
<td>40</td>
<td>16</td>
<td>±4.5 ±16</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL4430C</td>
<td>8</td>
<td>20</td>
<td>2</td>
<td>12</td>
<td>80</td>
<td>+1</td>
<td>380</td>
<td>0.04</td>
<td>0.08</td>
<td>40</td>
<td>16</td>
<td>±4.5 ±16</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>Up to ±5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±5Vs</td>
<td></td>
</tr>
<tr>
<td>EL2142C</td>
<td>−25 + 40</td>
<td>20</td>
<td>2</td>
<td>2</td>
<td>150</td>
<td>+1</td>
<td>400</td>
<td>0.2</td>
<td>0.2</td>
<td>50</td>
<td>14</td>
<td>±3 ±6</td>
<td>8P-N-N</td>
</tr>
</tbody>
</table>

*$R_L = 500\Omega$ for EL4431C, 150Ω for EL4430C, and 100Ω for EL2142C.

### Multiplexing Video/Wide Bandwidth Amplifiers
Voltage Feedback Amplifiers listed by decreasing bandwidth.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Mux Ratio and Gain</th>
<th>Input</th>
<th>Input</th>
<th>Bandwidth -3 dB at Min Gain</th>
<th>Slew Rate</th>
<th>Diff. Gain</th>
<th>Diff. Phase</th>
<th>Mux Delay Time</th>
<th>$I_{OUT}$ 10Ω Load</th>
<th>$I_{CC}$ at V$_S$</th>
<th>Supply Voltage Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Mux Ratio and Gain</td>
<td>Volts</td>
<td>Volts</td>
<td></td>
<td>MHz Typ</td>
<td>V/µs Typ</td>
<td>% Typ</td>
<td>% Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Min Max</td>
<td>P = Pins</td>
</tr>
<tr>
<td>Up to ±5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N = PDIP</td>
</tr>
<tr>
<td>EL4332C</td>
<td>Triple</td>
<td>2:1</td>
<td>2*</td>
<td>0.01</td>
<td>202</td>
<td>300</td>
<td>650</td>
<td>0.04</td>
<td>0.08</td>
<td>3</td>
<td>30**</td>
<td>60 ±5</td>
<td>16P-S</td>
</tr>
<tr>
<td>EL4331C</td>
<td>Triple</td>
<td>2:1</td>
<td>1*</td>
<td>0.01</td>
<td>202</td>
<td>300</td>
<td>425</td>
<td>0.04</td>
<td>0.08</td>
<td>3</td>
<td>30**</td>
<td>60 ±5</td>
<td>16P-S</td>
</tr>
<tr>
<td>Up to ±15V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL4421C</td>
<td>Com -IN</td>
<td>2:1</td>
<td>+1</td>
<td>0.01</td>
<td>202</td>
<td>500</td>
<td>80</td>
<td>0.01</td>
<td>0.01</td>
<td>8</td>
<td>40</td>
<td>14 ±3 ±15</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL4441C</td>
<td>Com -IN</td>
<td>4:1</td>
<td>+1</td>
<td>0.01</td>
<td>202</td>
<td>500</td>
<td>80</td>
<td>0.01</td>
<td>0.01</td>
<td>12</td>
<td>40</td>
<td>16 ±3 ±15</td>
<td>14P-N-S</td>
</tr>
<tr>
<td>EL443C</td>
<td>Diff Input</td>
<td>4:1</td>
<td>+1</td>
<td>0.01</td>
<td>202</td>
<td>500</td>
<td>80</td>
<td>0.01</td>
<td>0.01</td>
<td>12</td>
<td>40</td>
<td>16 ±3 ±15</td>
<td>14P-N-S</td>
</tr>
<tr>
<td>EL442C</td>
<td>Com -IN</td>
<td>4:1</td>
<td>+2</td>
<td>0.01</td>
<td>400</td>
<td>750</td>
<td>65</td>
<td>0.02</td>
<td>0.02</td>
<td>8</td>
<td>40</td>
<td>14 ±3 ±15</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL444C</td>
<td>Diff Input</td>
<td>4:1</td>
<td>+2</td>
<td>0.01</td>
<td>400</td>
<td>750</td>
<td>65</td>
<td>0.02</td>
<td>0.02</td>
<td>12</td>
<td>40</td>
<td>16 ±3 ±15</td>
<td>14P-N-S</td>
</tr>
</tbody>
</table>

*Internally Fixed Gain ** 75Ω Load
Features
- 1.3 mA supply current
- 70 MHz bandwidth
- 2000 V/µs slew rate
- Low bias current, 1 µA typical
- 100 mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5V to ±15V
- No thermal runaway

Applications
- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

General Description
The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a −3 dB bandwidth of 70 MHz, and delivers 100 mA, yet draws only 1.3 mA of supply current. It typically operates from ±15V power supplies but will work with as little as ±5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op amp.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: Elantec's Processing, Monolithic Integrated Circuits.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2001ACN</td>
<td>0°C to +75°C</td>
<td>P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2001CM</td>
<td>0°C to +75°C</td>
<td>20-Lead SOL</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2001CN</td>
<td>0°C to +75°C</td>
<td>P-DIP</td>
<td>MDP0031</td>
</tr>
</tbody>
</table>

Connection Diagrams

**EL2001 DIP Pinout**

**EL2001 SOL Pinout**

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>V&lt;sub&gt;S&lt;/sub&gt; Supply Voltage (V+ - V-)</th>
<th>±18V or 36V</th>
<th>T&lt;sub&gt;A&lt;/sub&gt; Operating Temperature Range</th>
<th>EL2001AC/EL2001C</th>
<th>0°C to +75°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Input Voltage (Note 1)</td>
<td>±15V or V&lt;sub&gt;S&lt;/sub&gt;</td>
<td>50 mA</td>
<td>T&lt;sub&gt;J&lt;/sub&gt; Operating Junction Temperature</td>
<td>EL2001AC/EL2001C</td>
<td>150°C</td>
</tr>
<tr>
<td>I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Current (Note 1)</td>
<td>±50 mA</td>
<td>50 mA</td>
<td>T&lt;sub&gt;ST&lt;/sub&gt; Storage Temperature</td>
<td>EL2001AC/EL2001C</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>PD</td>
<td>Power Dissipation (Note 2)</td>
<td>See Curves</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Duration</td>
<td>Output Short Circuit</td>
<td>Continuous</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LT/77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore T<sub>J</sub> = T<sub>C</sub> = T<sub>A</sub>.

### Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>EL2001AC</th>
<th>EL2001C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Load</td>
<td>Temp</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Test Level</td>
</tr>
<tr>
<td>V&lt;sub&gt;O&lt;/sub&gt;S</td>
<td>Offset Voltage</td>
<td>EL2001A/EL2001AC</td>
<td>EL2001/EL2001C</td>
<td>0</td>
<td>∞</td>
<td>25°C</td>
</tr>
<tr>
<td>I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Current</td>
<td>EL2001A/EL2001AC</td>
<td>EL2001/EL2001C</td>
<td>0</td>
<td>∞</td>
<td>25°C</td>
</tr>
<tr>
<td>R&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Resistance</td>
<td>±12V</td>
<td>100Ω</td>
<td>25°</td>
<td>1</td>
<td>8</td>
</tr>
</tbody>
</table>

---

2-10
## Electrical Characteristics

$V_S = \pm 15V, R_S = 50\Omega$, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>EL2001AC</th>
<th>EL2001C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$V_{in}$ Load</td>
<td>Temp</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>$A_{V1}$</td>
<td>Voltage Gain</td>
<td>$\pm 12V \infty$</td>
<td>25°C</td>
<td>0.990</td>
<td>0.998</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>0.985</td>
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<td></td>
</tr>
<tr>
<td>$A_{V2}$</td>
<td>Voltage Gain</td>
<td>$\pm 10V 100\Omega$</td>
<td>25°C</td>
<td>0.83</td>
<td>0.93</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>0.80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{V3}$</td>
<td>Voltage Gain with $V_S = \pm 5V$</td>
<td>$\pm 3V 100\Omega$</td>
<td>25°C</td>
<td>0.82</td>
<td>0.89</td>
<td></td>
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<td>$T_{MIN}, T_{MAX}$</td>
<td>0.79</td>
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</tr>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing</td>
<td>$\pm 12V 100\Omega$</td>
<td>25°C</td>
<td>$\pm 10\pm 11$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>$\pm 9.5$</td>
<td></td>
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</tr>
<tr>
<td>$R_{OUT}$</td>
<td>Output Resistance</td>
<td>$\pm 2V 100\Omega$</td>
<td>25°C</td>
<td>10</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td></td>
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<td>$T_{MIN}, T_{MAX}$</td>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>$\pm 12V$ (Note 4)</td>
<td>25°C</td>
<td>$\pm 100\pm 160$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>$\pm 95$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$0 \infty$</td>
<td>25°C</td>
<td>1.3</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>2.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Supply Rejection,  (Note 5)</td>
<td>$0 \infty$</td>
<td>25°C</td>
<td>60</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise Time</td>
<td>$0.5V 100\Omega$</td>
<td>25°C</td>
<td>4.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_d$</td>
<td>Propagation Delay</td>
<td>$0.5V 100\Omega$</td>
<td>25°C</td>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate, (Note 6)</td>
<td>$\pm 10V 100\Omega$</td>
<td>25°C</td>
<td>1200</td>
<td>2000</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds $\pm 7.5V$ then the input current must be limited to $\pm 50$ mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to $+12V$ and the output to $+10V$ and measure the output current. Repeat with $-12V_{IN}$ and $-10V$ on the output.

Note 5: $V_{OS}$ is measured at $V_S^+ = +4.5V$, $V_S^- = -4.5V$ and at $V_S^+ = +18V$, $V_S^- = -18V$. Both supplies are changed simultaneously.

Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$. 
Typical Performance Curves

Offset Voltage vs Temperature

Voltage Gain vs Temperature

Output Voltage Swing vs Temperature

Supply Current vs Supply Voltage

Voltage Gain vs Input Voltage

Voltage Gain vs Source Resistance

Input Bias Current vs Input Voltage

± Slew Rate vs Supply Voltage

± Slew Rate vs Capacitive Load
Typical Performance Curves — Contd.

Voltage Gain vs Frequency for Various Resistive Loads

Voltage Gain vs Frequency for Various Capacitive Loads; \( R_L = 100\Omega \)

Voltage Gain vs Frequency for Various Capacitive Loads; \( R_L = \infty \)

Phase Shift vs Frequency for Various Capacitive Loads

-3 dB Bandwidth vs Supply Voltage

Power Supply Rejection Ratio vs Frequency

Output Impedance vs Frequency

Reverse Isolation vs Frequency

Small Signal Output Resistance vs Output Current

- EL2001C
- Low Power, 70 MHz Buffer Amplifier

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Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

20-Lead SOL
Maximum Power Dissipation vs Ambient Temperature

Short Circuit Current vs Temperature

Large Signal Response

Small Signal Response
**Application Information**

The EL2001 is a monolithic buffer amplifier built on Elantec’s proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001’s topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

**Power Supplies**

The EL2001 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

**Input Characteristics**

The input to the EL2001 looks like a resistance in parallel with about 3.5 picofarads in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 50 mΩ. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above ±7.5V differential input to output, additional series resistance should be added.

**Source Impedance**

The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resistive sources up to 1 Meg present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_S > 100 kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.
EL2001C Macromodel

*Connections: + input
  * + Vsupply
  * - Vsupply
  * output
  *
.subckt M2001 2 1 4 7

* Input Stage
el 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 9pF
rc 11 12 100
cc 12 0 4pF
e2 13 0 12 0 1.0

* Output stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 0.9mA
i2 15 4 0.9mA

* Bias Current
iin+ 2 0 1uA

* Models
.model qn npn(is = 5e-15 bf = 150 rb = 200 ptf = 45 tf = 0.1nS)
.model qp pnp(is = 5e-15 bf = 150 rb = 200 ptf = 45 tf = 0.1nS)
.ends
EL2001C Macromodel — Contd.
**EL2002C**  
**Low Power, 180 MHz Buffer Amplifier**

### Features
- 180 MHz bandwidth
- 2000 V/µs slew rate
- Low bias current, 3 µA typical
- 100 mA output current
- 5 mA supply current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5V to ±15V
- No thermal runaway

### Applications
- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Isolation buffer

### Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2002ACN</td>
<td>0°C to +75°C</td>
<td>P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2002CM</td>
<td>0°C to +75°C</td>
<td>20-Lead SOL</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2002CN</td>
<td>0°C to +75°C</td>
<td>P-DIP</td>
<td>MDP0031</td>
</tr>
</tbody>
</table>

### General Description

The EL2002 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a −3 dB bandwidth of 180 MHz, and delivers 100 mA, yet draws only 5 mA of supply current. It typically operates from ±15V power supplies but will work with as little as ±5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. Typical examples include fast op-amp output current boosters, coaxial cable drivers and A/D converter input buffers.

Elantec’s products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see the Elantec document, QRA-1: Elantec’s Processing, Monolithic Integrated Circuits.

### Connection Diagrams

**EL2002 DIP Pinout**

![DIP Pinout](2002-1)

**EL2002 SOL Pinout**

![SOL Pinout](2002-2)

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Supply Voltage (V⁺⁻ - V⁻)</th>
<th>±18V or 36V</th>
<th>TA</th>
<th>Operating Temperature Range:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vₛ</td>
<td>Supply Voltage</td>
<td></td>
<td>±18V or 36V</td>
<td></td>
<td>EL2002AC/EL2002C 0°C to +75°C</td>
</tr>
<tr>
<td>Vᵢᵣ</td>
<td>Input Voltage (Note 1)</td>
<td></td>
<td>±15V or Vₛ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Iᵢᵣ</td>
<td>Input Current (Note 1)</td>
<td></td>
<td>±50 mA</td>
<td></td>
<td>Tᵣ Operating Junction Temperature 150°C</td>
</tr>
<tr>
<td>Pᵣ</td>
<td>Power Dissipation (Note 2)</td>
<td></td>
<td>See Curves</td>
<td></td>
<td>Tₛ Storage Temperature −65°C to +150°C</td>
</tr>
</tbody>
</table>

Output Short Circuit

Duration (Note 3) Continuous

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Tᵣ=Tₛ=Tₐ.

Test Level

| Test Procedure | The Test Procedures
<table>
<thead>
<tr>
<th></th>
<th></th>
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<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at Tₐ = 25°C and QA sample tested at Tₐ = 25°C.</td>
</tr>
<tr>
<td>III</td>
<td>Tₘₐₓ and Tₘᵢₙ per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td></td>
<td>Parameter is typical value at Tₐ = 25°C for information purposes only.</td>
</tr>
</tbody>
</table>

Electrical Characteristics Vₛ = ±15V, Rₛ = 50Ω, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>EL2002AC</th>
<th>EL2002C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vₒₛ</td>
<td>Offset Voltage</td>
<td>Vᵢᵣ, Load</td>
<td>Temp</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>EL2002A/EL2002AC</td>
<td>0</td>
<td>∞</td>
<td>25°C</td>
<td>-15</td>
<td>5</td>
<td>+15</td>
</tr>
<tr>
<td>EL2002/EL2002C</td>
<td>0</td>
<td>∞</td>
<td>25°C</td>
<td>-40</td>
<td>10</td>
<td>+40</td>
</tr>
<tr>
<td>Iᵢᵣ</td>
<td>Input Current</td>
<td>Vᵢᵣ, Load</td>
<td>Temp</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>EL2002A/EL2002AC</td>
<td>0</td>
<td>∞</td>
<td>25°C</td>
<td>-10</td>
<td>3</td>
<td>+10</td>
</tr>
<tr>
<td>EL2002/EL2002C</td>
<td>0</td>
<td>∞</td>
<td>25°C</td>
<td>-15</td>
<td>5</td>
<td>+15</td>
</tr>
<tr>
<td>Rᵢᵣ</td>
<td>Input Resistance</td>
<td>Vᵢᵣ, Load</td>
<td>Temp</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>+12V</td>
<td>100Ω</td>
<td>25°C</td>
<td>1</td>
<td>3</td>
<td>I</td>
<td>MΩ</td>
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<tr>
<td>Aᵥ₁</td>
<td>Voltage Gain</td>
<td>Vᵢᵣ, Load</td>
<td>Temp</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>±12V</td>
<td>∞</td>
<td>25°C</td>
<td>0.990</td>
<td>0.998</td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td>Aᵥ₂</td>
<td>Voltage Gain</td>
<td>Vᵢᵣ, Load</td>
<td>Temp</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>±10V</td>
<td>100Ω</td>
<td>25°C</td>
<td>0.85</td>
<td>0.93</td>
<td>I</td>
<td>V/V</td>
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</table>
### Electrical Characteristics \( V_S = \pm 15V, R_S = 50\Omega \), unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>EL2002AC</th>
<th>EL2002C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_{V3} )</td>
<td>Voltage Gain with ( V_S = \pm 5V )</td>
<td>( V_{IN} ) ( \pm 3V ) 100( \Omega )</td>
<td>25( ^\circ )C</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing</td>
<td>( V_{IN} ) ( \pm 12V ) 100( \Omega )</td>
<td>25( ^\circ )C</td>
<td>( T_{MIN} ) ( T_{MAX} ) 0.80</td>
<td>0.91</td>
<td>III</td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>Output Resistance</td>
<td>( V_{IN} ) ( \pm 2V ) 100( \Omega )</td>
<td>25( ^\circ )C</td>
<td>8</td>
<td>13</td>
<td>I</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output Current</td>
<td>( V_{IN} ) ( \pm 12V ) ( \text{(Note 4)} )</td>
<td>25( ^\circ )C</td>
<td>( T_{MIN} ) ( T_{MAX} ) 15</td>
<td>+100</td>
<td>+160</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>0</td>
<td>( \infty )</td>
<td>25( ^\circ )C</td>
<td>5</td>
<td>7.5</td>
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<tr>
<td>( PSRR )</td>
<td>Supply Rejection, ( \text{(Note 5)} )</td>
<td>0</td>
<td>( \infty )</td>
<td>25( ^\circ )C</td>
<td>( T_{MIN} ) ( T_{MAX} ) 10</td>
<td>60</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Rise Time</td>
<td>0.5V</td>
<td>100( \Omega )</td>
<td>25( ^\circ )C</td>
<td>5</td>
<td>7.5</td>
</tr>
<tr>
<td>( t_d )</td>
<td>Propagation Delay</td>
<td>0.5V</td>
<td>100( \Omega )</td>
<td>25( ^\circ )C</td>
<td>5</td>
<td>7.5</td>
</tr>
<tr>
<td>( SR )</td>
<td>Slew Rate, ( \text{(Note 6)} )</td>
<td>( V_{OUT} ) ( \pm 10V )</td>
<td>100( \Omega )</td>
<td>25( ^\circ )C</td>
<td>1200</td>
<td>2000</td>
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</tbody>
</table>

**Note 1:** If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds \( \pm 7.5V \) then the input current must be limited to \( \pm 50 \) mA. See the applications section for more information.

**Note 2:** The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

**Note 3:** A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

**Note 4:** Force the input to \(+12V\) and the output to \(+10V\) and measure the output current. Repeat with \(-12V_{IN}\) and \(-10V\) on the output.

**Note 5:** \( V_{OS} \) is measured at \( V_S^+ = +4.5V, V_S^- = -4.5V \) and \( V_S^+ = +18V, V_S^- = 18V \). Both supplies are changed simultaneously.

**Note 6:** Slew rate is measured between \( V_{OUT} = \pm 5V \) and \(-5V\).
Typical Performance Curves

Offset Voltage vs Temperature

Voltage Gain vs Temperature

Output Voltage Swing vs Temperature

Supply Current vs Supply Voltage

Voltage Gain vs Input Voltage

Voltage Gain vs Source Resistance

Input Bias Current vs Input Voltage at Various Temperatures

Input Bias Current vs Input Voltage

± Slew Rate vs Supply Voltage
Typical Performance Curves — Contd.

- Slew Rate vs Load Capacitance
- Voltage Gain vs Frequency for Various Resistive Loads
- Voltage Gain vs Frequency for Various Capacitive Loads; $R_L = 100\Omega$
- Voltage Gain vs Frequency for Various Capacitive Loads; $R_L = \infty$
- Phase Shift vs Frequency for Various Capacitive Loads
- $-3\,\text{dB}$ Bandwidth vs Supply Voltage
- Power Supply Rejection Ratio vs Frequency
- Output Impedance vs Frequency
- Reverse Isolation vs Frequency
Typical Performance Curves — Contd.

Small Signal Output Resistance vs Output Current

- $R_{\text{on}} = 50 \Omega$
- $V_{\text{GS}} = 15V$
- $V_{\text{IN}} = 0V$
- $T_A = 25^\circ C$

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

- $T_{J\text{MAX}} = 150^\circ C$
- $\theta_{JC} = 50^\circ C/W$
- $\theta_{JA} = 55^\circ C/W$

20-Lead SOL Maximum Power Dissipation vs Ambient Temperature

- $T_{J\text{MAX}} = 150^\circ C$
- $\theta_{JA} = 95^\circ C/W$

Short Circuit Current vs Temperature

-$V_{\text{GS}} = 15V$

Large Signal Response

- INPUT $-0V$
- OUTPUT $R_L = 100\Omega$
- $C_L = 10\ pF$
- $f = 20\ MHz$

Small Signal Response

- INPUT $-0V$
- OUTPUT $R_L = \infty$
- $C_L = 220\ pF$
- $f = 5\ MHz$
Burn-In Circuit

\ [+V = +10V \hfill +5Hz \hfill \pm \hfill 5V \hfill -V = -10V \hfill -10V \hfill \]

Simplified Schematic

Application Information
The EL2002 is a monolithic buffer amplifier built on Elantec's proprietary Complementary Bipolar process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2002 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2002's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/\mu s slew rates with 100\Omega loads possible with very low supply current.

Power Supplies
The EL2002 may be operated with single or split supplies with total voltage difference between 10V (\pm 5V) and 36V (\pm 18V). It is not necessary to use equal split value supplies. For example -5V and +12V would be excellent for signals from -2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 \mu F tantalum capacitor with short leads should be used for both supplies.

Input Characteristics
The input to the EL2002 looks like a resistance in parallel with about 3.5 pF in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (\(R_{IN}\)) is affected by the output load, beta and the internal boost. \(R_{IN}\) can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about \(\pm 2.5V\) input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 200\Omega. There is also 100\Omega in series with the input that limits input current. Above \(\pm 7.5V\) differential input to output, additional series resistance should be added.

Source Impedance
The EL2002 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resistive sources up to 1 MHz present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (\(R_S > 100\ \text{k}\Omega\)), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.
EL2002 Macromodel

* Connections: + input
  * + Vsupply
  * - Vsupply
  * output

.subckt M2002 2 1 4 7

* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 2pF
rc 11 12 100
cc 12 0 3pF
e2 13 0 12 0 1.0

* Output Stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 2mA
i2 15 4 2mA

* Bias Current
iin+ 2 0 3uA

* Models
.model qn npn(is = 5e-15 bf = 150 rb = 200 ptf = 45 tf = 0.1nS)
.model qp pnp(is = 5e-15 bf = 150 rb = 200 ptf = 45 tf = 0.1nS)
.ends
EL2002 Macromodel — Contd.
**Features**
- Differential gain 0.1%
- Differential phase 0.1°
- 100 mA continuous output current guaranteed
- Short circuit protected
- Wide bandwidth—100 MHz
- High slew rate—1200 V/μs
- High input impedance—2 MΩ
- Low quiescent current drain
- EL2003—Pin compatible with LH0002CN, LH0002H, HA2-5002
- EL2033—Pin compatible with HA3-5002, HA7-5002, HA3-5033, HA7-5033

**Applications**
- Co-ax cable driver
- Flash converter driver
- Video DAC buffer
- Op amp booster

**General Description**
The EL2003/EL2033 are general purpose monolithic unity gain buffers featuring 100 MHz, -3 dB bandwidth and 4 ns small signal rise time. These buffers are capable of delivering a ±100 mA current to a resistive load and are oscillation free into capacitive loads. In addition, the EL2003/EL2033 have internal output short circuit current limiting which will protect the devices under both a DC fault condition and AC operation with reactive loads. The extremely fast slew rate of 1200 V/μs, wide bandwidth, and high output drive make the EL2003/EL2033 ideal choices for closed loop buffer applications with wide band op amps. These same characteristics and excellent DC performance make the EL2003/EL2033 excellent choices for open loop applications such as driving coaxial and twisted pair cables.

The EL2003/EL2033 are constructed using Elantec’s proprietary dielectric isolation process that produces PNP and NPN transistors with essentially identical AC and DC characteristics.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec’s processing, request our brochure: QRA-1: Elantec’s Processing—Monolithic Products.

**Connection Diagrams**
# EL2003C/EL2033C
100 MHz Video Line Driver

## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level 2003C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_S$</td>
<td>Supply Voltage ($V_+ - V_-)$</td>
<td>±18V or 36V</td>
<td>$T_A$ Operating Temperature Range</td>
<td>0°C to +75°C</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage (Note 1)</td>
<td>±15V or $V_S$</td>
<td>$T_A$ Operating Junction Temperature</td>
<td>EL2003C/2033C</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Current (Note 1)</td>
<td>±50 mA</td>
<td>$T_J$ Operating Junction Temperature</td>
<td>175°C</td>
<td></td>
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<tr>
<td>$P_D$</td>
<td>Power Dissipation (Note 2)</td>
<td>See Curves</td>
<td>Metal Can</td>
<td>150°C</td>
<td></td>
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<tr>
<td></td>
<td>Output Short Circuit</td>
<td>Continuous</td>
<td>Plastic</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Duration (Note 3)</td>
<td></td>
<td>$T_{ST}$ Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
</tbody>
</table>

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J=T_C=T_A$.

### Test Levels and Procedures

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at $T_A=25°C$ and QA sample tested at $T_A=25°C$, $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at $T_A=25°C$ for information purposes only.</td>
</tr>
</tbody>
</table>

## Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level 2003C</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Output Offset Voltage</td>
<td>$V_{IN}$ Load</td>
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<td>Min</td>
<td>Typ</td>
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<td></td>
<td></td>
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<td>$T_{MIN}$, $T_{MAX}$</td>
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<td>5</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Current</td>
<td>$V_{IN}$ Load</td>
<td>$25°C$, $T_{MAX}$</td>
<td>-25</td>
<td>-5</td>
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<td></td>
<td>$T_{MIN}$</td>
<td>-50</td>
<td>50</td>
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<tr>
<td>$R_{IN}$</td>
<td>Input Resistance</td>
<td>±12V Load 100$\Omega$</td>
<td>$25°C$, $T_{MAX}$</td>
<td>0.5</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>$T_{MIN}$</td>
<td>0.05</td>
<td>2</td>
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<tr>
<td>$A_{V1}$</td>
<td>Voltage Gain</td>
<td>±12V Load 1 k$\Omega$</td>
<td>$25°C$</td>
<td>0.98</td>
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<td>0.97</td>
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<td>$A_{V2}$</td>
<td>Voltage Gain</td>
<td>±6V Load 50$\Omega$</td>
<td>$25°C$</td>
<td>0.83</td>
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<td>$T_{MIN}$, $T_{MAX}$</td>
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<td>$A_{V3}$</td>
<td>Voltage Gain with $V_S = \pm 5V$</td>
<td>±3V Load 50$\Omega$</td>
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### Electrical Characteristics

$$V_S = \pm 15V, \quad R_S = 50\Omega$$ — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
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<tr>
<td></td>
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<td>$$V_{IN}$$</td>
<td>Load</td>
<td>Temp</td>
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<td>$$R_{OUT}$$</td>
<td>Output Resistance</td>
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<td>50Ω</td>
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<td>$$I_{OUT}$$</td>
<td>Output Current</td>
<td>±12V</td>
<td>(Note 4)</td>
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<td>$$I_S$$</td>
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<td>Supply Rejection, (Note 5)</td>
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<td>SR1</td>
<td>Slew Rate, (Note 6)</td>
<td>±10V</td>
<td>1 kΩ</td>
<td>25°C</td>
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<tr>
<td>SR2</td>
<td>Slew Rate, (Note 7)</td>
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<td>THD</td>
<td>Distortion @ 1 kHz</td>
<td>4 $$V_{rms}$$</td>
<td>50Ω</td>
<td>25°C</td>
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</table>

**Note 1:** If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

**Note 2:** The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

**Note 3:** A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

**Note 4:** Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V in and −10V on the output.

**Note 5:** $$V_S = \pm 4.5V$$ to ±18V.

**Note 6:** Slew rate is measured between $$V_{OUT} = +5V$$ and −5V.

**Note 7:** Slew rate is measured between $$V_{OUT} = +2.5V$$ and −2.5V.
Typical Performance Curves

### Quiescent Supply Current vs Supply Voltage
- **SUPPLY VOLTAGE (V)**
- **SUPPLY CURRENT (mA)**
- **TJ = -55°C**
- **TJ = 25°C**
- **TJ = 125°C**
- **VIN = 0V**

### Input Current vs Supply Voltage
- **INPUT CURRENT (mA)**
- **TJ = 125°C**
- **TJ = 25°C**
- **TJ = -55°C**

### Input Resistance vs Temperature
- **JUNCTION TEMPERATURE (°C)**
- **INPUT RESISTANCE (kΩ)**

### Voltage Gain vs Frequency
- **FREQUENCY (MHz)**
- **VOLTAGE GAIN (dB)**
- **VS = ±15V**
- **RL = 50Ω**
- **RL = 10Ω**
- **RL > 1kΩ**
- **CL = 100pF**
- **CL = 50pF**
- **CL = 0.01μF**

### Voltage Gain vs Frequency with No Resistive Load
- **VOLTAGE GAIN (dB)**
- **CL = 0.01μF**

### Voltage Gain vs Frequency with Various Capacitive Loads
- **CL = 100pF**
- **CL = 500pF**
- **CL = 1000pF**
- **CL = 10nF**

### Phase Shift vs Frequency
- **PHASE SHIFT (DEGREES)**
- **FREQUENCY (MHz)**
- **VGS = ±15V**
- **RL = 50Ω**
- **RL = 10Ω**
- **RL > 1kΩ**
- **TJ = 25°C**
- **TJ = -55°C**
- **TJ = 125°C**

### 3 dB Bandwidth vs Supply Voltage
- **FREQUENCY (MHz)**
- **SUPPLY VOLTAGE (±V)**
- **VIN = ±12V**
- **RL = 100Ω**
- **TJ = -55°C**
- **TJ = 25°C**
- **TJ = 125°C**

**Typical Performance Curves for EL2003C/EL2033C 100 MHz Video Line Driver**
Typical Performance Curves — Contd.

Maximum Undistorted Output Voltage vs Frequency

- Voltage (V)
- Frequency (Hz)

Power Supply Rejection Ratio vs Frequency

- Voltage (V)
- Frequency (Hz)

 Rise Time vs Temperature

- Voltage (V)
- Frequency (Hz)

Slew Rate vs Supply Voltage

- Frequency (Hz)

Slew Rate vs Temperature

- Frequency (Hz)

Slew Rate vs Capacitive Load

- Frequency (Hz)

Output Resistance vs Supply Voltage

- Frequency (Hz)

Small Signal Output Resistance vs DC Output Current

- Frequency (Hz)

Output Impedance vs Frequency

- Frequency (Hz)
Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

- $T_J$ MAX = 150°C
- $R_{JC} = 50°C/W
- $R_{JA} = 95°C/W

- INFINITE HEAT SINK
- FREE AIR NO HEAT SINK

20-Lead SOL
Maximum Power Dissipation vs Ambient Temperature

- $T_J$ MAX = 150°C
- $R_{JA} = 95°C/W

- FREE AIR NO HEAT SINK

Current Limit vs Temperature

- $V_G = \pm 15V$
- $V_O = 0V$
- $V_{IN} > 2V$

- JUNCTION TEMPERATURE (°C)

2003-8
Applications Hints
The EL2003/EL2033 are monolithic buffer amplifiers built with Elantec's proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The circuits are connection of symmetrical common collector transistors that provide both sink and source current capability independent of output voltage while maintaining constant output and input impedances. The high slew rate and wide bandwidth of the EL2003 and EL2033 make them useful beyond video frequencies.

Power Supplies
The EL2003/EL2033 may be operated with single or split supplies as low as ±2.5V (5V total) to as high as ±18V (36V total). However, the bandwidth, slew rate and output impedance degrade significantly for supply voltages less than ±5V (10V total) as shown in the characteristic curves. It is not necessary to use equal value split supplies, for example −5V and +12V would be excellent for 0V to 1V video signals.

Bypass capacitors from each supply pin to a ground plane are recommended. The EL2003/EL2033 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate a supply ringing and the interference it can cause, a 10 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rates and longer settling times.

The EL2003 metal can package has the collectors of the output transistors brought out separately from the input supplies for pin compatibility with the ELH0002H. If the collectors operate on lower supplies than the input stage, the internal power dissipation can be reduced. However, the output transistors can be driven into hard saturation when the input voltage exceeds the collector supply voltage. The recovery time to come out of saturation will be 2 μs or 3 μs and the output may oscillate during this recovery period.

Input Range
The input to the EL2003/EL2033 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit. However, there are clamp diodes from the input to the output that protect the transistor base emitter junctions. These diodes start to conduct at about ±9.5V input to output differential voltage. Of course the input resistance drops dramatically when the diodes start conducting; the diodes are rated at ±50 mA.

The input characteristics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However, if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance
The EL2003/EL2033 have excellent input-output isolation and are very tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources can cause oscillations; a 1 kΩ resistor in series with the buffer input lead will usually eliminate problems without sacrificing too much speed. An unterminated cable or other resonant source can also cause oscillations. Again, an isolating resistor will eliminate the problem.

Current Limit
The EL2003/EL2033 have internal current limits that protect the output transistors. The current limit goes down with junction temperature rise as shown in the characteristic curves. At a junction temperature of +175°C the current limits are at about 100 mA. If the EL2003 or EL2033 output is shorted to ground when operating on ±15V supplies, the power dissipation will be greater than 1.5W. A heat sink is required in order for the EL2003 or EL2033 to survive an indefinite short. Recovery time to come out of current limit is about 250 ns.
Heat Sinking

When operating the EL2003/EL2033 in elevated ambient temperatures and/or high supply voltages and low impedance loads, the internal power dissipation can force the junction temperature above the maximum rating (175°C for the metal can package and 150°C for the plastic DIP). Also, an indefinite short of the output to ground will cause excessive power dissipation.

The thermal resistance junction to case is 55°C per Watt for the metal can package and 50°C/W for the plastic DIP. A suitable heat sink will increase the power dissipation capability significantly beyond that of the package alone. Several companies make standard heat sinks for both packages. Aavid and Thermalloy heat sinks have been used successfully.

Parallel Operation

If more than 100 mA output is required or if heat management is a problem, several EL2003s or EL2033s may be paralleled together. The result is as though each device was driving only part of the load. For example, if two units are paralleled then a 50Ω load looks like 100Ω to each EL2003. Parallel operation results in lower input and output impedances, increased bias current but no increase in offset voltage. An example showing three EL2003s in parallel and also the addition of a FET input buffer stage is shown below. By using a dual FET the circuit complexity is minimal and the performance is excellent. Take care to minimize the stray capacitance at the input of the EL2003s for maximum slew rate and bandwidth.

FET Input Buffer with High Output Currents

Resistive Loads

The DC gain of the EL2003/EL2033 is the product of the unloaded gain (0.995) and the voltage divider formed by the device output resistance and the load resistance.

\[ A_V = \frac{0.995 \cdot R_L}{R_L + R_{OUT}} \]

The high frequency response of the EL2003/EL2033 varies with the value of the load resistance as shown in the characteristic curves. If the 100 MHz peaking is undesirable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from the output to ground. The snubber circuit works by presenting a high frequency load resistance of less than 50Ω while having no loading effect at low frequencies.

Small Signal Response

Large Signal Response

![Small Signal Response](image1)

![Large Signal Response](image2)
Applications Hints — Contd.

Capacitive Loads
The EL2003/EL2033 are stable driving any type of capacitive load. However, when driving a pure capacitance of less than a thousand picofarads the frequency response has excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and will ring for several hundred ns.

If the peaking and ringing cause system problems they can be eliminated with an RC snubber circuit from the output to ground. The values can be found empirically by observing a squarewave or the frequency response. First just put the resistor alone from output to ground until the desired response is obtained. Of course the gain will be reduced due to $R_{OUT}$. Then put capacitance in series with the resistor to restore the gain at low frequencies. Start with a small capacitor and increase until the response is optimum. Too large a capacitor will roll the gain off prematurely and result in a longer settling time. The figure below shows an example of an EL2003 driving a 330 pF load, which is similar to the input of a flash converter.

Inductive Loads
The EL2003/EL2033 can drive small motors, solenoids, LDT's and other inductive loads. Fold-back current limiting is NOT used in the EL2003 or EL2033 and current limiting into an inductive load does NOT in and of itself cause spikes or kickbacks. However, if the EL2003 or EL2033 is in current limit and the input voltage is changing quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltage. Motors are also able to generate kickbacks when the EL2003 or EL2033 is in current limit.

To prevent damage to the EL2003/EL2033 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Reverse Isolation
The EL2003/EL2033 have excellent output to input isolation over a wide frequency range. This characteristic is very important when the buffer is used to drive signals between different equipment over cables. Often the cable is not perfect or the termination is improper and reflections occur that act like a signal source at the output of the buffer. Worst case the cable is connected to a source instead of where it is supposed to go. In both situations the buffer must keep these signals from its input. The following curve shows the reverse isolation of the EL2003/EL2033 versus frequency for various source resistors.
Applications Hints — Contd.

Driving Cables
There are at least three ways to use the EL2003 and EL2033 to drive cables, as shown in the adjacent figure. The most obvious is to directly connect the cable to the output of the buffer. This results in a gain determined by the output resistance of the EL2003 or EL2033 and the characteristic impedance of the cable, assuming it is properly terminated. For RG-58 into 50Ω, the gain is about −1 dB, exclusive of cable losses. For optimum response and minimum reflections it is important for the cable to be properly terminated.

Double termination of a cable is the cleanest way to drive it since reflections are absorbed on both ends of the cable. The cable source resistor is equal to the characteristic impedance of the cable less the output resistance of the EL2003/EL2033. The gain is −6 dB exclusive of the cable attenuation.

Back matching is the last and most interesting way to drive a cable. The cable source resistor is again the characteristic impedance less the output resistance of the EL2003/EL2033; the termination resistance is now much greater than the cable impedance. The gain is 0 dB and DC levels waste no power.

An additional EL2033 or EL2033 make a good receiver at the terminating end. Because an un terminated cable looks like a resonant circuit, the receiving EL2003 or EL2033 should have an isolating resistor in series with its input to prevent oscillations when the cable is not connected to the driver. Of course if the cable is always connected to the back match, no resistor is necessary.

WARNING: ONE END OF A CABLE MUST BE PROPERLY TERMINATED. If neither end is terminated in the cable characteristic impedance, the cable will have standing waves that appear as resonances in the frequency response. The resonant frequencies are a function of the cable length and even relatively short cables can cause problems at frequencies as low as 1 MHz. Longer cables should be terminated on both ends.

Op Amp Booster
The EL2003 or EL2033 can boost the output drive of almost any monolithic op amp. Because the phase shift in the EL2003/EL2033 is low at the op amp's unity gain frequency, no additional compensation is required. By following an op amp with an EL2003 or EL2033, the buffered op amp can drive cables and other low impedance loads directly. Even decompensated high speed op amps can take advantage of the EL2003's or EL2033's 100 mA drive.
Applications Hints — Contd.

Driving capacitive loads with any closed loop amplifier creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The output impedance of the EL2003 or EL2033 is less than 10Ω from DC to about 10 MHz, but a capacitive load of 1000 pF will generate about 45 degrees phase shift at 10 MHz and make high speed op amps unstable. Obviously more capacitance will cause the same problem but at lower frequencies, and slower op amps as well would become unstable.

The easiest way to drive capacitive loads is to isolate them from the feedback with a series resistor. Ten to twenty ohms is usually enough but the final value depends on the op amp used and the range of load capacitance.

Op Amp Booster with Capacitive Load

If the system requirements will not tolerate the isolation resistor, then additional high frequency feedback from the op amp output (the buffer input) and an isolating resistor from the buffer output is required. This requires that the op amp be unity gain stable.

Complex Feedback with the Buffer to Drive Capacitive Loads

This works with any unity gain stable OA. Snubber Circuit (51Ω 470 pF) is optional.
Typical Applications — Contd.

Turbo Amplifier, BW = 30 MHz for Gains from 1 to 5

Video Distribution Amplifier
In this broadcast quality circuit, the EL2006 FET input amplifier provides a very high input impedance so that it may be used with a wide variety of signal sources including video DACs, CCD cameras, video switches or 75Ω cables. The EL2006 provides a voltage gain of 2.5 while the potentiometer allows the overall gain to be adjusted to drive the standard signal levels into the back matched 75Ω cables. Back matching prevents multiple reflections in the event that the remote end of the cable is not properly terminated. The 1k pull up resistors reduce the differential gain error from 0.15% to less than 0.1%.
Burn-In Circuits

**EL2003 Metal Can**

![EL2003 Metal Can Schematic](image)

**EL2003 DIP**

![EL2003 DIP Schematic](image)

Simplified Schematic

![Simplified Schematic](image)
EL2003/EL2033C
100 MHz Video Line Driver

EL2003 Macromodel

* Connections: + input
  •
  •
  •
  •
  •
  .subckt M2003 2 1 4 7

* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 10pF
rc 11 12 100
cc 12 0 3pF
e2 13 0 12 0 1.0

* Output Stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 5
r3 19 7 5
c1 14 0 3pF
c2 1 15 0 3pF
i1 1 14 3mA
i2 15 4 3mA

* Models
.model qn npn(is = 5e-15 bf = 150 rb = 350 ptf = 45 cjc = 2pF tf = 0.3nS)
.model qp pnp(is = 5e-15 bf = 150 rb = 350 ptf = 45 cjc = 2pF tf = 0.3nS)
.ends
EL2003 Macromodel — Contd.
EL2008C
55 MHz 1 Amp Buffer Amplifier

Features
- High slew rate—2500 V/μs
- Wide bandwidth—
  100 MHz @ $R_L = 50\Omega$
  55 MHz @ $R_L = 10\Omega$
- Output current—1A continuous
- Output impedance—1Ω
- Quiescent current—13 mA
- Short circuit protected
- Power package with isolated metal tab

Applications
- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information
<table>
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<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline #</th>
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<tbody>
<tr>
<td>EL2008CT</td>
<td>0°C to +75°C</td>
<td>TO-220</td>
<td>MDP0028</td>
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</tbody>
</table>

General Description
The EL2008 is a patented high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing only 13 mA of quiescent supply current. The EL2008's 1500 V/μs slew rate and 55 MHz bandwidth driving a 10Ω load is second only to the EL2009 and insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2008.

Used as an open loop buffer, the EL2008's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load. The EL2008 has output short circuit current limiting which will protect the device under both a DC fault condition and AC operation with reactive loads.

The EL2008 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2008, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages, therefore the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2008CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic

Absolute Maximum Ratings (25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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</thead>
<tbody>
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<td>Vgs</td>
<td>Supply Voltage (V + − V −)</td>
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<td>−40</td>
<td>10</td>
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<td>Vds</td>
<td>Operating Temperature Range</td>
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<td>If</td>
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<td>±15 or Vgs</td>
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<td>65°C</td>
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<td>Is</td>
<td>Current (Note 1)</td>
<td>±50 mA</td>
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<td>−5</td>
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<td>Pd</td>
<td>Power Dissipation (Note 2)</td>
<td>See Curves</td>
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Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Tst = Tc = Tja.

Electrical Characteristics $V_{s} = \pm 15V$, $R_s = 50\Omega$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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<td>10Ω</td>
<td>25°C</td>
<td>0.88</td>
</tr>
<tr>
<td>Avo</td>
<td>Voltage Gain, $V_s = \pm 15V$</td>
<td>±3V</td>
<td>10Ω</td>
<td>25°C</td>
<td>0.87</td>
</tr>
<tr>
<td>V01</td>
<td>Output Voltage Swing</td>
<td>±14V</td>
<td>100Ω</td>
<td>25°C</td>
<td>±13</td>
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<td>V02</td>
<td>Output Voltage Swing</td>
<td>±12V</td>
<td>10Ω</td>
<td>25°C</td>
<td>±10.5</td>
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<tr>
<td>Ro1</td>
<td>Output Impedance</td>
<td>±10V</td>
<td>±10 mA</td>
<td>25°C</td>
<td>1.8</td>
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<tr>
<td>Ro2</td>
<td>Output Impedance</td>
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<td>±1A</td>
<td>25°C</td>
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<td>Io</td>
<td>Output Current</td>
<td>±12V</td>
<td>(Note 3)</td>
<td>25°C</td>
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<tr>
<td>Is</td>
<td>Supply Current</td>
<td>0</td>
<td>25°C</td>
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<tr>
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<td>Supply Rejection (Note 4)</td>
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<td>25°C</td>
<td>60</td>
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<td>Vs+ , Vs−</td>
<td>Supply Sensitivity (Note 5)</td>
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<td>25°C</td>
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### Electrical Characteristics

**V_s = ±15V, R_s = 50Ω**, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>V_IN</td>
<td>Load</td>
<td>Temp</td>
<td>Min</td>
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<tr>
<td>SR1</td>
<td>Slew Rate</td>
<td>±10V</td>
<td>50Ω</td>
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<td>10Ω</td>
<td>25°C</td>
<td>1500</td>
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<td>SR2</td>
<td>Slew Rate</td>
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<td>25°C</td>
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<td>tr, tf</td>
<td>Rise/Fall Time</td>
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<td>10Ω</td>
<td>25°C</td>
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<td>BW</td>
<td>-3 dB Bandwidth</td>
<td>100 mV</td>
<td>10Ω</td>
<td>25°C</td>
<td>55</td>
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<td>C_IN</td>
<td>Input Capacitance</td>
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<tr>
<td>TD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>25°C</td>
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</tbody>
</table>

**Note 1:** If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for information.

**Note 2:** The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

**Note 3:** Force the input to +12V and the output to +10V and measure the output current. Repeat with -12V and -10V on the output.

**Note 4:** V_S = ±4.5V then V_S is changed to ±18V.

**Note 5:** V_S+ = +15V, V_S- = -4.5V then V_S- is changed to -18V and V_S+ = +4.5V then V_S+ is changed to +18V.

**Note 6:** Slew Rate is measured between V_OUT = +5V and -5V.

**Note 7:** Slew Rate is measured between V_OUT = +2.5V and -2.5V.
Typical Performance Curves

- **Slew Rate vs Capacitance Load**
- **Slew Rate vs Supply Voltage**
- **Rise Time vs Temperature**
- **Output Impedance vs Frequency**
- **Output Resistance vs Supply Voltage**
- **Small Signal Output Resistance vs DC Output Current**
- **input Current vs Input Voltage**
- **-3 dB Bandwidth vs Supply Voltage**
- **Quiescent Supply Current vs Supply Voltage**
- **Supply Current (mA) vs Supply Voltage**
- **Input Current (µA) vs Input Voltage**
Typical Performance Curves — Contd.

Voltage Gain vs Frequency at Various Resistive Loads

Voltage Gain vs Frequency at Various Capacitive Loads

Phase Shift vs Frequency at Various Resistive Loads

Reverse Isolation vs Frequency

Power Supply Rejection Ratio vs Frequency

Active operating area.
Applications Information
The EL2008 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2008 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2008's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 3000 V/μs slew rates with 10Ω load possible with modest supply current.

Power Supplies
The EL2008 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). However, bandwidth, slew rate and output impedance are affected by total supply voltages below 20V (±10V) as shown by the characteristic curves. It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum a 10 μF tantalum capacitor in parallel with a 0.1 μF capacitor with short leads should be used for both supplies.

Input Characteristics
The input to the EL2008 looks like a resistance in parallel with about 25 pF in addition to a DC bias current. The DC bias current is due to the mismatch in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (RIN) is affected by the output load, beta and the internal boost. RIN can actually appear negative over portions of the input range in some units. A few typical input current (IIN) curves are shown in the characteristic curves.

Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. If the output of the EL2008 is accidentally shorted it is possible that some devices driving the EL2008's input could be damaged or destroyed driving the EL2008's load through the diodes while the EL2008 is unaffected. In such cases a resistor in series with the input of the EL2008 can limit the current.
Applications Information — Contd.

Source Impedance
The EL2008 has good input to output isolation. Open loop, capacitive and resistive sources up to 100 kΩ present no oscillation problem driving resistive loads as long as care is used in board layout to minimize output to input coupling and the supplies are properly bypassed. When driving capacitive loads in the 100 pF to 1000 pF region source resistances above 250 Ω can cause peaking and oscillation. Such problems can be eliminated by placing a capacitor from the EL2008’s input to ground. The value should be about ¼ the load capacitance. In a feedback loop there is a speed penalty and a possibility of oscillation when the EL2008 is driven with a source impedance of 2000 Ω or more. Significant phase shift can occur due to the EL2008’s 25 pF input capacitance. Inductive sources can cause oscillations. A series resistor of a few hundred ohms to 1 kΩ will usually solve the problem.

Current Limit
The EL2008 has internal current limiting to protect the output transistors. The current limit is about 1.5 A at room temperature and decreases with junction temperature. At 150°C junction temperature it is above 1 A.

Heat Sinking
A suitable heat sink will be required for most applications. The thermal resistance junction to case for the TO-220 package is 4°C per watt. No voltage appears at the heat sink tab so no precautions need to be taken to avoid shorting the tab to a supply voltage or ground. As there is a small parasitic capacitance between the tab and the buffer circuitry, it is recommended that the tab be connected to AC ground (either supply voltage or DC ground). The center lead is internally connected to the tab so the connection can be made at the tab or the center lead.

Parallel Operation
If more than 1 A is required or if heat management is a problem, several EL2008s may be paralleled together. The result is as through each device was driving only part of the load. For example, if two units are paralleled then a 5 Ω load looks like 10 Ω to each EL2008. Of course, parallel operation reduces both the input and output impedance and increases bias current. But there is no increase in offset voltage. Three units in parallel can drive a 3 Ω load ±10 V at 2500 V/µs. The output impedance will be about 0.33 Ω.

Resistive Loads
The DC gain of the EL2008 is the product of the unloaded gain (0.999) and the voltage divider formed by the device output resistance and the load resistance.

\[ A_v = 0.999 \times \left( \frac{R_L}{R_L + R_{OUT}} \right) \]

The high frequency response varies with the load resistance as shown by the characteristic curves. Both gain and phase are shown. If the 80 MHz peaking is undesirable when driving load resistors greater than 50 Ω, an RC snubber circuit can be used from output to ground. The capacitive load section discusses snubber usage in more detail.

Capacitive Loads
The EL2008 is not stable driving purely capacitive loads between 100 pF and 500 pF. Purely capacitive loads from 500 pF to 1000 pF will also have excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and ring for hundreds of nanoseconds.

When driving capacitive loads, stability can be achieved and peaking and ringing can be mini-
Applications Information — Contd.
mixed either by adding a 50Ω (or less) load in parallel with the capacitive load or by an RC snubber circuit from output to ground. The snubber values can be found empirically by observing a squarewave or the frequency response. First just put a resistor alone from the output to ground until the desired response is achieved. The gain will be reduced due to the output resistance of the EL2008 and power consumption will be high. Then put a capacitor in series with the resistor to restore gain at low frequencies and eliminate the DC current. Start with a small capacitor and increase until the response is optimum. The figure below shows an example of an EL2008 driving a 100 pF load.

Driving a pure capacitive load. Top trace is without a snubber. Bottom trace is with a snubber circuit.

Inductive Loads
The EL2008 with its 1A output current can drive small motors and other inductive loads. The EL2008’s current limiting into inductive loads does NOT in and of itself cause spikes and kickbacks. However, if the EL2008 is in current limit and the input voltage is changing very quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltages. Motors are also able to generate kickback voltages when the EL2008 is in current limit.

To prevent damage to the EL2008 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Op Amp Booster
The EL2008 can boost the output drive of almost any monolithic op amp. If the phase shift in the EL2008 is low at the op amp’s unity gain frequency, no additional frequency compensation is required. An op amp followed with the EL2008 can drive loads as low as 10Ω to ±10V.

Driving capacitive loads with any closed loop system creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The EL2008 output impedance is less than 10Ω from DC to 30 MHz. But a capacitive load of 1000 pF will generate about 45 degrees of phase shift at 30 MHz. More capacitance will cause the problem at lower frequency.

With enough capacitance even slow op amps will become unstable. The simplest way to drive capacitive loads is to isolate them from the feedback with a series resistor. 1Ω to 5Ω is usually enough but the final value will depend on the op amp used and the range of load capacitance.

<table>
<thead>
<tr>
<th>C_L</th>
<th>t_r</th>
<th>O.S.</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 pF</td>
<td>45 ns</td>
<td>20%</td>
</tr>
<tr>
<td>470 pF</td>
<td>50 ns</td>
<td>20%</td>
</tr>
<tr>
<td>1000 pF</td>
<td>55 ns</td>
<td>30%</td>
</tr>
<tr>
<td>3300 pF</td>
<td>60 ns</td>
<td>30%</td>
</tr>
<tr>
<td>0.1 μF</td>
<td>350 ns</td>
<td>0%</td>
</tr>
<tr>
<td>1 μF</td>
<td>4 μs</td>
<td>0%</td>
</tr>
<tr>
<td>5 μF</td>
<td>20 μs</td>
<td>0%</td>
</tr>
</tbody>
</table>
Applications Information — Contd.

Unfortunately the isolation resistor is not inside the op amp feedback loop and cannot be neglected when computing the DC voltage gain into a resistive load. If load dependent DC gain is not tolerable then additional high frequency feedback from the op amp output (the EL2008 input) and an isolation resistor from the buffer output can be used to stabilize the loop. This configuration requires the op amp to be unity gain stable. This feedback method will allow the EL2008 to boost the output of the EHA2505 amplifier below and serve as a variable, bipolar 1A voltage supply with short circuit protection.

Video Distribution Amplifier

The EL2008 can drive 15 double matched 75Ω cables. If the EL2008 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Dis-
Video Mux and Distribution Amplifier

![Amplifier Circuit Diagram]

- **Vin 1**: 75 Ω, Sel 1
- **Vin 2**: 75 Ω, Sel 2
- **R1**: 100 Ω
- **R2**:
- **C1**: 0.1 μF
- **C2**: 0.1 μF
- **R3**: 75 Ω
- **R4**: 75 Ω
- **R5**: 75 Ω
- **R6**: 75 Ω

Notes:
- 2008-11
EL2008 Macromodel

* Connections: +input
  * +Vsupply
  * –Vsupply
  * output

.subckt M2008 4 5 1 2

* Input Stage
  cl 10 0 4 0 1.0
  rl 10 0 1K
  rh 10 11 1K
  ch 11 0 2.65pF
  rc 11 12 10K
  cc 12 0 0.159pF
  e2 13 0 12 0 1.0

* Output Stage
  q1 1 13 14 qp
  q2 5 13 15 qn
  q3 5 14 16 qn 15
  q4 1 15 19 qp 15
  r2 16 2 0.4
  r3 19 2 0.4
  cl 14 0 0.6pF
  c2 15 0 0.6pF
  i1 5 14 1.2mA
  i2 15 1 1.2mA

* Bias Current
  iin+ 4 0 5μA

* Models
  .model qn npn (is = 5e−15 bf = 1500)
  .model qp pnp (is = 5e−15 bf = 1500)
  .ends
Features

- High slew rate—3000 V/μs
- Wide bandwidth—
  125 MHz @ R_L = 50Ω
  90 MHz @ R_L = 10Ω
- Output current—1A continuous
- Output impedance—1Ω
- Short circuit protected
- Power package with isolated metal tab

Applications

- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2009CT</td>
<td>0°C to +75°C</td>
<td>TO-220</td>
<td>MDP0028</td>
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General Description

The EL2009 is a patented high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing 40 mA of quiescent supply current. The EL2009's 3000 V/μs slew rate and 90 MHz bandwidth driving a 10Ω load insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2009.

Used as an open loop buffer, the EL2009's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load.

The EL2009 has an output short circuit current limit which will protect the device under both a DC fault condition and AC operation with reactive loads.

The EL2009 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2009, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore, the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2009CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Connection Diagram

5-Pin TO-220

Simplified Schematic

## Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_S)</td>
<td>Supply Voltage ((V_+ - V_-))</td>
<td>±18V or 36V</td>
<td>(T_A) Operating Temperature Range</td>
<td>0°C to +75°C</td>
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</tr>
<tr>
<td>(V_{IN})</td>
<td>Input Voltage (Note 1)</td>
<td>±15V or (V_S)</td>
<td>(T_J) Operating Junction Temp.</td>
<td>125°C</td>
<td></td>
</tr>
<tr>
<td>(I_{IN})</td>
<td>Input Current (Note 1)</td>
<td>±50 mA</td>
<td>(T_ST) Storage Temp. Range</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>(P_D)</td>
<td>Power Dissipation (Note 2)</td>
<td>See Curves</td>
<td>(T_LD) Lead Solder Temp. &lt; 10 seconds</td>
<td>300°C</td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

## Electrical Characteristics \(V_S = \pm 15V, R_S = 50Ω\), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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<td>Output Offset Voltage</td>
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<td>(V_{IN})</td>
<td>Input Current</td>
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<td>(\infty)</td>
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<td>-60</td>
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<tr>
<td>(R_{IN})</td>
<td>Input Impedance</td>
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<td>±12V</td>
<td>100Ω</td>
<td>25°C</td>
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<tr>
<td>(A_{V1})</td>
<td>Voltage Gain</td>
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<td>±10V</td>
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<td>25°C</td>
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<tr>
<td>(A_{V2})</td>
<td>Voltage Gain</td>
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<td>±10V</td>
<td></td>
<td>10Ω</td>
</tr>
<tr>
<td>(A_{V3})</td>
<td>Voltage Gain, (V_S = \pm 5V)</td>
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<td>25°C</td>
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<tr>
<td>(V_{O1})</td>
<td>Output Voltage Swing</td>
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<td>±14V</td>
<td>100Ω</td>
<td>25°C</td>
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<tr>
<td>(R_{O1})</td>
<td>Output Impedance</td>
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<td>±10V</td>
<td></td>
<td>25°C</td>
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<tr>
<td>(R_{O2})</td>
<td>Output Impedance</td>
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<td>±10V</td>
<td></td>
<td>±10 mA</td>
</tr>
<tr>
<td>(I_O)</td>
<td>Output Current</td>
<td></td>
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<td>(Note 3)</td>
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<tr>
<td>(I_S)</td>
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<td>(\infty)</td>
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<td>60</td>
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Electrical Characteristics  $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>$V_{S^+}, V_{S^-}$</td>
<td>Supply Sensitivity (Note 5)</td>
<td>$V_{IN}$ Load Temp</td>
<td>$Min$</td>
<td>$Typ$</td>
<td>$Max$</td>
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<tr>
<td>$SR_1$</td>
<td>Slew Rate (Note 6)</td>
<td>$\pm 10V$ $50\Omega$ $25^\circ C$</td>
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<td>2500</td>
<td>V</td>
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<tr>
<td>$SR_2$</td>
<td>Slew Rate (Note 7)</td>
<td>$\pm 5V$ $10\Omega$ $25^\circ C$</td>
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<td>2500</td>
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<td>$t_\text{r}$, $t_\text{f}$</td>
<td>Rise/Fall Time</td>
<td>$100 mV$ $25^\circ C$</td>
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<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>$BW$</td>
<td>-3 dB Bandwidth</td>
<td>$100 mV$ $25^\circ C$</td>
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<td>V</td>
<td>MHz</td>
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<td>$C_{IN}$</td>
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<td>V</td>
<td>pF</td>
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<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>$25^\circ C$</td>
<td>1</td>
<td>I</td>
<td>%</td>
</tr>
</tbody>
</table>

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds $\pm 7.5V$ then the input current must be limited to $\pm 50$ mA.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: Force the input to $+12 V$ and the output to $+10 V$ and measure the output current. Repeat with $-12 V$ input and $-10 V$ on the output.

Note 4: $V_S = \pm 4.5V$ then $V_S$ is changed to $\pm 18V$.

Note 5: $V_{S^+} = +15V$, $V_{S^-} = 4.5V$ then $V_{S^-}$ is changed to $-18V$ and $V_{S^+} = -15V$, $V_{S^-} = +4.5V$ then $V_{S^+}$ is changed to $+18V$.

Note 6: Slew Rate is measured between $V_{OUT} = +5V$ and $-5V$.

Note 7: Slew Rate is measured between $V_{OUT} = +2.5V$ and $-2.5V$.

Applications Information

The EL2009 is a higher bandwidth of the EL2008. It is recommended that you read the EL2008 application section.

Video Distribution Amplifier

The EL2009 can drive 15 double matched 75Ω cables. If the EL2009 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Disable) is used to multiplex between the inputs and can be easily expanded to accept more inputs. The circuit as shown when fully loaded has differential phase $<0.1^\circ$ and differential gain $<0.1%$. The 100Ω resistor at the EL2009 input (R1) is necessary to stabilize the loop. The EL2009 operates with a CLASS AB output which exhibits a slight rise in output impedance when-
Applications Information — Contd.  

ever the current it sources into the load approaches zero. In those cases, where differential gain and phase are measurably affected, resistor R2 may be added to ensure that the EL2009 output current never reaches zero. This will result in a CLASS A output stage with active pulldown but with the penalty of power dissipation in R2. More information about driving cables can be found in the EL2003 data sheet.

Video Mux and Distribution Amp.

![Video Mux and Distribution Amp. Diagram]
EL2009 Macromodel

* Connections:  
  +input  
  +Vs supply  
  -Vs supply  
  output

* .subckt M2009 4 5 1 2

* Input Stage  
  e1 1 0 4 0 1.0  
  r1 1 0 1K  
  rh 10 11 1K  
  ch 11 0 1pF  
  rc 11 12 6.3K  
  cc 12 0 0.159pF  
  e2 13 0 12 0 1.0  
  *

* Output Stage  
  q1 1 13 14 qp  
  q2 5 13 15 qn  
  q3 5 14 16 qn 10  
  q4 1 15 16 qp 10  
  r2 16 2 0.2  
  r3 19 2 0.2  
  cl 14 0 1.7pF  
  cl 15 0 1.7pF  
  i1 5 14 5mA  
  i2 15 1 5mA  
  *

* Bias Current  
  iin + 405 1-A  
  *

* Models  
  .model qn nnpn (is = 5e-15 bf = 500)  
  .model qp npnp (is = 5e-15 bf = 500)  
  *

.ends
Features
• Slew rate 500 V/μs
• ±33 mA output current
• Drives ±2.4 V into 75Ω
• Differential phase <0.1°
• Differential gain <0.1%
• V supply ±5 V to ±18 V
• Output short circuit protected
• Uses current mode feedback
• 1% settling time of 50 ns for 10 V step
• Low cost
• 9 mA supply current
• 8-pin mini-dip

Applications
• Video gain block
• Residue amplifier
• Radar systems
• Current to voltage converter
• Coax cable driver with gain of 2

General Description
The EL2020 is a fast settling, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

The EL2020 will drive two double terminated 75Ω coax cables to video levels with low distortion. Since it is a closed loop device, the EL2020 provides better gain accuracy and lower distortion than an open loop buffer. The device includes output short circuit protection, and input offset adjust capability.

The bandwidth and slew rate of the EL2020 are relatively independent of the closed loop gain taken. The 50 MHz bandwidth at unity gain only reduces to 30 MHz at a gain of 10. The EL2020 may be used in most applications where a conventional op amp is used, with a big improvement in speed power product.

Elantec products and facilities comply with Elantec document, QRA-1: Processing-Monolithic Products.

Ordering Information
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2020CN</td>
<td>−40°C to +85°C</td>
<td>P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2020CM</td>
<td>−40°C to +85°C</td>
<td>20-Lead</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagrams
### Absolute Maximum Ratings (25°C)

- **Vs** Supply Voltage: ±18V or 36V
- **Vin** Input Voltage: ±15V or Vs
- **AVin** Differential Input Voltage: ±10V
- **IN** Input Current (Pins 2 or 3): ±10 mA
- **INS** Input Current (Pins 1, 5, or 8): ±5 mA
- **PD** Maximum Power Dissipation (See Curves): 1.25W
- **IOP** Peak Output Current: Short Circuit Protected
- **VSS** Supply Voltage: ±15V or Vss

### Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore **Tj** = **TC** = **TA**.

### Open Loop Characteristics **Vs** = ±15V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VOS</strong> (Note 1)</td>
<td>Input Offset Voltage</td>
<td>25°C</td>
<td>Min</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typ</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Max</td>
<td>III</td>
<td>mV</td>
</tr>
<tr>
<td><strong>AVOS/ΔT</strong></td>
<td>Offset Voltage Drift</td>
<td></td>
<td></td>
<td></td>
<td>µV/°C</td>
</tr>
<tr>
<td><strong>CMRR</strong> (Note 3)</td>
<td>Common Mode Rejection Ratio</td>
<td>ALL</td>
<td>Min</td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typ</td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td><strong>PSRR</strong> (Note 4)</td>
<td>Power Supply Rejection Ratio</td>
<td>25°C</td>
<td>Min</td>
<td>III</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typ</td>
<td>III</td>
<td>dB</td>
</tr>
<tr>
<td><strong>+IN</strong></td>
<td>Non-inverting Input Current</td>
<td>25°C</td>
<td>Min</td>
<td>II</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typ</td>
<td>II</td>
<td>µA</td>
</tr>
<tr>
<td><strong>+RIN</strong></td>
<td>Non-Inverting Input Resistance</td>
<td>ALL</td>
<td>Min</td>
<td>II</td>
<td>MΩ</td>
</tr>
<tr>
<td><strong>+IPSR</strong> (Note 4)</td>
<td>Non-Inverting Input Current</td>
<td>25°C</td>
<td>Min</td>
<td>II</td>
<td>µA/V</td>
</tr>
<tr>
<td><strong>-IN</strong> (Note 1)</td>
<td>- Input Current</td>
<td>25°C</td>
<td>Min</td>
<td>II</td>
<td>µA</td>
</tr>
</tbody>
</table>

**Note:** Parameter is guaranteed (but not tested) by Design and Characterization Data. Parameter is typical value at **TA** = 25°C for information purposes only.
## Open Loop Characteristics $V_S = \pm 15V$ — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>$-ICMR$ (Note 3)</td>
<td>$-Input$ Current</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>0.5</td>
<td>2.0</td>
<td>II</td>
</tr>
<tr>
<td></td>
<td>Common Mode Rejection</td>
<td>$T_{MIN}$</td>
<td>4.0</td>
<td>III</td>
<td>$\mu A/V$</td>
</tr>
<tr>
<td>$-IPSR$ (Note 4)</td>
<td>$-Input$ Current</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>0.05</td>
<td>0.5</td>
<td>II</td>
</tr>
<tr>
<td></td>
<td>Power Supply Rejection</td>
<td>$T_{MIN}$</td>
<td>1.0</td>
<td>III</td>
<td>$\mu A/V$</td>
</tr>
<tr>
<td>$R_{ol}$</td>
<td>Transimpedence ($\Delta V_{OUT}/\Delta(-I_{IN})$)</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>300</td>
<td>1000</td>
<td>II</td>
</tr>
<tr>
<td></td>
<td>$R_L = 400\Omega$, $V_{OUT} = \pm 10V$</td>
<td>$T_{MIN}$</td>
<td>50</td>
<td>III</td>
<td>V/mA</td>
</tr>
<tr>
<td>$AVOL_1$</td>
<td>Open Loop DC Voltage Gain</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>70</td>
<td>80</td>
<td>II</td>
</tr>
<tr>
<td></td>
<td>$R_L = 400\Omega$, $V_{OUT} = \pm 10V$</td>
<td>$T_{MIN}$</td>
<td>60</td>
<td>III</td>
<td>dB</td>
</tr>
<tr>
<td>$AVOL_2$</td>
<td>Open Loop DC Voltage Gain</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>60</td>
<td>70</td>
<td>II</td>
</tr>
<tr>
<td></td>
<td>$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$</td>
<td>$T_{MIN}$</td>
<td>55</td>
<td>III</td>
<td>dB</td>
</tr>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>$\pm 12$</td>
<td>$\pm 13$</td>
<td>II</td>
</tr>
<tr>
<td></td>
<td>$R_L = 400\Omega$</td>
<td>$T_{MIN}$</td>
<td>$\pm 11$</td>
<td>III</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>$\pm 30$</td>
<td>$\pm 32.5$</td>
<td>II</td>
</tr>
<tr>
<td></td>
<td>$R_L = 400\Omega$</td>
<td>$T_{MIN}$</td>
<td>$\pm 27.5$</td>
<td>III</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Quiescent Supply Current</td>
<td>$25^\circ C$</td>
<td>9</td>
<td>12</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>15</td>
<td>III</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{off}$</td>
<td>Supply Current, Disabled, $V_S = 0V$</td>
<td>ALL</td>
<td>5.5</td>
<td>7.5</td>
<td>II</td>
</tr>
<tr>
<td>$I_{logic}$</td>
<td>Pin 8 Current, Pin 8 = 0V</td>
<td>ALL</td>
<td>1.1</td>
<td>1.5</td>
<td>II</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Min Pin 8 Current to Disable</td>
<td>ALL</td>
<td>120</td>
<td>250</td>
<td>II</td>
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<tr>
<td>$I_{CE}$</td>
<td>Max Pin 8 Current to Enable</td>
<td>ALL</td>
<td>30</td>
<td>II</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Parameter</td>
<td>Description</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Test Level</td>
</tr>
<tr>
<td>-----------</td>
<td>-------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------------</td>
</tr>
<tr>
<td>SR1</td>
<td>Closed Loop Gain of 1 V/V (0 dB), $R_P = 1 , k\Omega$</td>
<td>300</td>
<td>500</td>
<td>I</td>
<td>V/µs</td>
</tr>
<tr>
<td>FPBW1</td>
<td>Full Power Bandwidth (Note 5)</td>
<td>4.77</td>
<td>7.95</td>
<td>I</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise Time, $R_I = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%</td>
<td>6</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall Time, $R_I = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%</td>
<td>6</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_p$</td>
<td>Propagation Delay, $R_I = 100\Omega$, $V_{OUT} = 1V$, 50% Points</td>
<td>8</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>BW</td>
<td>Closed Loop Gain of 1 V/V (0 dB), $R_P = 820\Omega$</td>
<td>50</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>$-3 , dB$ Small Signal Bandwidth, $R_I = 100\Omega$, $V_O = 100 , mV$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_s$</td>
<td>1% Settling Time, $R_I = 400\Omega$, $V_O = 10V$</td>
<td>50</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>0.1% Settling Time, $R_I = 400\Omega$, $V_O = 10V$</td>
<td>90</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>SR10</td>
<td>Closed Loop Gain of 10 V/V (20 dB), $R_P = 1 , k\Omega$, $R_G = 111\Omega$</td>
<td>300</td>
<td>500</td>
<td>I</td>
<td>V/µs</td>
</tr>
<tr>
<td>FPBW10</td>
<td>Full Power Bandwidth (Note 5)</td>
<td>4.77</td>
<td>7.95</td>
<td>I</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise Time, $R_I = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%</td>
<td>25</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall Time, $R_I = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%</td>
<td>25</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_p$</td>
<td>Propagation Delay, $R_I = 100\Omega$, $V_{OUT} = 1V$, 50% points</td>
<td>12</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>BW</td>
<td>Closed Loop Gain of 10 V/V (20 dB), $R_P = 680\Omega$, $R_G = 76\Omega$</td>
<td>30</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>$-3 , dB$ Small Signal Bandwidth, $R_I = 100\Omega$, $V_O = 100 , mV$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_s$</td>
<td>1% Settling Time, $R_I = 400 , \Omega$, $V_O = 10V$</td>
<td>55</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>0.1% Settling Time, $R_I = 400 , \Omega$, $V_O = 10V$</td>
<td>280</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: The offset voltage and inverting input current can be adjusted with an external 10 kΩ pot between pins 1 and 5 with the wiper connected to $V_{CC}$ (Pin 7) to make the output offset voltage zero.

Note 2: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 3: $V_{CM} = \pm 10V$.

Note 4: $\pm 4.5V \leq V_S \leq \pm 18V$.

Note 5: Full Power Bandwidth is guaranteed based on Slew Rate measurement. $FPBW = SR/2\pi V_{peak}$.
Typical Performance Curves Non-Inverting Gain of One

AVCL = +1

Gain vs Frequency

Phase Shift vs Frequency

Settling Time vs Output Swing

-3 dB Bandwidth vs Supply Voltage

Rise Time and Prop Delay vs Temperature

Slew Rate vs Supply Voltage

Slew Rate vs Temperature

2020-4
Typical Performance Curves — Contd. Inverting Gain of One

\[
\text{AVCL} = -1
\]

Gain vs Frequency

\[
\begin{align*}
\text{AVCL} &= -1 \\
R_F &= R_G = 750 \Omega \\
R_L &= 1 \Omega \\
R_L &= 50 \Omega
\end{align*}
\]

Phase Shift vs Frequency

\[
\begin{align*}
\text{AVCL} &= -1 \\
R_F &= R_G = 750 \Omega \\
R_L &= 1 \Omega \\
R_L &= 50 \Omega
\end{align*}
\]

Supply Voltage (V)

Temperature (°C)

-3 dB Bandwidth vs Output Swing

\[
\begin{align*}
\text{AvCL} &= -1, R_L = 100 \Omega \\
V_S &= \pm 15 \text{V} \\
R_L &= 400 \Omega
\end{align*}
\]

Rise Time and Prop Delay vs Temperature

\[
\begin{align*}
V_S &= \pm 15 \text{V}, V_{OUT} = \pm 0.5 \text{V} \\
\text{AVCL} &= -1 \\
R_L &= 1 \Omega \\
R_L &= 50 \Omega
\end{align*}
\]

Supply Voltage (V)

Temperature (°C)

Slew Rate vs Supply Voltage

\[
\begin{align*}
\text{AvCL} &= -1 \\
R_L &= 1 \Omega \\
R_L &= 1 \Omega
\end{align*}
\]

Slew Rate vs Temperature

\[
\begin{align*}
V_S &= \pm 15 \text{V}, R_L = 400 \Omega \\
\text{AVCL} &= -1
\end{align*}
\]

Supply Voltage (V)

Temperature (°C)
Typical Performance Curves — Contd. Non-Inverting Gain of Two

Gain vs Frequency

Phase Shift vs Frequency

Settling Time vs Output Swing

-3 dB Bandwidth vs Supply Voltage

Rise Time and Prop Delay vs Temperature

Slew Rate vs Supply Voltage

Slew Rate vs Temperature
Typical Performance Curves — Contd. Non-Inverting Gain of Ten

Gain vs Frequency

Phase Shift vs Frequency

Gain vs Frequency

Phase Shift vs Frequency

Settling Time vs Output Swing

-3 dB Bandwidth vs Supply Voltage

Rise Time and Prop Delay vs Temperature

Slew Rate vs Supply Voltage

Slew Rate vs Temperature
Typical Performance Curves — Contd.

- **Maximum Undistorted Output Voltage vs Frequency**
  - Frequency (MHz) vs Output Voltage (V-p)

- **Input Resistance vs Temperature**
  - Temperature (°C) vs Input Resistance (MΩ)
  - AVCL = 10
  - AVCL = 1

- **PSRR vs Frequency**
  - Frequency (Hz) vs PSRR (dB)

- **Voltage Noise vs Frequency**
  - Frequency (Hz) vs Voltage Noise (nV/√Hz)

- **Current Noise vs Frequency**
  - Frequency (Hz) vs Current Noise (pA/√Hz)

- **Output Impedance vs Frequency**
  - Frequency (Hz) vs Output Impedance (Ω)

- **Supply Current vs Supply Voltage**
  - Supply Voltage (V) vs Supply Current (mA)

- **8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature**
  - Temperature (°C) vs Power Dissipation (W)
  - TJ MAX = 150°C
  - θJC = 50°C/W
  - θJA = 85°C/W

- **20-Lead SOL Maximum Power Dissipation vs Ambient Temperature**
  - Temperature (°C) vs Power Dissipation (W)
  - TJ MAX = 150°C
  - θJC = 85°C/W
  - FREE AIR NO HEAT SINK
  - FREE AIR HEAT SINK
  - INFINITE HEAT SINK

*2020-8*
Application Information

Theory of Operation
The EL2020 has a unity gain buffer similar to the EL2003 from the non-inverting input to the inverting input. The error signal of the EL2020 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is the transresistance ($R_{OL}$) of the EL2020 ($V_{OUT} = R_{OL} \times I_{INV}$). Since $R_{OL}$ is very large ($\approx 10^6$), the current flowing into the inverting input in the steady state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first order approximation for circuit analysis, namely that...
1. The voltage across the inputs $\approx 0$ and
2. The current into the inputs is $\approx 0$

Simplified Block Diagram of EL2020

Resistor Value Selection and Optimization
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2020. A nominal value for the feedback resistor is 1 kΩ, which is the value used for production testing. This value guarantees stability. For a given gain, the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth will be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower $-3$ dB frequency. Attenuation at high frequency is limited by a zero in the closed loop transfer function which results from stray capacitance between the inverting input and ground.

Power Supplies
The EL2020 may be operated with single or split power supplies as low as $\pm 3V$ (6V total) to as high as $\pm 18V$ (36V total). The slew rate degrades significantly for supply voltages less than $\pm 5V$ (10V total), but the bandwidth only changes 25% for supplies from $\pm 3V$ to $\pm 18V$. It is not necessary to use equal value split power supplies, i.e., $-5V$ and $+12V$ would be excellent for 0V to 1V video signals. Bypass capacitors from each supply pin to a ground plane are recommended. The EL2020 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate supply ringing and the errors it might cause, a 4.7 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rate and longer settling times.
Application Information — Contd.

Summing Amplifier

![Diagram of a summing amplifier](image)

EL2020 Typical Inverting Amplifier Characteristics

<table>
<thead>
<tr>
<th>AV</th>
<th>RF</th>
<th>R1, R2</th>
<th>Bandwidth</th>
<th>10V Settling Time</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1%</td>
</tr>
<tr>
<td>−1</td>
<td>750Ω</td>
<td>750Ω</td>
<td>40 MHz</td>
<td>50 ns</td>
</tr>
<tr>
<td>−2</td>
<td>750Ω</td>
<td>375Ω</td>
<td>40 MHz</td>
<td>55 ns</td>
</tr>
<tr>
<td>−5</td>
<td>680Ω</td>
<td>130Ω</td>
<td>40 MHz</td>
<td>55 ns</td>
</tr>
<tr>
<td>−10</td>
<td>680Ω</td>
<td>68Ω</td>
<td>30 MHz</td>
<td>70 ns</td>
</tr>
</tbody>
</table>

Input Range

The non-inverting input to the EL2020 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit.

The input characteristics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that Schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2020 is fairly tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources may cause oscillations; a 1 kΩ resistor in series with the input lead will usually eliminate problems without sacrificing too much speed.

Current Limit

The EL2020 has internal current limits that protect the output transistors. The current limit goes down with junction temperature rise. At a junction temperature of +175°C the current limits are at about 50 mA. If the EL2020 output is shorted to ground when operating on ±15V supplies, the power dissipation could be as great as 1.1W. A heat sink is required in order for the EL2020 to survive an indefinite short. Recovery time to come out of current limit is about 50 ns.

Using the 2020 with Output Buffers

When more output current is required, a wideband buffer amplifier can be included in the feedback loop of the EL2020. With the EL2003 the subsystem overshoots about 10% due to the phase lag of the EL2003. With the EL2004 in the loop, the overshoot is less than 2%. For even more output current, several buffers can be paralleled.

Capacitive Loads

The EL2020 is like most high speed feedback amplifiers in that it does not like capacitive loads between 50 pF and 1000 pF. The output resistance works with the capacitive load to form a second non-dominant pole in the loop. This results in excessive peaking and overshoot and can lead to oscillations. Standard resistive isolation techniques used with other op amps work well to isolate capacitive loads from the EL2020.
Application Information — Contd.

**Offset Adjust**
To calculate the amplifier system offset voltage from input to output we use the equation:

\[
\text{Output Offset Voltage} = V_{OS} \left( \frac{R_F}{R_G} + 1 \right) \pm I_{BIAS} R_F
\]

The EL2020 output offset can be nulled by using a 10 kΩ potentiometer from pins 1 to 5 with the slider tied to pin 7 (+VCC). This adjusts both the offset voltage and the inverting input bias current. The typical adjustment range is \( \pm 80 \text{ mV} \) at the output.

**Compensation**
The EL2020 is internally compensated to work with external feedback resistors for optimum bandwidth over a wide range of closed loop gain. The part is designed for a nominal 1 kΩ of feedback resistance, although it is possible to get more bandwidth by decreasing the feedback resistance.

The EL2020 becomes less stable by adding capacitance in parallel with the feedback resistor, so feedback capacitance is not recommended.

The EL2020 is also sensitive to stray capacitance from the inverting input to ground, so the board should be laid out to keep the physical size of this node small, with ground plane kept away from this node.

**Active Filters**
The EL2020's low phase lag at high frequencies makes it an excellent choice for high performance active filters. The filter response more closely approaches the theoretical response than with conventional op amps due to the EL2020's smaller propagation delay. Because the internal compensation of the EL2020 depends on resistive feedback, the EL2020 should be set up as a gain block.

**Driving Cables**
The EL2020 was designed with driving coaxial cables in mind. With 30 mA of output drive and low output impedance, driving one to three 75Ω double terminated coax cables with one EL2020 is practical. Since it is easy to set up a gain of +2, the double matched method is the best way to drive coax cables, because the impedance match on both ends of the cable will suppress reflections. For a discussion on some of the other ways to drive cables, see the section on driving cables in the EL2003 data sheet.

**Video Performance Characteristics**
The EL2020 makes an excellent gain block for video systems, both RS-170 (NTSC) and faster. It is capable of driving 3 double terminated 75Ω cables with distortion levels acceptable to broadcasters. A common video application is to drive a 75Ω double terminated coax with a gain of 2.

To measure the video performance of the EL2020 in the non-inverting gain of 2 configuration, 5 identical gain-of-two circuits were cascaded (with a divide by two 75Ω attenuator between each stage) to increase the errors.

The results, shown in the photos, indicate the entire system of 5 gain-of-two stages has a differential gain of 0.5% and a differential phase of 0.5°. This implies each device has a differential gain/phase of 0.1% and 0.1°, but these are too small to measure on single devices.
Application Information — Contd.

Video Distribution Amplifier
The distribution amplifier shown below features a difference input to reject common mode signals on the 75Ω coax cable input. Common mode rejection is often necessary to help to eliminate 60 Hz noise found in production environments.

![Video Distribution Amplifier with Difference Input](image)

EL2020 Disable/Enable Operation
The EL2020 has an enable/disable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to pin 7, VCC. When more than 250 μA is pulled from pin 8, the EL2020 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is halved. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (~1.1 mA) if pin 8 is grounded.

To draw current out of pin 8 an "open collector output" logic gate or a discrete NPN transistor can be used. This logic interface method has the advantage of level shifting the logic signal from 5V supplies to whatever supply the EL2020 is operating on without any additional components.

Using the EL2020 as a Multiplexer
An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown.

When the EL2020 is disabled, the DC output impedance is very high, over 10 kΩ. However there is also an output capacitance that is non-linear. For signals of less than 5V peak to peak, the output capacitance looks like a simple 15 pF capacitor. However, for larger signals the output capacitance becomes much larger and non-linear.

The example multiplexer will switch between amplifiers in 5 μs for signals of less than ±2V on the outputs. For full output signals of 20V peak to peak, the selection time becomes 25 μs. The disabled outputs also present a capacitive load and therefore only three amplifiers can have their outputs shorted together. However an unlimited number can sum together if a small resistor (25 kΩ) is inserted in series with each output to isolate it from the "bus". There will be a small gain loss due to the resistors of course.

Using the EL2020 as a Multiplexer
Burn-In Circuit

Pin numbers are for DIP Packages. All Packages Use the Same Schematic.

Equivalent Circuit
EL2020 Macromodel

* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:
  + input
  | -input
  | + Vsupply
  | -Vsupply
  | output

.subckt M2020 3 2 7 4 6

* Input Stage
  c1 10 0 3 0 1.0
  vis 10 9 0V
  h2 9 12 vxx 1.0
  r1 2 11 50
  l1 11 12 2nH
  iinp 3 0 10μA
  iinm 2 0 5μA

* Slew Rate Limiting
  h1 13 0 vis 600
  r2 13 14 1K
  d1 14 0 dclamp
  d2 0 14 dclamp

* High Frequency Pole
  *e2 30 0 14 0 0.0016666666666
  15 30 17 1.5μH
  c5 17 0 1pF
  r5 17 0 500

* Transimpedance Stage
  g1 0 18 17 0 1.0
  rol 18 0 1Meg
  cdp 18 0 5pF

* Output Stage
  q1 4 18 19 qp
  q2 7 18 20 qa
  q3 7 19 21 qa
  q4 4 20 22 qp
  r7 21 6 4
  r8 22 6 4
EL2020 Macromodel — Contd.

ios1 7 19 2.5mA
ios2 20 4 2.5mA

* Supply
* 
ips 7 4 3mA

* Error Terms
* 
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 23 1K

* Models
* 
.model qn npn (is = 5e-15 bf = 100 tf = 0.2nS)
.model qp pnp (is = 5e-15 bf = 100 tf = 0.2nS)
.model dclamp d(is = 1e - 30 ibv = 0.266 bv = 1.67 n = 4)
.ends
EL2020 Macromodel

[Diagram of EL2020 Macromodel]
Features

• $-3$ dB bandwidth $= 120$ MHz, $A_V = 1$
• $-3$ dB bandwidth $= 110$ MHz, $A_V = 2$
• 0.01% differential gain and 0.01° differential phase (NTSC, PAL)
• 0.05% differential gain and 0.02° differential phase (HDTV)
• Slew rate 2000 V/µs
• 65 mA output current
• Drives $±10$V into 200Ω load
• Characterized at $±5$V and $±15$V
• Low voltage noise
• Current mode feedback
• Settling time of 40 ns to 0.25% for a 10V step
• Output short circuit protected
• Low cost

Applications

• Video gain block
• Video distribution amplifier
• HDTV amplifier
• Residue amplifiers in ADC
• Current to voltage converter
• Coax cable driver

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2030CN</td>
<td>$-40^\circ$C to $+85^\circ$C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2030CM</td>
<td>$-40^\circ$C to $+85^\circ$C</td>
<td>20-Lead SOL</td>
<td>MDP0027</td>
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</tbody>
</table>

General Description

The EL2030 is a very fast, wide bandwidth amplifier optimized for gains between $-10$ and $+10$. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

Due to its wide operating supply range ($±15$V) and extremely high slew rate of 2000 V/µs, the EL2030 drives $±10$V into 200Ω at a frequency of 30 MHz, while achieving 110 MHz of small signal bandwidth at $A_V = +2$. This bandwidth is still 95 MHz for a gain of $+10$. On $±5$V supplies the amplifier maintains a 90 MHz bandwidth for $A_V = +2$. When used as a unity gain buffer, the EL2030 has a 120 MHz bandwidth with the gain precision and low distortion of closed loop buffers.

The EL2030 features extremely low differential gain and phase, a low noise topology that reduces noise by a factor of 2 over competing amplifiers, and settling time of 40 ns to 0.25% for a 10V step. The output is short circuit protected. In addition, datasheet limits are guaranteed for $±5$V and $±15$V supplies.

Elantec's products and facilities comply with applicable quality specifications. See Elantec document, QRA-1: Processing, Monolithic Integrated Circuits.

Connection Diagrams

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,893,091.
### Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>TA</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS</td>
<td>Supply Voltage</td>
<td>±18V or 36V</td>
<td>T_A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_IN</td>
<td>Input Voltage</td>
<td>±15V or VS</td>
<td>T_J</td>
<td></td>
<td></td>
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<tr>
<td>ΔVIN</td>
<td>Differential Input Voltage</td>
<td>±6V</td>
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<td></td>
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<tr>
<td>P_D</td>
<td>Maximum Power Dissipation</td>
<td>See Curves</td>
<td>T_S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_IN</td>
<td>Input Current</td>
<td>±10 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>I_OP</td>
<td>Peak Output Current</td>
<td>Short Circuit Protected</td>
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<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

Output Short Circuit Duration Continuous

(Note 1)

### Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore T_A = T_C = T_A.

### Test Level

<table>
<thead>
<tr>
<th>Test Procedure</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>I 100% production tested</td>
<td>VA = ±15V, TA = 25°C and QA sample tested at VA = ±15V, TA = 25°C; T_MAX and T_MIN per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II 100% production tested</td>
<td>VA = ±15V, TA = 25°C and QA sample tested at VA = ±15V, TA = 25°C; T_MAX and T_MIN per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III QA sample tested</td>
<td>VA = ±15V, TA = 25°C and QA sample tested at VA = ±15V, TA = 25°C; T_MAX and T_MIN per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
<td></td>
</tr>
<tr>
<td>V Parameter is typical value at T_A = 25°C for information purposes only.</td>
<td></td>
</tr>
</tbody>
</table>

### Open Loop DC Electrical Characteristics

VS = ±15V, RL = 200Ω, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>VS = ±15V</td>
<td>25°C</td>
<td>10</td>
<td>20</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>T_MIN, T_MAX</td>
<td>30</td>
<td></td>
<td></td>
<td>III</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VS = ±5V</td>
<td>25°C</td>
<td>5</td>
<td>10</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>T_MIN, T_MAX</td>
<td>15</td>
<td></td>
<td></td>
<td>III</td>
<td></td>
</tr>
<tr>
<td>ΔVOS/ΔT</td>
<td>Offset Voltage Drift</td>
<td></td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>μV/°C</td>
</tr>
<tr>
<td>+I_IN</td>
<td>+ Input Current</td>
<td>VS = ±5V, ±15V</td>
<td>25°C</td>
<td>5</td>
<td>15</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>T_MIN, T_MAX</td>
<td>25</td>
<td></td>
<td></td>
<td>III</td>
<td>μA</td>
</tr>
<tr>
<td>-I_IN</td>
<td>- Input Current</td>
<td>VS = ±5V, ±15V</td>
<td>25°C</td>
<td>10</td>
<td>40</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>T_MIN, T_MAX</td>
<td>50</td>
<td></td>
<td></td>
<td>III</td>
<td>μA</td>
</tr>
<tr>
<td>+R_IN</td>
<td>+ Input Resistance</td>
<td></td>
<td>Full</td>
<td>1.1</td>
<td>2.0</td>
<td></td>
<td>II</td>
<td>MΩ</td>
</tr>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
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<td>25°C</td>
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<td></td>
<td>1</td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio (Note 2)</td>
<td>VS = ±5V, ±15V</td>
<td>Full</td>
<td>50</td>
<td>60</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>-ICMR</td>
<td>Input Current Common Mode Rejection (Note 2)</td>
<td>25°C</td>
<td>5</td>
<td>10</td>
<td></td>
<td>I</td>
<td>μA/V</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Note 3)</td>
<td></td>
<td>Full</td>
<td>60</td>
<td>70</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>+IPSR</td>
<td>+ Input Current Power Supply Rejection (Note 3)</td>
<td>25°C</td>
<td>0.1</td>
<td>0.5</td>
<td></td>
<td>II</td>
<td>μA/V</td>
<td></td>
</tr>
<tr>
<td>-IPSR</td>
<td>- Input Current Power Supply Rejection (Note 3)</td>
<td>25°C</td>
<td>0.5</td>
<td>5.0</td>
<td></td>
<td>II</td>
<td>μA/V</td>
<td></td>
</tr>
</tbody>
</table>
### Open Loop DC Electrical Characteristics

\( V_S = \pm 15V, R_L = 200\Omega, \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level EL2030C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{OL} )</td>
<td>Transimpedance ((\Delta V_{OUT}/\Delta (-I_{IN})))</td>
<td>( V_S = \pm 15V )</td>
<td>25°C</td>
<td>88</td>
<td>150</td>
<td>II</td>
<td>V/mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{OUT} = \pm 2.5V )</td>
<td>( V_S = \pm 5V )</td>
<td>25°C</td>
<td>80</td>
<td>120</td>
<td>II</td>
<td>V/mA</td>
<td></td>
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<tr>
<td>( A_{VOL} )</td>
<td>Open Loop DC Voltage Gain</td>
<td>( V_S = \pm 15V )</td>
<td>Full</td>
<td>60</td>
<td>70</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{OUT} = \pm 2.5V )</td>
<td>( V_S = \pm 5V )</td>
<td>Full</td>
<td>56</td>
<td>65</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing</td>
<td>( V_S = \pm 15V )</td>
<td>Full</td>
<td>12</td>
<td>13</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>Full</td>
<td>3</td>
<td>3.5</td>
<td>II</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output Current</td>
<td>( V_S = \pm 15V )</td>
<td>Full</td>
<td>60</td>
<td>65</td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>Full</td>
<td>30</td>
<td>35</td>
<td>II</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>Output Resistance</td>
<td>25°C</td>
<td>5</td>
<td></td>
<td></td>
<td>V</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>( I_S )</td>
<td>Quiescent Supply Current</td>
<td></td>
<td>Full</td>
<td>15</td>
<td>21</td>
<td>II</td>
<td>mA</td>
<td></td>
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<tr>
<td>( I_{SC} )</td>
<td>Short Circuit Current</td>
<td>25°C</td>
<td>85</td>
<td></td>
<td></td>
<td>V</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

### Closed Loop AC Electrical Characteristics

\( V_S = \pm 15V, A_V = +2, R_F = 820\Omega, R_O = 820\Omega \) and \( R_L = 200\Omega \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level EL2030C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( SR )</td>
<td>Slew Rate (Note 7)</td>
<td></td>
<td>25°C</td>
<td>1200</td>
<td>2000</td>
<td>IV</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>( FPBW )</td>
<td>Full Power Bandwidth (Note 4)</td>
<td></td>
<td>25°C</td>
<td>19</td>
<td>31.8</td>
<td>IV</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( t_{Rf} )</td>
<td>Rise Time. Fall Time</td>
<td>( V_{PP} = 250 \text{ mV} )</td>
<td>25°C</td>
<td>3</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_s )</td>
<td>Settling Time to 0.25% for 10V step (Note 5)</td>
<td></td>
<td>25°C</td>
<td>40</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( \Delta G )</td>
<td>Differential Gain (Note 8)</td>
<td></td>
<td>25°C</td>
<td>0.01</td>
<td></td>
<td>V</td>
<td>% p-p</td>
<td></td>
</tr>
<tr>
<td>( \Delta \phi )</td>
<td>Differential Phase (Note 8)</td>
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<td>25°C</td>
<td>0.01</td>
<td></td>
<td>V</td>
<td>* p-p</td>
<td></td>
</tr>
<tr>
<td>( eN )</td>
<td>Input Spot Noise at 1 kHz ( R_G = 101; R_P = 909 )</td>
<td></td>
<td>25°C</td>
<td>4</td>
<td></td>
<td>V</td>
<td>nV/√Hz</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: \( V_{CM} = \pm 10V \) for \( V_S = \pm 15V \). For \( V_S = \pm 5V, V_{CM} = \pm 2.5V \).

Note 3: \( V_{OS} \) is measured at \( V_S = \pm 4.5V \) and at \( V_S = \pm 18V \). Both supplies are changed simultaneously.

Note 4: Full Power Bandwidth is specified based on Slew Rate measurement \( FPBW = SR/2\pi V_p \).

Note 5: Settling Time measurement techniques are shown in: "Take The Guesswork Out of Settling Time Measurements", EDN, September 19, 1985. Available from the factory upon request.

Note 6: \( R_L = 100Ω \).

Note 7: \( V_O = \pm 10V \), tested at \( V_O = \pm 5V \). See test circuit.

Note 8: NTSC (3.58 MHz) and PAL (4.43 MHz).

Note 9: For \( V_S = \pm 15V, V_{OUT} = \pm 10V \). For \( V_S = \pm 5V, V_{OUT} = \pm 2.5V \).
Typical Performance Curves

Figure 1. NTSC Video Differential Gain and Phase Test Set-Up

Differential Gain and Phase vs Load Resistance, Gain = +1

Differential Gain and Phase vs Load Capacitance, Gain = +1

Differential Gain and Phase vs Supply Voltage, Gain = +1

Differential Gain and Phase vs Load Resistance, Gain = +2

Differential Gain and Phase vs Load Capacitance, Gain = +2

Differential Gain and Phase vs Supply Voltage, Gain = +2
Typical Performance Curves — Contd.

Figure 2. HDTV and Wideband Video Differential Gain and Phase Test Set-Up

Differential Gain Error vs Frequency for Various DC Output Levels

Differential Phase Error vs Frequency for Various DC Output Levels

Risetime and Overshoot vs \( R_F \)
for \( A_V = +1 \)

Bandwidth and Peaking vs \( R_F \)
for \( A_V = +1 \)

\( \pm \) Slew Rate vs Supply Voltage
Typical Performance Curves — Contd.

Risetime and Overshoot vs \( R_F \) for \( A_V = +2 \)

Bandwidth and Peaking vs \( R_F \) for \( A_V = +2 \)

\(-3\) dB Bandwidth vs Supply Voltage

Voltage Gain vs Frequency for \( A_V = +2 \), various Capacitive Loads

Risetime and Overshoot vs \( R_F \) for \( A_V = +10 \)

Bandwidth and Peaking vs \( R_F \) for \( A_V = +10 \)

\(-3\) dB Bandwidth vs Frequency for \( A_V = +2 \), various Capacitive Loads

Risetime and Overshoot vs \( R_F \) for \( A_V = +2 \), \( V_S = \pm 5V \)

Bandwidth and Peaking vs \( R_F \) for \( A_V = +2 \), \( V_S = \pm 5V \)

Output Settling Error vs Time
Typical Performance Curves — Contd.

Output Settling Error vs Time, $V_S = \pm 5\text{V}$

Input Offset Voltage vs Temperature

Input Bias Current vs Temperature

Output Swing vs Supply Voltage

Transimpedance ($R_{OL}$)

Supply Current vs Supply Voltage

Current Limit vs Temperature

Power Supply Rejection vs Frequency

Common Mode Rejection vs Frequency
Typical Performance Curves — Contd.

**Equivalent Input Noise**

- **Frequency (Hz)** vs **Input Noise Voltage (mV)** and **Input Noise Current (pA/√Hz)**

**Long-Term Output Settling Error vs Time**

- **Time (µs)** vs **Input Noise Current (pA/√Hz)**

**Long-Term Output Settling Error vs Time, $V_S = \pm 5V$**

- **Time (µs)** vs **Output Settling Error (%)**

**8-Lead Plastic DIP**

- **Maximum Power Dissipation** vs **Ambient Temperature**

**20-Lead SOL**

- **Maximum Power Dissipation** vs **Ambient Temperature**

---

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Typical Performance Curves — Contd.

Large Signal Response

\[ AV = +1, \; R_F = 1 \, \text{k}\Omega, \]
\[ R_L = 200\Omega, \; V_S = \pm 15V \]

Large Signal Response

\[ AV = +2, \; R_F = 820, \]
\[ R_L = 200\Omega, \; V_S = \pm 15V \]

Large Signal Response

\[ AV = +10, \; R_F = 750, \; R_G = 82\Omega, \]
\[ R_L = 200\Omega, \; V_S = \pm 15V \]

Large Signal Response

\[ AV = +2, \; R_F = R_G = 750\Omega, \]
\[ R_L = 200\Omega, \; V_S = \pm 15V \]

Burn-In Circuit

Test Circuit

ALL PACKAGES USE THE SAME SCHEMATIC.
An industry standard way of measuring the distortion of a video component (or system) is to measure the amount of differential gain and phase error it introduces. A 100 mV peak to peak sine wave at 3.58 MHz for NTSC (4.3 MHz for PAL), with 0V DC component serves as the reference. The reference signal is added to a DC offset, shifting the sine wave from 0V to 0.7V which is then applied to the device under test (DUT). The output signal from the DUT is compared to the reference signal. The Differential Gain is a measure of the change in amplitude of the sine wave and is measured in percent; The Differential Phase is a measure of the change in the phase of the sine wave and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak differential gain and differential phase errors. The test setup in Figure 1 was used to characterize the EL2030. For higher than NTSC and PAL frequencies, an alternate Differential Gain and Phase measurement can be made using an HP3577A Network Analyser and the setup shown in Figure 2. The frequency response is normalized to gain or phase with 0V DC at the input. From the normalized value a DC offset voltage is introduced and the Differential Gain or Phase is the deviation from the normalized value.

Application Information

Product Description
The EL2030 is a current mode feedback amplifier similar to the industry standard EL2020, but with greatly improved AC characteristics. Most significant among these are the extremely wide bandwidth and very low differential gain and phase. In addition, the EL2030 is fully characterized and tested at ±5V and ±15V supplies.

Power Supply Bypassing/Lead Dressing
It is important to bypass the power supplies of the EL2030 with 0.1 μF ceramic disc capacitors. Although the lead length is not critical, it should not be more than the 1/2 inch from the IC pins. Failure to do this will result in oscillation, and possible destruction of the part. Another important detail is the lead length of the inputs. The inputs should be designed with minimum stray capacitance and short lead lengths to avoid ringing and distortion.

Latch Mode
The EL2030 can be damaged in certain circumstances resulting in catastrophic failure in which destructive supply currents flow in the device. Specifically, an input signal greater than ±5 volts at currents greater than 5 mA is applied to the device when the power supply voltages are zero will result in failure of the device.

In addition, the EL2030 will be destroyed or damaged in the same way for momentary power supply voltage reversals. This could happen, for example, during a power turn on transient, or if the power supply voltages were oscillating and the positive rail were instantaneously negative with respect to the negative rail or vice versa.

Differential Gain and Differential Phase
Composite video signals contain intensity, color, hue, timing and audio information in AM, FM, and Phase Modulation. These video signals pass through many stages during their production, processing, archiving and transmission. It is important that each stage not corrupt these signals to provide a "high fidelity" image to the end viewer.

Video Applications
The video signals that must be transmitted for modest distances are usually amplified by a device such as the EL2030 and carried via coax cable. There are at least two ways to drive cables, single terminated and double terminated.

When driving a cable, it is important to terminate it properly to avoid unwanted signal reflections. Single termination (75Ω to ground at receive end) may be sufficient for less demanding applications. In general, a double terminated cable (75Ω in series at drive end and 75Ω to ground at receive end) is preferred since the impedance match at both ends of the line will absorb signal reflections. However, when double termination is used (a total impedance of 150Ω), the received signal is reduced by half; therefore, the amplifier is usually set at a gain of 2 or higher to compensate for attenuation.
**Video Applications — Contd.**

Video signals are 1V peak-peak in amplitude, from sync tip to peak white. There are 100 IRE (0.714V) of picture (from black to peak white of the transmitted signal) and 40 IRE (0.286V) of sync in a composite video signal (140 IRE = 1V).

For video applications where a gain of two is used (double termination), the output of the video amplifier will be a maximum of 2V peak-peak. With ±5V power supply, the EL2030 output swing of 3.5V is sufficient to satisfy the video output swing requirements. The EL2030 can drive two double terminated coax cables under these conditions. With ±15V supplies, driving four double terminated cables is feasible.

Although the EL2030’s video characteristics (differential gain and phase) are impressive with ±5V supplies at NTSC and PAL frequencies, it can be optimized when the supplies are increased to ±15V, especially at 30 MHz HDTV applications. This is primarily due to a reduction in internal parasitic junction capacitance with increased power supply voltage.

The following table summarizes the behavior of the EL2030 at ±5V and ±15V for NTSC. In addition, 30 MHz HDTV data is included. Refer to the differential gain and phase typical performance curves for more data.

<table>
<thead>
<tr>
<th>±V_s</th>
<th>R_{load}</th>
<th>A_v</th>
<th>ΔGain</th>
<th>ΔPhase</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>15V</td>
<td>75Ω</td>
<td>1</td>
<td>0.02%</td>
<td>0.03°</td>
<td>Single terminated</td>
</tr>
<tr>
<td>15V</td>
<td>150Ω</td>
<td>1</td>
<td>0.02%</td>
<td>0.02°</td>
<td>Double terminated</td>
</tr>
<tr>
<td>5V</td>
<td>150Ω</td>
<td>1</td>
<td>0.05%</td>
<td>0.02°</td>
<td>Double terminated</td>
</tr>
<tr>
<td>15V</td>
<td>75Ω</td>
<td>2</td>
<td>0.02%</td>
<td>0.08°</td>
<td>Single terminated</td>
</tr>
<tr>
<td>15V</td>
<td>150Ω</td>
<td>2</td>
<td>0.01%</td>
<td>0.02°</td>
<td>Double terminated</td>
</tr>
<tr>
<td>5V</td>
<td>150Ω</td>
<td>2</td>
<td>0.03%</td>
<td>0.09°</td>
<td>Double terminated</td>
</tr>
<tr>
<td>15V</td>
<td>150Ω</td>
<td>2</td>
<td>0.05%</td>
<td>0.02°</td>
<td>HDTV, Double terminated</td>
</tr>
</tbody>
</table>

**Equivalent Circuit**
EL2030 Macromodel

* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:  + input  |  - input  |  + Vsupply  |  - Vsupply  |  output
* .subckt M2030  3  2  7  4  6

  * Input Stage
  * e1 10 0 3 0 1.0
    vis 10 9 0V
    h2 9 12 vxx 1.0
    r1 2 11 50
    l1 11 12 48nH
    iinp 3 0 5µA
    iinm 2 0 10µA
    r12 3 0 2Meg
  *
  * Slew Rate Limiting
  * h1 13 0 vis 600
    r2 13 14 1K
    d1 14 0 dclamp
    d2 0 14 dclamp
  *
  * High Frequency Pole
  * e2 30 0 14 0 0.001666666666
    l3 30 17 0.5µH
    c5 17 0 1pF
    r5 17 0 500
  *
  * Transimpedance Stage
  * g1 0 18 17 0 1.0
    rol 18 0 150K
    cdp 18 0 2.8pF
  *
  * Output Stage
  * q1 4 18 19 qp
    q2 7 18 20 qn
    q3 7 19 21 qn
    q4 4 20 22 qp
    r7 21 6 4
    r8 22 6 4
**EL2030 Macromodel — Contd.**

ios1 7 19 2.5mA
ios2 20 4 2.5mA
  *
  * Supply Current
  *
ips 7 4 9mA
  *
  * Error Terms
  *
ivos 0 23 5mA
vxx 23 0 0V
e4 24 3 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
  *
  * Models
  *
.model qn npn (is = 5e−15 bf = 100 tf = 0.1nS)
.model qp pnp (is = 5e−15 bf = 100 tf = 0.1nS)
.model dclamp d(is = 1e−30 ibv = 0.266 bv = 3.7 n = 4)
.ends
EL2030 Macromodel — Contd.
**Features**

- **120 MHz** - 3 dB bandwidth
- Unity-gain stable
- Low supply current
  - $= 5.2$ mA at $V_S = \pm 15V$
- Wide supply range
  - $= \pm 2$V to $\pm 18$V dual-supply
  - $= 2.5V$ to $36V$ single-supply
- High slew rate $= 325 V/\mu s$
- Fast settling $= 80$ ns to 0.1% for a 10V step
- Low differential gain $= 0.04\%$ at $A_V = + 2$, $R_L = 150\Omega$
- Low differential phase $= 0.15^\circ$ at $A_V = + 2$, $R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing
  - $= \pm 13.6V$ with $V_S = \pm 15V$, $R_L = 1000\Omega$
  - $= 3.8V/0.3V$ with $V_S = + 5V$, $R_L = 500\Omega$
- Low cost, enhanced replacement for the AD847 and LM6361

**Applications**

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2044CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2044CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

**General Description**

The EL2044C is a high speed, low power, low cost monolithic operational amplifier built on Elantec’s proprietary complementary bipolar process. The EL2044C is unity-gain stable and features a $325 V/\mu s$ slew rate and $120$ MHz gain-bandwidth product while requiring only $5.2$ mA of supply current.

The power supply operating range of the EL2044C is from $\pm 18V$ down to as little as $\pm 2V$. For single-supply operation, the EL2044C operates from $36V$ down to as little as $2.5V$. The excellent power supply operating range of the EL2044C makes it an obvious choice for applications on a single $+5V$ supply.

The EL2044C also features an extremely wide output voltage swing of $\pm 13.6V$ with $V_S = \pm 15V$ and $R_L = 1000\Omega$. At $\pm 5V$, output voltage swing is a wide $\pm 3.8V$ with $R_L = 500\Omega$ and $\pm 3.2V$ with $R_L = 150\Omega$. Furthermore, for single-supply operation at $+5V$, output voltage swing is an excellent $0.3V$ to $3.8V$ with $R_L = 500\Omega$.

At a gain of $+1$, the EL2044C has a $-3$ dB bandwidth of $120$ MHz with a phase margin of $50^\circ$. It can drive unlimited load capacitance, and because of its conventional voltage-feedback topology, the EL2044C allows the use of reactive or nonlinear elements in its feedback network. This versatility combined with low cost and $75$ mA of output-current drive makes the EL2044C an ideal choice for price-sensitive applications requiring low power and high speed.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: Elantec's Processing, Monolithic Integrated Circuits.

**Connection Diagram**

DIP and SO Package

```
DIP and SO Package

NC 1 8 NC
IN- 2 7 V+
IN+ 5 6 OUT
V- 4 3 NC
```

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### Absolute Maximum Ratings \((T_A = 25°C)\)
- **Supply Voltage** \((V_S)\): ±18V or 36V
- **Peak Output Current** \((I_{OP})\): Short-Circuit Protected
- **Output Short-Circuit Duration** (Note 1): Infinite
- **Input Voltage** \((V_{IN})\): ±Vs
- **Differential Input Voltage** \((dV_{IN})\): ±10V

### Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX15 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

### Test Level
<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
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<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25°C) and QA sample tested at (T_A = 25°C).</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25°C) for information purposes only.</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics \(V_S = \pm 15V, R_L = 1000\,\Omega\), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(V_S = \pm 15V)</td>
<td>25°C</td>
<td>0.5</td>
<td>7.0</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td>13.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>mV</td>
</tr>
<tr>
<td>(TC_{VOS})</td>
<td>Average Offset Voltage Drift</td>
<td>(Note 2)</td>
<td>All</td>
<td>10.0</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu V/^\circ C)</td>
</tr>
<tr>
<td>(I_B)</td>
<td>Input Bias Current</td>
<td>(V_S = \pm 15V)</td>
<td>25°C</td>
<td>2.8</td>
<td>8.2</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5V)</td>
<td>25°C</td>
<td>2.8</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input Offset Current</td>
<td>(V_S = \pm 15V)</td>
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<td>300</td>
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<td>I</td>
<td>nA</td>
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<td></td>
<td>(V_S = \pm 5V)</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>IV</td>
<td>nA</td>
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<td>(Note 2)</td>
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<td>V</td>
<td>(nA/^\circ C)</td>
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<tr>
<td>(A_{VOL})</td>
<td>Open-Loop Gain</td>
<td>(V_S = \pm 15V, V_{OUT} = \pm 10V, R_L = 1000,\Omega)</td>
<td>25°C</td>
<td>800</td>
<td>1500</td>
<td></td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5V, V_{OUT} = \pm 2.5V, R_L = 500,\Omega)</td>
<td>25°C</td>
<td></td>
<td>1200</td>
<td></td>
<td>IV</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5V, V_{OUT} = \pm 2.5V, R_L = 150,\Omega)</td>
<td>25°C</td>
<td></td>
<td>1000</td>
<td></td>
<td>V</td>
<td>V/V</td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td>(V_S = \pm 5V) to (\pm 15V)</td>
<td>25°C</td>
<td>65</td>
<td>80</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>dB</td>
</tr>
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</table>
### DC Electrical Characteristics

**Vs** = ±15V, **R_L** = 1000Ω, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td><strong>V_CM</strong> = ±12V, <strong>V_OUT</strong> = 0V</td>
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<td>70</td>
<td>90</td>
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<td>I</td>
<td>dB</td>
</tr>
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<td></td>
<td></td>
<td><strong>T_MIN, T_MAX</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td></td>
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<td>CMIR</td>
<td>Common-Mode Input Range</td>
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<td>25°C</td>
<td>±14.0</td>
<td>V</td>
<td>V</td>
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<td></td>
<td></td>
<td><strong>Vs</strong> = ±5V</td>
<td>25°C</td>
<td>±4.2</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = +5V</td>
<td>25°C</td>
<td>4.2/0.1</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOUT</td>
<td>Output Voltage Swing</td>
<td><strong>Vs</strong> = ±15V, <strong>R_L</strong> = 1000Ω</td>
<td>25°C</td>
<td>±13.4</td>
<td>±13.6</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>T_MIN, T_MAX</strong></td>
<td></td>
<td>±13.1</td>
<td></td>
<td></td>
<td>IV</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = ±15V, <strong>R_L</strong> = 500Ω</td>
<td>25°C</td>
<td>±12.0</td>
<td>±13.4</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = ±5V, <strong>R_L</strong> = 500Ω</td>
<td>25°C</td>
<td>±3.4</td>
<td>±3.8</td>
<td>IV</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = ±5V, <strong>R_L</strong> = 150Ω</td>
<td>25°C</td>
<td>±3.2</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = +5V, <strong>R_L</strong> = 500Ω</td>
<td>25°C</td>
<td>3.6/0.4</td>
<td>3.8/0.3</td>
<td>I</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td><strong>T_MIN, T_MAX</strong></td>
<td></td>
<td>3.5/0.5</td>
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<td></td>
<td>IV</td>
<td>V</td>
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<tr>
<td>ISC</td>
<td>Output Short Circuit Current</td>
<td></td>
<td>25°C</td>
<td>40</td>
<td>75</td>
<td></td>
<td>I</td>
<td>mA</td>
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<tr>
<td></td>
<td></td>
<td><strong>T_MIN, T_MAX</strong></td>
<td></td>
<td>35</td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
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<tr>
<td>IS</td>
<td>Supply Current</td>
<td><strong>Vs</strong> = ±15V, No Load</td>
<td>25°C</td>
<td>5.2</td>
<td>7</td>
<td>I</td>
<td>I</td>
<td>mA</td>
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<td></td>
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<td><strong>V_MIN, T_MAX</strong></td>
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<td>7.6</td>
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<td>IV</td>
<td>IV</td>
<td>mA</td>
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<td></td>
<td></td>
<td><strong>Vs</strong> = ±5V, No Load</td>
<td>25°C</td>
<td>5.0</td>
<td></td>
<td>V</td>
<td>V</td>
<td>mA</td>
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<td>RIN</td>
<td>Input Resistance</td>
<td>Differential</td>
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<td>150</td>
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<td>V</td>
<td>kΩ</td>
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<td></td>
<td></td>
<td>Common-Mode</td>
<td>25°C</td>
<td>15</td>
<td></td>
<td>V</td>
<td>MΩ</td>
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<tr>
<td>Cap</td>
<td>Input Capacitance</td>
<td><strong>A/V</strong> = +1 @ 10 MHz</td>
<td>25°C</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
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<tr>
<td>ROUT</td>
<td>Output Resistance</td>
<td><strong>A/V</strong> = +1</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td>V</td>
<td>mΩ</td>
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<td>PSOR</td>
<td>Power-Supply Operating Range</td>
<td>Dual-Supply</td>
<td>25°C</td>
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<td>±18.0</td>
<td>V</td>
<td>V</td>
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<td></td>
<td></td>
<td>Single-Supply</td>
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<td>2.5</td>
<td>36.0</td>
<td>V</td>
<td>V</td>
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### Closed-Loop AC Electrical Characteristics

**Vs** = ±15V, **A/V** = +1, **R_L** = 1000Ω unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>BW</td>
<td>−3 dB Bandwidth</td>
<td><strong>Vs</strong> = ±15V, <strong>A/V</strong> = +1</td>
<td>25°C</td>
<td>120</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = ±15V, <strong>A/V</strong> = −1</td>
<td>25°C</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = ±15V, <strong>A/V</strong> = +2</td>
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<td>60</td>
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<td></td>
<td>V</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td><strong>Vs</strong> = ±15V, <strong>A/V</strong> = +5</td>
<td>25°C</td>
<td>12</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
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<td></td>
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<td><strong>Vs</strong> = ±15V, <strong>A/V</strong> = +10</td>
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<td>6</td>
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<td></td>
<td>V</td>
<td>MHz</td>
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<td></td>
<td></td>
<td><strong>Vs</strong> = ±5V</td>
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<td>MHz</td>
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<tr>
<td>GBWP</td>
<td>Gain-Bandwidth Product</td>
<td><strong>Vs</strong> = ±15V</td>
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<td>V</td>
<td>MHz</td>
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<td></td>
<td><strong>Vs</strong> = ±5V</td>
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<td>45</td>
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<td>V</td>
<td>MHz</td>
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<tr>
<td>PM</td>
<td>Phase Margin</td>
<td><strong>R_L</strong> = 1 kΩ, <strong>C_L</strong> = 10 pF</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
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### Closed-Loop AC Electrical Characteristics

\( V_S = \pm 15V, A_V = +1, R_L = 1000\Omega \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>SR</td>
<td>Slew Rate (Note 3)</td>
<td>( V_S = \pm 15V, R_L = 1000\Omega )</td>
<td>25°C</td>
<td>250</td>
<td>325</td>
<td>I</td>
<td>V/\mu s</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, R_L = 500\Omega )</td>
<td>25°C</td>
<td>200</td>
<td></td>
<td>V</td>
<td>V/\mu s</td>
<td></td>
</tr>
<tr>
<td>FPBW</td>
<td>Full-Power Bandwidth (Note 4)</td>
<td>( V_S = \pm 15V )</td>
<td>25°C</td>
<td>4.0</td>
<td>5.2</td>
<td>I</td>
<td>MHz</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>25°C</td>
<td>12.7</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( t_r, t_f )</td>
<td>Rise Time, Fall Time</td>
<td>0.1V Step</td>
<td>25°C</td>
<td>3.0</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
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<tr>
<td>OS</td>
<td>Overshoot</td>
<td>0.1V Step</td>
<td>25°C</td>
<td>20</td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
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<tr>
<td>( t_{PD} )</td>
<td>Propagation Delay</td>
<td>25°C</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
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<tr>
<td>( t_s )</td>
<td>Settling to + 0.1% (( A_V = +1 ))</td>
<td>( V_S = \pm 15V, 10V ) Step</td>
<td>25°C</td>
<td>80</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, 5V ) Step</td>
<td>25°C</td>
<td>60</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td>0.04</td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
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<tr>
<td>dP</td>
<td>Differential Phase (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td>0.15</td>
<td></td>
<td>V</td>
<td>°</td>
<td></td>
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<tr>
<td>eN</td>
<td>Input Noise Voltage</td>
<td>10 kHz</td>
<td>25°C</td>
<td>15.0</td>
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<td>V</td>
<td>nV/\sqrt{Hz}</td>
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<td>iN</td>
<td>Input Noise Current</td>
<td>10 kHz</td>
<td>25°C</td>
<td>1.50</td>
<td></td>
<td>V</td>
<td>pA/\sqrt{Hz}</td>
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<tr>
<td>CI STAB</td>
<td>Load Capacitance Stability</td>
<td>( A_V = +1 )</td>
<td>25°C</td>
<td>Infinite</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 2: Measured from \( T_{MIN} \) to \( T_{MAX} \).

Note 3: Slew rate is measured on rising edge.

Note 4: For \( V_S = \pm 15V, V_{OUT} = 20 \) Vpp. For \( V_S = \pm 5V, V_{OUT} = 5 \) Vpp. Full-power bandwidth is based on slew rate measurement using: \( FPBW = \frac{SR}{2\pi \cdot V_{peak}} \).

Note 5: Video Performance measured at \( V_S = \pm 15V, A_V = +2 \) with 2 times normal video level across \( R_L = 150\Omega \). This corresponds to standard video levels across a back-terminated 75\Omega load. For other values of \( R_L \), see curves.
Typical Performance Curves (TA = 25°C, RL = 1000Ω, AV = +1 unless otherwise specified)

- **Non-Inverting Frequency Response**
- **Inverting Frequency Response**
- **Frequency Response for Various Load Resistances**
- **Open-Loop Gain and Phase vs Frequency**
- **Output Voltage Swing vs Frequency**
- **Equivalent Input Noise**
- **CMRR, PSRR and Closed-Loop Output Resistance vs Frequency**
- **2nd and 3rd Harmonic Distortion vs Frequency**
- **Settling Time vs Output Voltage Change**
- **Supply Current vs Supply Voltage**
- **Common-Mode Input Range vs Supply Voltage**
- **Output Voltage Range vs Supply Voltage**
Typical Performance Curves \((T_A = 25°C, R_L = 1000\Omega, AV = +1 \text{ unless otherwise specified})\) — Contd.
Typical Performance Curves \((T_A = 25^\circ C, R_L = 1000\Omega, A_v = +1\) unless otherwise specified) — Contd.

Short-Circuit Current vs Temperature

Gain-Bandwidth Product vs Load Capacitance

Overshoot vs Load Capacitance

Small-Signal Step Response

Large-Signal Step Response

Differential Gain and Phase vs DC Input Offset at 3.58 MHz

Differential Gain and Phase vs DC Input Offset at 4.43 MHz

Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz

Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz

Differential Gain and Phase vs Number of 8-Pin Plastic DIP Loads at 4.43 MHz

Differential Gain and Phase vs Number of 8-Lead SO Loads at 4.43 MHz

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature

8-Lead SO Maximum Power Dissipation vs Ambient Temperature

Maximum Power Dissipation

Temperature (°C)

Power Dissipation (W)

Number of 150Ω Loads

Temperature (°C)

Power Dissipation (W)

INFINITE HEAT SINK

FREE AIR

NO HEAT SINK

INFINITE HEAT SINK

FREE AIR

NO HEAT SINK

2-95
Simplified Schematic

EL2044C
Low Power/Low Voltage 120 MHz Unity-Gain Stable Operational Amplifier
Applications Information

Product Description
The EL2044C is a low-power wideband monolithic operational amplifier built on Elantec's proprietary high-speed complementary bipolar process. The EL2044C uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2044C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2044C is an excellent choice for applications such as fast log amplifiers.

Single-Supply Operation
The EL2044C has been designed to have a wide input and output voltage range. This design also makes the EL2044C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (RL = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and RL = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2044C still has 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth
The EL2044C has a gain-bandwidth product of 60 MHz while using only 5.2 mA of supply current. For gains greater than 4, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2044C has a −3 dB bandwidth of 120 MHz at a gain of +1, dropping to 60 MHz at a gain of +2. It is important to note that the EL2044C has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2044C in a gain of +1 only exhibits 1.0 dB of peaking with a 1000Ω load.

Video Performance
An industry-standard method of measuring the video distortion of a component such as the EL2044C is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 Vpp (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2044C has been designed as an economical solution for applications requiring low video distortion. It has been thoroughly characterized.
Applications Information — Contd.
for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2044C exhibits dG and dP of only 0.04% and 0.15° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2044C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The output drive capability of the EL2044C allows it to drive up to 2 back-terminated loads with good video performance. For more demanding applications such as greater output drive or better video distortion, a number of alternatives such as the EL2120, EL400, or EL2073 should be considered.

Output Drive Capability
The EL2044C has been designed to drive low impedance loads. It can easily drive 6 VPP into a 150Ω load. This high output drive capability makes the EL2044C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2044C remains a minimum of 35 mA at low temperatures. The EL2044C is current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads
For ease of use, the EL2044C has been designed to drive any capacitive load. However, the EL2044C remains stable by automatically reducing its gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2044C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout
The EL2044C is well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 µF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2044C Macromodel
This macromodel has been developed to assist the user in simulating the EL2044C with surrounding circuitry. It has been developed for the PSPICE simulator (copyrighted by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

- noise
- settling-time
- CMRR
- PSRR
- non-linearities
- temperature effects
- manufacturing variations
EL2044C Macromodel — Contd.

* Connections: + input
  * | | -input
  * | | + Vsupply
  * | | - Vsupply
  * | | output
  *
  .subckt M2044 3 2 7 4 6
  *
  * Input stage
  *
  ie 7 37 1mA
  r6 36 37 800
  r7 38 37 800
  rc1 4 30 850
  rc2 4 39 850
  q1 30 3 36 qp
  q2 39 2 38 qpa
  ediff 33 3 39 30 1.0
  rdiff 33 0 1Meg
  *
  * Compensation Section
  *
  ga 34 33 0 1m
  rh 34 0 2Meg
  ch 34 0 1.3pF
  re 34 40 1K
  cc 40 0 1pF
  *
  * Poles
  *
  ep 41 0 40 0 1
  rpa 41 42 200
  cpa 42 0 1pF
  rpb 42 43 200
  cpb 43 0 1pF
  *
  * Output Stage
  *
  ios1 7 50 1.0mA
  ios2 51 4 1.0mA
  q3 4 43 50 qp
  q4 7 43 51 qn
  q5 7 50 52 qn
  q6 4 51 53 qp
  ros1 52 6 25
  ros2 6 53 25
  *
  * Power Supply Current
  *
  ips 7 4 2.7mA
  *
  * Models
  *
  .model qn npn(is = 800E-18 bf = 200 tf = 0.2nS)
  .model qpa pnp(is = 864E-18 bf = 100 tf = 0.2nS)
  .model qp pnp(is = 800E-18 bf = 125 tf = 0.2nS)
  .ends
EL2044C Macromodel — Contd.

EL2044C Model
Features

- 60 MHz gain-bandwidth product
- Unity-gain stable
- Low supply current (per Amplifier)
  \[ = 5.2 \text{ mA at } V_S = \pm 15 \text{V} \]
- Wide supply range
  \[ = \pm 2 \text{V to } \pm 18 \text{V dual-supply} \]
  \[ = 2.5 \text{V to } 36 \text{V single-supply} \]
- High slew rate \[ = 325 \text{ V/μs} \]
- Fast settling \[ = 80 \text{ ns to } 0.1\% \text{ for a } 10 \text{V step} \]
- Low differential gain \[ = 0.04\% \text{ at } A_V = + 2, R_L = 150\Omega \]
- Low differential phase \[ = 0.15° \text{ at } A_V = + 2, R_L = 150\Omega \]
- Stable with unlimited capacitive load
- Wide output voltage swing
  \[ = \pm 13.6 \text{V with } V_S = \pm 15 \text{V}, \]
  \[ = 3.8V/0.3V \text{ with } V_S = + 5 \text{V}, \]
  \[ R_L = 500\Omega \]
- Low cost, enhanced replacement for the ADB27 and LT1229/LT1230

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

General Description

The EL2244C/EL2444C are dual and quad versions of the popular EL2044C. They are high speed, low power, low cost monolithic operational amplifiers built on Elantec’s proprietary complementary bipolar process. The EL2244C/EL2444C are unity-gain stable and feature a 325 V/μs slew rate and 60 MHz gain-bandwidth product while requiring only 5.2 mA of supply current per amplifier.

The power supply operating range of the EL2244C/EL2444C is from \[ \pm 18 \text{V} \text{ down to as little as } \pm 2 \text{V} \]. For single-supply operation, the EL2244C/EL2444C operate from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2244C/EL2444C makes them an obvious choice for applications on a single +5V or +3V supply.

The EL2244C/EL2444C also feature an extremely wide output voltage swing of \[ \pm 13.6 \text{V with } V_S = \pm 15 \text{V} \text{ and } R_L = 1000\Omega \]. At \[ \pm 5 \text{V} \], output voltage swing is a wide \[ \pm 3.8 \text{V with } R_L = 500\Omega \text{ and } \pm 3.2 \text{V with } R_L = 150\Omega \]. Furthermore, for single-supply operation at \[ + 5 \text{V} \], output voltage swing is an excellent \[ 0.3 \text{V to } 3.8 \text{V with } R_L = 500\Omega \].

At a gain of \[ + 1 \], the EL2244C/EL2444C have a \[ -3 \text{ dB bandwidth of } 120 \text{MHz with a phase margin of } 50° \]. They can drive unlimited load capacitance, and because of their conventional voltage-feedback topology, the EL2244C/EL2444C allow the use of reactive or non-linear elements in their feedback network. This versatility combined with low cost and 75 mA of output-current drive make the EL2244C/EL2444C an ideal choice for price-sensitive applications requiring low power and high speed.

Connection Diagrams

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duals</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2244CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2244CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
<tr>
<td>Quads</td>
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</tr>
<tr>
<td>EL2444CN</td>
<td>-40°C to +85°C</td>
<td>14-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2444CS</td>
<td>-40°C to +85°C</td>
<td>14-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>
## Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Power Dissipation ((P_D))</th>
<th>Operating Temperature Range ((T_A))</th>
<th>Operating Junction Temperature ((T_J))</th>
<th>Storage Temperature ((T_{ST}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ((V_S))</td>
<td>(\pm 18\text{V} \text{ or } 36\text{V})</td>
<td>See Curves</td>
<td>(-40^\circ C \text{ to } +85^\circ C)</td>
<td>(150^\circ C)</td>
<td>(-65^\circ C \text{ to } +150^\circ C)</td>
</tr>
<tr>
<td>Peak Output Current ((I_{OP}))</td>
<td>Short-Circuit Protected</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Short-Circuit Duration ((Note 1))</td>
<td>Infinite</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage ((V_{IN}))</td>
<td>(\pm V_S)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage ((dV_{IN}))</td>
<td>(\pm 10\text{V})</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Important Note

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25^\circ C) and QA sample tested at (T_A = 25^\circ C), (T_{MAX}) and (T_{MIN}) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25^\circ C) for information purposes only.</td>
</tr>
</tbody>
</table>

## DC Electrical Characteristics \(V_S = \pm 15\text{V}, R_L = 1000\text{\Omega}\), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>(V_S = \pm 15\text{V})</td>
<td>25°C</td>
<td>0.5</td>
<td>4.0</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>mV</td>
</tr>
<tr>
<td>TCVOS</td>
<td>Average Offset Voltage Drift</td>
<td>(Note 2)</td>
<td>All</td>
<td>10.0</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu V/\circ C)</td>
</tr>
<tr>
<td>IB</td>
<td>Input Bias Current</td>
<td>(V_S = \pm 15\text{V})</td>
<td>25°C</td>
<td>2.8</td>
<td>8.2</td>
<td>I</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5\text{V})</td>
<td>25°C</td>
<td>2.8</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>IOS</td>
<td>Input Offset Current</td>
<td>(V_S = \pm 15\text{V})</td>
<td>25°C</td>
<td>50</td>
<td>300</td>
<td>I</td>
<td>I</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5\text{V})</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>nA</td>
</tr>
<tr>
<td>TCIOS</td>
<td>Average Offset Current Drift</td>
<td>(Note 2)</td>
<td>All</td>
<td>0.3</td>
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<td></td>
<td>V</td>
<td>nA/\circ C</td>
</tr>
<tr>
<td>AYOL</td>
<td>Open-Loop Gain</td>
<td>(V_S = \pm 15\text{V}, V_{OUT} = \pm 10\text{V}, R_L = 1000\text{\Omega})</td>
<td>25°C</td>
<td>800</td>
<td>1500</td>
<td>I</td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5\text{V}, V_{OUT} = \pm 2.5\text{V}, R_L = 500\text{\Omega})</td>
<td>25°C</td>
<td>1200</td>
<td></td>
<td></td>
<td>V</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5\text{V}, V_{OUT} = \pm 2.5\text{V}, R_L = 500\text{\Omega})</td>
<td>25°C</td>
<td>1000</td>
<td></td>
<td></td>
<td>V</td>
<td>V/V</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>(V_S = \pm 5\text{V to } \pm 15\text{V})</td>
<td>25°C</td>
<td>65</td>
<td>80</td>
<td>I</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>dB</td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics

**V_s = ±15V, R_L = 1000Ω**, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td><strong>CMRR</strong></td>
<td>Common-Mode Rejection Ratio</td>
<td><strong>V_{CM} = ±12V, V_{OUT} = 0V</strong></td>
<td>25°C</td>
<td>70</td>
<td>90</td>
<td>I</td>
<td>IV</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>T_{MIN}, T_{MAX}</strong></td>
<td>70</td>
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<tr>
<td><strong>CMIR</strong></td>
<td>Common-Mode Input Range</td>
<td><strong>V_s = ±15V</strong></td>
<td>25°C</td>
<td>±14.0</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>V_s = ±5V</strong></td>
<td>25°C</td>
<td>±4.2</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td><strong>V_s = +5V</strong></td>
<td>25°C</td>
<td>4.2/0.1</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td><strong>V_{OUT}</strong></td>
<td>Output Voltage Swing</td>
<td><strong>V_s = ±15V, R_L = 1000Ω</strong></td>
<td>25°C</td>
<td>±13.4</td>
<td>±13.6</td>
<td>I</td>
<td>V</td>
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<td><strong>T_{MIN}, T_{MAX}</strong></td>
<td>±13.1</td>
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<td><strong>V_s = ±15V, R_L = 500Ω</strong></td>
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<td>±12.0</td>
<td>±13.4</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>V_s = ±5V, R_L = 500Ω</strong></td>
<td>25°C</td>
<td>±3.4</td>
<td>±3.8</td>
<td>IV</td>
<td>V</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td><strong>V_s = ±5V, R_L = 150Ω</strong></td>
<td>25°C</td>
<td>±3.2</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
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<tr>
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<td></td>
<td><strong>V_s = +5V, R_L = 500Ω</strong></td>
<td>25°C</td>
<td>3.6/0.4</td>
<td>3.8/0.3</td>
<td>I</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td><strong>T_{MIN}, T_{MAX}</strong></td>
<td>3.5/0.5</td>
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<td><strong>I_{SC}</strong></td>
<td>Output Short Circuit Current</td>
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<td>25°C</td>
<td>40</td>
<td>75</td>
<td>I</td>
<td>mA</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td><strong>T_{MIN}, T_{MAX}</strong></td>
<td>35</td>
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<tr>
<td><strong>I_s</strong></td>
<td>Supply Current (Per Amplifier)</td>
<td><strong>V_s = ±15V, No Load</strong></td>
<td>25°C</td>
<td>5.2</td>
<td>7</td>
<td>I</td>
<td>mA</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td><strong>T_{MIN}</strong></td>
<td>7.6</td>
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<td><strong>T_{MAX}</strong></td>
<td>7.6</td>
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<tr>
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<td></td>
<td><strong>V_s = ±5V, No Load</strong></td>
<td>25°C</td>
<td>5.0</td>
<td></td>
<td>V</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td><strong>R_{IN}</strong></td>
<td>Input Resistance</td>
<td>Differential</td>
<td>25°C</td>
<td>150</td>
<td></td>
<td>V</td>
<td>kΩ</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Common-Mode</td>
<td>25°C</td>
<td>15</td>
<td></td>
<td>V</td>
<td>MΩ</td>
<td></td>
</tr>
<tr>
<td><strong>C_{IN}</strong></td>
<td>Input Capacitance</td>
<td><strong>A_v = +1@ 10 MHz</strong></td>
<td>25°C</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td><strong>R_{OUT}</strong></td>
<td>Output Resistance</td>
<td><strong>A_v = +1</strong></td>
<td>25°C</td>
<td>50</td>
<td></td>
<td>V</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td><strong>PSOR</strong></td>
<td>Power-Supply Operating Range</td>
<td>Dual-Supply</td>
<td>25°C</td>
<td>±2.0</td>
<td>±18.0</td>
<td>V</td>
<td>V</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Single-Supply</td>
<td>25°C</td>
<td>2.5</td>
<td>36.0</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### Closed-Loop AC Electrical Characteristics

**V_s = ±15V, A_v = +1, R_L = 1000Ω** unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>−3 dB Bandwidth (V_{OUT} = 0.4 V_{pp})</td>
<td><strong>V_s = ±15V, A_v = +1</strong></td>
<td>25°C</td>
<td>120</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>V_s = ±15V, A_v = −1</strong></td>
<td>25°C</td>
<td>60</td>
<td></td>
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<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>V_s = ±15V, A_v = +2</strong></td>
<td>25°C</td>
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<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
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<td><strong>V_s = ±15V, A_v = +5</strong></td>
<td>25°C</td>
<td>12</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
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<tr>
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<td><strong>V_s = ±15V, A_v = +10</strong></td>
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<td>6</td>
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<td>V</td>
<td>MHz</td>
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<td><strong>V_s = ±5V, A_v = +1</strong></td>
<td>25°C</td>
<td>80</td>
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<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain-Bandwidth Product</td>
<td><strong>V_s = ±15V</strong></td>
<td>25°C</td>
<td>60</td>
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<td></td>
<td>V</td>
<td>MHz</td>
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<td></td>
<td><strong>V_s = ±5V</strong></td>
<td>25°C</td>
<td>45</td>
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<td>V</td>
<td>MHz</td>
</tr>
</tbody>
</table>
### Closed-Loop AC Electrical Characteristics

\( V_S = \pm 15V, A_V = +1, R_L = 1000\Omega \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PM</strong></td>
<td>Phase Margin</td>
<td>( R_L = 1 , \text{k}\Omega, C_L = 10 , \text{pF} )</td>
<td>25°C</td>
<td>50</td>
<td>V</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td><strong>CS</strong></td>
<td>Channel Separation</td>
<td>( f = 5 , \text{MHz} )</td>
<td>25°C</td>
<td>85</td>
<td>V</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>SR</strong></td>
<td>Slew Rate (Note 3)</td>
<td>( V_S = \pm 15V, R_L = 1000\Omega )</td>
<td>25°C</td>
<td>250</td>
<td>325</td>
<td>I</td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, R_L = 500\Omega )</td>
<td>25°C</td>
<td></td>
<td>200</td>
<td>V</td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td><strong>FPBW</strong></td>
<td>Full-Power Bandwidth</td>
<td>(Note 4)</td>
<td>25°C</td>
<td>4.0</td>
<td>5.2</td>
<td>I</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 15V )</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>t_{r}, t_{f}</strong></td>
<td>Rise Time, Fall Time</td>
<td>0.1V Step</td>
<td>25°C</td>
<td>3.0</td>
<td>V</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td><strong>OS</strong></td>
<td>Overshoot</td>
<td>0.1V Step</td>
<td>25°C</td>
<td>20</td>
<td>V</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td><strong>t_{PD}</strong></td>
<td>Propagation Delay</td>
<td></td>
<td>25°C</td>
<td>2.5</td>
<td>V</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td><strong>t_s</strong></td>
<td>Settling to +0.1% (Av = +1)</td>
<td>( V_S = \pm 15V, 10V \text{Step} )</td>
<td>25°C</td>
<td>80</td>
<td>V</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, 5V \text{Step} )</td>
<td>25°C</td>
<td>60</td>
<td>V</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>dG</strong></td>
<td>Differential Gain (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td>0.04</td>
<td>V</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td><strong>dP</strong></td>
<td>Differential Phase (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td>0.15</td>
<td>V</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td><strong>eN</strong></td>
<td>Input Noise Voltage</td>
<td>10 kHz</td>
<td>25°C</td>
<td>15.0</td>
<td>V</td>
<td></td>
<td></td>
<td>nV/\sqrt{Hz}</td>
</tr>
<tr>
<td><strong>iN</strong></td>
<td>Input Noise Current</td>
<td>10 kHz</td>
<td>25°C</td>
<td>1.50</td>
<td>V</td>
<td></td>
<td></td>
<td>pA/\sqrt{Hz}</td>
</tr>
<tr>
<td><strong>Cl STAB</strong></td>
<td>Load Capacitance Stability</td>
<td></td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

**Note 2:** Measured from \( T_{MIN} \) to \( T_{MAX} \).

**Note 3:** Slew rate is measured on rising edge.

**Note 4:** For \( V_S = \pm 15V, V_{OUT} = 20 \, \text{Vpp} \). For \( V_S = \pm 5V, V_{OUT} = 5 \, \text{Vpp} \). Full-power bandwidth is based on slew rate measurement using: \( \text{FPBW} = \frac{\text{SR}}{2\pi \times V_{\text{peak}}} \).

**Note 5:** Video Performance measured at \( V_S = \pm 15V, A_V = +2 \) with 2 times normal video level across \( R_L = 150\Omega \). This corresponds to standard video levels across a back-terminated 75\Omega load. For other values of \( R_L \), see curves.
Typical Performance Curves \((T_A = 25^\circ C, R_L = 1000\Omega, A_V = +1\) unless otherwise specified)
Typical Performance Curves (TA = 25°C, RL = 1000Ω, AV = +1 unless otherwise specified) — Contd.
Typical Performance Curves (TA = 25°C, RL = 1000Ω, AV = +1 unless otherwise specified) — Contd.
Typical Performance Curves ($T_A = 25^\circ\text{C}$, $R_L = 1000\Omega$, $A_V = +1$ unless otherwise specified) — Contd.

### 14-Pin Plastic DIP

**Maximum Power Dissipation vs Ambient Temperature**

- $T_J \text{ MAX} = 150^\circ\text{C}$
- $R_{JA} = 70^\circ\text{C/W}$

### 14-Lead SO

**Maximum Power Dissipation vs Ambient Temperature**

- $T_J \text{ MAX} = 150^\circ\text{C}$
- $R_{JA} = 110^\circ\text{C/W}$

### Channel Separation vs Frequency

- $V_{in} = 0\text{dBm}$
- $R_1 = 1\text{K\Omega}$
- $V_{out} = \pm15V$

#### Simplified Schematic (Per Amplifier)

![Simplified Schematic](image)

#### Burn-In Circuit (Per Amplifier)

![Burn-In Circuit](image)

All Packages Use the Same Schematic
Applications Information

Product Description
The EL2244C/EL2444C are low-power wideband monolithic operational amplifiers built on Elantec's proprietary high-speed complementary bipolar process. The EL2244C/EL2444C use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2244C/EL2444C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2244C/EL2444C are an excellent choice for applications such as fast log amplifiers.

Power Dissipation
With the wide power supply range and large output drive capability of the EL2244C/EL2444C, it is possible to exceed the 150°C maximum junction temperatures under certain load and powersupply conditions. It is therefore important to calculate the maximum junction temperature (TJmax) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2244C/EL2444C to remain in the safe operating area. These parameters are related as follows:

\[ TJ_{\text{max}} = T_{\text{max}} + (\theta_{JA} \times (PD_{\text{max total}})) \]

where PD_{max total} is the sum of the maximum power dissipation of each amplifier in the package (PD_{max}). PD_{max} for each amplifier can be calculated as follows:

\[ PD_{\text{max}} = (2V_S \times IS_{\text{max}} + (V_S - V_{\text{outmax}}) \times (V_{\text{outmax}}/RL)) \]

where:
\[ T_{\text{max}} = \text{Maximum Ambient Temperature} \]
\[ \theta_{JA} = \text{Thermal Resistance of the Package} \]
\[ PD_{\text{max}} = \text{Maximum Power Dissipation of 1 Amplifier} \]
\[ V_S = \text{Supply Voltage} \]

\[ IS_{\text{max}} = \text{Maximum Supply Current of 1 Amplifier} \]
\[ V_{\text{outmax}} = \text{Maximum Output Voltage Swing of the Application} \]
\[ RL = \text{Load Resistance} \]

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that TJ_{\text{max}} = 150°C, T_{\text{max}} = 75°C, IS_{\text{max}} = 7.6 mA, and the package \( \theta_{JAS} \) are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the maximum average value (over duty-cycle) of V_{\text{outmax}} is 1.4V, and RL = 150Ω, giving the results seen in Table 1.

Table 1

<table>
<thead>
<tr>
<th>Duals</th>
<th>Package</th>
<th>( \theta_{JA} )</th>
<th>Max PDiss @ T_{\text{max}}</th>
<th>Max V_S</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2244CN</td>
<td>PDIP8</td>
<td>95°C/C/W</td>
<td>0.789W @ 75°C</td>
<td>±16.6V</td>
</tr>
<tr>
<td>EL2244CS</td>
<td>SO8</td>
<td>150°C/C/W</td>
<td>0.500W @ 75°C</td>
<td>±10.7V</td>
</tr>
<tr>
<td>QUADS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2444CN</td>
<td>PDIP14</td>
<td>70°C/C/W</td>
<td>1.071W @ 75°C</td>
<td>±11.5V</td>
</tr>
<tr>
<td>EL2444CS</td>
<td>SO14</td>
<td>110°C/C/W</td>
<td>0.682W @ 75°C</td>
<td>±7.5V</td>
</tr>
</tbody>
</table>

Single-Supply Operation
The EL2244C/EL2444C have been designed to have a wide input and output voltage range. This design also makes the EL2244C/EL2444C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (RL = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and RL = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2244C/EL2444C still have 1V of output swing.

Gain-Bandwidth Product and the \(-3 \text{ dB Bandwidth}\)
The EL2244C/EL2444C have a gain-bandwidth product of 60 MHz while using only 5.2 mA of supply current per amplifier. For gains greater...
Applications Information — Contd.

than 4, their closed-loop $-3\,\text{dB}$ bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifiers’ transfer function contribute to even higher closed loop bandwidths. For example, the EL2244C/EL2444C have a $-3\,\text{dB}$ bandwidth of 120 MHz at a gain of +1, dropping to 60 MHz at a gain of +2. It is important to note that the EL2244C/EL2444C have been designed so that this “extra” bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2244C/EL2444C in a gain of +1 only exhibit 1.0 dB of peaking with a 10000, load.

Video Performance

An industry-standard method of measuring the video distortion of components such as the EL2244C/EL2444C is to measure the amount of differential gain ($dG$) and differential phase ($dP$) that they introduce. To make these measurements, a 0.286 Vpp (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75$\Omega$ in series at the drive end, and 75$\Omega$ to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2244C/EL2444C have been designed as an economical solution for applications requiring low video distortion. They have been thoroughly characterized for video performance in the topology described above, and the results have been included as typical $dG$ and $dP$ specifications and as typical performance curves. In a gain of +2, driving 150$\Omega$, with standard video test levels at the input, the EL2244C/EL2444C exhibit $dG$ and $dP$ of only 0.04% and 0.15° at NTSC and PAL. Because $dG$ and $dP$ can vary with different DC offsets, the video performance of the EL2244C/EL2444C has been characterized over the entire DC offset range from $-0.714V$ to $+0.714V$. For more information, refer to the curves of $dG$ and $dP$ vs DC Input Offset.

Output Drive Capability

The EL2244C/EL2444C have been designed to drive low impedance loads. They can easily drive 6 Vpp into a 150$\Omega$ load. This high output drive capability makes the EL2244C/EL2444C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2244C/EL2444C remains a minimum of 35 mA at low temperatures. The EL2244C/EL2444C are current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2244C/EL2444C have been designed to drive any capacitive load. However, the EL2244C/EL2444C remain stable by automatically reducing their gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor ($Rs$). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2244C/EL2444C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2244C/EL2444C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum
Applications Information — Contd.

The performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2244C/EL2444C Macromodel

This macromodel has been developed to assist the user in simulating the EL2244C/EL2444C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

- noise
- settling-time
- CMRR
- PSRR
- non-linearities
- temperature effects
- manufacturing variations

* Connections: + input
  * | | -input
  * | | +Vs
  * | | -Vs
  * | | output

.* Subckt M2244 3 2 7 4 6
* * Input stage
* *
* ie 7 37 1mA
* r6 36 37 800
* r7 38 37 800
* rc1 4 30 850
* rc2 4 39 850
* q1 30 3 36 qp
* q2 39 2 38 qpa
* ediff 33 0 39 30 1.0
* rdiff 33 0 1Meg
* * Compensation Section
* *
* ga 34 33 0 1m
* rh 34 0 2Meg
* ch 34 0 1.3pF
* rc 34 40 1K
* cc 40 0 1pF
* *

* Poles
* *
* ep 41 0 40 0 1
* rpa 41 42 200
* cpa 42 0 1pF
* rpb 42 43 200
* cpb 43 0 1pF
* * * Output Stage
* *
* ips 7 4 2.7mA
* * * Models
* *
* .model qn npn(is = 800E−18 bf = 200 tf = 0.2nS)
* .model qpa npn(is = 864E−18 bf = 100 tf = 0.2nS)
* .model qp npn(is = 800E−18 bf = 125 tf = 0.2nS)
* .ends

2-111
EL2244C/EL2444C Macromodel — Contd.

EL2244C/EL2444C Model
**Features**

- 100 MHz gain-bandwidth product
- Gain-of-2 stable
- Low supply current
  - $5.2 \text{ mA at } V_S = \pm 15V$
- Wide supply range
  - $\pm 2V$ to $\pm 18V$ dual-supply
  - $2.5V$ to $36V$ single-supply
- High slew rate $= 275 V/\mu s$
- Fast settling $= 80 \text{ ns to } 0.1\%$ for a $10V$ step
- Low differential gain $= 0.02\%$ at $A_V = +2, R_L = 150\Omega$
- Low differential phase $= 0.07^\circ$ at $A_V = +2, R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing
  - $\pm 13.6V$ with $V_S = \pm 15V$
  - $3.8V/0.3V$ with $V_S = +5V$
  - $R_L = 500\Omega$

**Applications**

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

**General Description**

The EL2045C is a high speed, low power, low cost monolithic operational amplifier built on Elantec's proprietary complementary bipolar process. The EL2045C is gain-of-2 stable and features a $275 V/\mu s$ slew rate and 100 MHz gain-bandwidth product while requiring only 5.2 mA of supply current.

The power supply operating range of the EL2045C is from $\pm 18V$ down to as little as $\pm 2V$. For single-supply operation, the EL2045C operates from $36V$ down to as little as 2.5V. The excellent power supply operating range of the EL2045C makes it an obvious choice for applications on a single $+5V$ or $+3V$ supply.

The EL2045C also features an extremely wide output voltage swing of $\pm 13.6V$ with $V_S = \pm 15V$ and $R_L = 1000\Omega$. At $+5V$, output voltage swing is a wide $\pm 3.8V$ with $R_L = 500\Omega$ and $\pm 3.2V$ with $R_L = 150\Omega$. Furthermore, for single-supply operation at $+5V$, output voltage swing is an excellent $0.3V$ to $3.8V$ with $R_L = 500\Omega$.

At a gain of $+2$, the EL2045C has a $-3$ dB bandwidth of 100 MHz with a phase margin of $50^\circ$. It can drive unlimited load capacitance, and because of its conventional voltage-feedback topology, the EL2045C allows the use of reactive or nonlinear elements in its feedback network. This versatility combined with low cost and 75 mA of output-current drive makes the EL2045C an ideal choice for price-sensitive applications requiring low power and high speed.

**Connection Diagram**

![Connection Diagram](image-url)
**Absolute Maximum Ratings** \( (T_A = 25°C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>( V_S = \pm 15V )</td>
<td>25°C</td>
<td>0.5</td>
<td>7.0</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Average Offset</td>
<td>( V_S = \pm 15V )</td>
<td>All</td>
<td>10.0</td>
<td></td>
<td></td>
<td>V</td>
<td>( \mu V/°C )</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Current</td>
<td>( V_S = \pm 15V )</td>
<td>25°C</td>
<td>2.8</td>
<td>8.2</td>
<td></td>
<td>I</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_B )</td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>25°C</td>
<td>2.8</td>
<td></td>
<td></td>
<td>V</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td>( V_S = \pm 15V )</td>
<td>25°C</td>
<td>50</td>
<td>300</td>
<td></td>
<td>I</td>
<td>nA</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>nA</td>
</tr>
<tr>
<td>( T_{ClO} )</td>
<td>Average Offset Current Drift</td>
<td>( V_S = \pm 15V )</td>
<td>All</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>( nA/°C )</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Open-Loop Gain</td>
<td>( V_S = \pm 15V, V_{OUT} = \pm 10V, R_L = 1000\Omega )</td>
<td>25°C</td>
<td>1500</td>
<td>3000</td>
<td></td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td></td>
<td>( V_S = \pm 5V, V_{OUT} = \pm 2.5V, R_L = 500\Omega )</td>
<td>25°C</td>
<td>1500</td>
<td></td>
<td></td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td></td>
<td>( V_S = \pm 5V, V_{OUT} = \pm 2.5V, R_L = 150\Omega )</td>
<td>25°C</td>
<td>1500</td>
<td></td>
<td></td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td>( PSRR )</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S = \pm 5V )</td>
<td>25°C</td>
<td>65</td>
<td>85</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
</tbody>
</table>

**Important Note:** All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LT677 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

**DC Electrical Characteristics** \( V_S = \pm 15V, R_L = 1000\Omega \), unless otherwise specified.
### DC Electrical Characteristics

**$V_s = \pm 15V, R_L = 1000\Omega$, unless otherwise specified — Contd.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CMRR</strong></td>
<td>Common-Mode Rejection Ratio</td>
<td>$V_{CM} = \pm 12V, V_{OUT} = 0V$</td>
<td>$25^\circ C$</td>
<td>70</td>
<td>95</td>
<td>I</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>CMIR</strong></td>
<td>Common-Mode Input Range</td>
<td>$V_s = \pm 15V$</td>
<td>$25^\circ C$</td>
<td>±14.0</td>
<td>±14.0</td>
<td>I</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = \pm 5V$</td>
<td>$25^\circ C$</td>
<td>±4.2</td>
<td>±4.2</td>
<td>I</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +5V$</td>
<td>$25^\circ C$</td>
<td>4.2/0.1</td>
<td>4.2/0.1</td>
<td>V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>V_{OUT}</strong></td>
<td>Output Swing</td>
<td>$V_s = \pm 15V, R_L = 1000\Omega$</td>
<td>$25^\circ C$</td>
<td>±13.4</td>
<td>±13.6</td>
<td>I</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = \pm 15V, R_L = 500\Omega$</td>
<td>$25^\circ C$</td>
<td>±12.0</td>
<td>±13.4</td>
<td>I</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = \pm 5V, R_L = 500\Omega$</td>
<td>$25^\circ C$</td>
<td>±3.4</td>
<td>±3.8</td>
<td>IV</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = \pm 5V, R_L = 150\Omega$</td>
<td>$25^\circ C$</td>
<td>±3.2</td>
<td>±3.2</td>
<td>V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +5V, R_L = 500\Omega$</td>
<td>$25^\circ C$</td>
<td>3.6/0.4</td>
<td>3.8/0.3</td>
<td>I</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>±13.1</td>
<td></td>
<td></td>
<td>III</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>I_{SC}</strong></td>
<td>Output Short Circuit Current</td>
<td>$V_s = \pm 15V, No Load$</td>
<td>$25^\circ C$</td>
<td>40</td>
<td>75</td>
<td>I</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
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<td></td>
<td></td>
<td>III</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>I_S</strong></td>
<td>Supply Current</td>
<td>$V_s = \pm 15V, No Load$</td>
<td>$25^\circ C$</td>
<td>5.2</td>
<td>7</td>
<td>I</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>7.6</td>
<td></td>
<td></td>
<td>III</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>R_{IN}</strong></td>
<td>Input Resistance</td>
<td>Differential</td>
<td>$25^\circ C$</td>
<td>150</td>
<td>V</td>
<td>kΩ</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Common-Mode</td>
<td>$25^\circ C$</td>
<td>15</td>
<td>V</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>C_{IN}</strong></td>
<td>Input Capacitance</td>
<td>$A_V = +2@10 MHz$</td>
<td>$25^\circ C$</td>
<td>1.0</td>
<td>V</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>R_{OUT}</strong></td>
<td>Output Resistance</td>
<td>$A_V = +2$</td>
<td>$25^\circ C$</td>
<td>50</td>
<td>V</td>
<td>mΩ</td>
<td></td>
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<tr>
<td><strong>PSOR</strong></td>
<td>Power-Supply Operating Range</td>
<td>Dual-Supply</td>
<td>$25^\circ C$</td>
<td>±2.0</td>
<td>±18.0</td>
<td>V</td>
<td></td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td>Single-Supply</td>
<td>$25^\circ C$</td>
<td>2.5</td>
<td>36.0</td>
<td>V</td>
<td></td>
<td>V</td>
</tr>
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</table>

### Closed-Loop AC Electrical Characteristics

**$V_s = \pm 15V, A_V = +2, R_f = R_e = 1 k\Omega, C_f = 3 pF, R_L = 1000\Omega$ unless otherwise specified**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td><strong>BW</strong></td>
<td>−3 dB Bandwidth</td>
<td>$V_s = \pm 15V, A_V = +2$</td>
<td>$25^\circ C$</td>
<td>100</td>
<td>V</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td>$V_s = \pm 15V, A_V = -1$</td>
<td>$25^\circ C$</td>
<td>75</td>
<td>V</td>
<td>MHz</td>
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<td></td>
<td></td>
<td>$V_s = \pm 15V, A_V = +5$</td>
<td>$25^\circ C$</td>
<td>20</td>
<td>V</td>
<td>MHz</td>
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<td></td>
<td></td>
<td>$V_s = \pm 15V, A_V = +10$</td>
<td>$25^\circ C$</td>
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<td>V</td>
<td>MHz</td>
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<td></td>
<td></td>
<td>$V_s = \pm 15V, A_V = +20$</td>
<td>$25^\circ C$</td>
<td>5</td>
<td>V</td>
<td>MHz</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>$V_s = \pm 5V, A_V = +2$</td>
<td>$25^\circ C$</td>
<td>75</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
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<tr>
<td><strong>GBWP</strong></td>
<td>Gain-Bandwidth Product</td>
<td>$V_s = \pm 15V$</td>
<td>$25^\circ C$</td>
<td>100</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = \pm 5V$</td>
<td>$25^\circ C$</td>
<td>75</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
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<tr>
<td><strong>PM</strong></td>
<td>Phase Margin</td>
<td>$R_L = 1 k\Omega, C_L = 10 pF$</td>
<td>$25^\circ C$</td>
<td>50</td>
<td>V</td>
<td></td>
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</table>
**Closed-Loop AC Electrical Characteristics**

When $V_S = \pm 15V, A_V = +2, R_f = R_g = 1 k\Omega, C_f = 3 \text{ pF}, R_L = 1000\Omega$, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>SR</td>
<td>Slew Rate (Note 3)</td>
<td>$V_S = \pm 15V, R_L = 1000\Omega$</td>
<td>25°C</td>
<td>200</td>
<td>275</td>
<td></td>
<td>I</td>
<td>V/\mu s</td>
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<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V, R_L = 500\Omega$</td>
<td>25°C</td>
<td>200</td>
<td></td>
<td></td>
<td>V</td>
<td>V/\mu s</td>
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<tr>
<td>FPBW</td>
<td>Full-Power Bandwidth (Note 4)</td>
<td>$V_S = \pm 15V$</td>
<td>25°C</td>
<td>3.2</td>
<td>4.4</td>
<td></td>
<td>I</td>
<td>MHz</td>
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<td></td>
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<td>$V_S = \pm 5V$</td>
<td>25°C</td>
<td></td>
<td>12.7</td>
<td></td>
<td>V</td>
<td>MHz</td>
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<tr>
<td>$t_r, t_f$</td>
<td>Rise Time, Fall Time</td>
<td>0.1V Output Step</td>
<td>25°C</td>
<td></td>
<td>3.0</td>
<td></td>
<td>V</td>
<td>ns</td>
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<tr>
<td>OS</td>
<td>Overshoot</td>
<td>0.1V Output Step</td>
<td>25°C</td>
<td></td>
<td>20</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay</td>
<td>25°C</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
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<tr>
<td>$t_s$</td>
<td>Settling to +0.1% (A_V = +2)</td>
<td>$V_S = \pm 15V, 10V Step$</td>
<td>25°C</td>
<td></td>
<td>80</td>
<td></td>
<td>V</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V, 5V Step$</td>
<td>25°C</td>
<td></td>
<td>60</td>
<td></td>
<td>V</td>
<td>ns</td>
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<tr>
<td>dG</td>
<td>Differential Gain (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td></td>
<td>0.02</td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td></td>
<td>0.07</td>
<td></td>
<td>V</td>
<td>°</td>
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<td>cN</td>
<td>Input Noise Voltage</td>
<td>10 kHz</td>
<td>25°C</td>
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<td>15.0</td>
<td></td>
<td>V</td>
<td>nV/\sqrt{Hz}</td>
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<tr>
<td>iN</td>
<td>Input Noise Current</td>
<td>10 kHz</td>
<td>25°C</td>
<td></td>
<td>1.50</td>
<td></td>
<td>V</td>
<td>pA/\sqrt{Hz}</td>
</tr>
<tr>
<td>CI STAB</td>
<td>Load Capacitance Stability</td>
<td>$A_V = +2$</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>Infinite</td>
<td>V</td>
</tr>
</tbody>
</table>

**Notes:**

- **Note 1:** A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
- **Note 2:** Measured from $T_{MIN}$ to $T_{MAX}$.
- **Note 3:** Slew rate is measured on rising edge.
- **Note 4:** For $V_S = \pm 15V, V_{OUT} = 20 \text{ Vpp}$. For $V_S = \pm 5V, V_{OUT} = 5 \text{ Vpp}$. Full-power bandwidth is based on slew rate measurement using: $FPBW = SR/(2\pi \times \text{Vpeak})$.
- **Note 5:** Video Performance measured at $V_S = \pm 15V, A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of $R_L$, see curves.

**EL2045C Test Circuit**

![EL2045C Test Circuit](image)
Typical Performance Curves

(TA = 25°C, RF = 1 kΩ, CF = 3 pF, RL = 1000Ω, AV = +2 unless otherwise specified)

Non-Inverting Frequency Response

Inverting Frequency Response

Frequency Response for Various Load Resistances

Open-Loop Gain and Phase vs Frequency

Output Voltage Swing vs Frequency

CMRR, PSRR and Closed-Loop Output Resistance vs Frequency

2nd and 3rd Harmonic Distortion vs Frequency

Equivalent Input Noise

Settling Time vs Output Voltage Change

Supply Current vs Supply Voltage

Common-Mode Input Range vs Supply Voltage

Output Voltage Range vs Supply Voltage
Typical Performance Curves
(T_A = 25°C, R_f = 1 kΩ, C_f = 3 pF, R_L = 10000, A_V = +2 unless otherwise specified) — Contd.
Typical Performance Curves

(T_a = 25°C, R_I = 1 kΩ, C_I = 3 pF, R_L = 1000Ω, A_v = +2 unless otherwise specified) — Contd.

**Short-Circuit Current vs Temperature**

**Gain-Bandwidth Product vs Load Capacitance**

**Overshoot vs Load Capacitance**

**Small-Signal Step Response**

**Large-Signal Step Response**

**Differential Gain and Phase vs DC Input Offset at 3.58 MHz**

**DC Input Voltage (V) vs Number of 150Ω Loads at 4.43 MHz**

**Differential Gain and Phase vs DC Input Offset at 4.43 MHz**

**Number vs 150Ω Loads 8-Lead SO Maximum Power Dissipation vs Ambient Temperature**

**Maximum Power Dissipation vs Ambient Temperature**
Simplified Schematic
Applications Information

Product Description
The EL2045C is a low-power wideband, gain-of-2 stable monolithic operational amplifier built on Elantec's proprietary high-speed complementary bipolar process. The EL2045C uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2045C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2045C is an excellent choice for applications such as fast log amplifiers.

Single-Supply Operation
The EL2045C has been designed to have a wide input and output voltage range. This design also makes the EL2045C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground ($R_L = 500 \Omega$), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and $R_L = 500 \Omega$. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2045C still has 1V of output swing.

Gain-Bandwidth Product and the $-3 \, \text{dB}$ Bandwidth
The EL2045C has a gain-bandwidth product of 100 MHz while using only 5.2 mA of supply current. For gains greater than 4, its closed-loop $-3 \, \text{dB}$ bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2045C has a $-3 \, \text{dB}$ bandwidth of 100 MHz at a gain of +2, dropping to 20 MHz at a gain of +5. It is important to note that the EL2045C has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2045C in a gain of +2 only exhibits 1.0 dB of peaking with a 1000$\Omega$ load.

Video Performance
An industry-standard method of measuring the video distortion of a component such as the EL2045C is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 Vpp (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75$\Omega$ in series at the drive end, and 75$\Omega$ to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2045C has been designed as an economical solution for applications requiring low video distortion. It has been thoroughly characterized.
Applications Information — Contd.

for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2045C exhibits dG and dP of only 0.02% and 0.07° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2045C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The output drive capability of the EL2045C allows it to drive up to 2 back-terminated loads with good video performance. For more demanding applications such as greater output drive or better video distortion, a number of alternatives such as the EL2120, EL400, or EL2074 should be considered.

Output Drive Capability

The EL2045C has been designed to drive low impedance loads. It can easily drive 6 Vpp into a 150Ω load. This high output drive capability makes the EL2045C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2045C remains a minimum of 35 mA at low temperatures. The EL2045C is current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2045C has been designed to drive any capacitive load. However, the EL2045C remains stable by automatically reducing its gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2045C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2045C is well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2045C Macromodel

This macromodel has been developed to assist the user in simulating the EL2045C with surrounding circuitry. It has been developed for the PSPICE simulator (copyswriten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model resistive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

- noise
- settling-time
- CMRR
- PSRR
- non-linearities
- temperature effects
- manufacturing variations
**EL2045C Macromodel — Contd.**

* Connections:  
*  
* Connections:  
+ input  
- input  
+ Vsupply  
- Vsupply  
output  

* Models  

.model qn npn(is = 800E-18 bf = 200 tf = 0.2nS)  
.model qpa pnp(is = 864E-18 bf = 100 tf = 0.2nS)  
.model qp pnp(is = 800E-18 bf = 125 tf = 0.2nS)  
.ends  

* Subckt M2045  
3 2 7 4 6  

* Input stage  
*  
ie 7 37 0.9mA  
r6 36 37 400  
r7 38 37 400  
rc1 4 30 850  
rc2 4 39 850  
q1 30 3 36 qp  
q2 39 2 38 qpa  
ediff 33 39 30 1.0  
rdiff 33 0 1Meg  

* Compensation Section  
*  
ga 0 34 33 0 1m  
rh 34 0 2Meg  
ch 34 0 1.5pF  
rc 34 40 1K  
cc 40 0 1pF  

* Poles  
*  
ep 41 0 40 0 1  
rpa 41 42 200  
cpa 42 0 2pF  
rpb 42 43 200  
cpb 43 0 2pF  

* Output Stage  
*  
ios1 7 50 1.0mA  
ios2 51 4 1.0mA  
q3 4 43 50 qp  
q4 7 43 51 qn  
q5 7 50 52 qn  
q6 4 51 53 qp  
ros1 52 6 25  
ros2 6 53 25  

* Power Supply Current  

ips 7 4 2.7mA  

*  

2-123
EL2045C Macromodel — Contd.

EL2045C Model
Features

- 100 MHz gain-bandwidth product
- Gain-of-2 stable
- Low supply current (per Amplifier)
  \[ I_{ss} = 5.2 \, mA \] at \( V_S = \pm 15V \)
- Wide supply range
  \[ = \pm 2V \rightarrow \pm 18V \] dual-supply
  \[ = 2.5V \rightarrow 36V \text{ single-supply} \]
- High slew rate = 275 V/\mu s
- Fast settling = 80 ns to 0.1% for a 10 V step
- Low differential gain = 0.02% at \( A_V = +2, R_L = 150\Omega \)
- Low differential phase = 0.07° at \( A_V = +2, R_L = 150\Omega \)
- Stable with unlimited capacitive load
- Wide output voltage swing
  \[ = \pm 13.6V \text{ with } V_S = \pm 15V, R_L = 1000\Omega \]
  \[ = 3.8V/0.3V \text{ with } V_S = +5V, R_L = 5000\Omega \]

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

General Description

The EL2245C/EL2445C are dual and quad versions of the popular EL2045C. They are high speed, low power, low cost monolithic operational amplifiers built on Elantec’s proprietary complementary bipolar process. The EL2245C/EL2445C are unity-gain stable and feature a 275 V/\mu s slew rate and 100 MHz gain-bandwidth product while requiring only 5.2 mA of supply current per amplifier.

The power supply operating range of the EL2245C/EL2445C is from \( \pm 18V \) down to as little as \( \pm 2V \). For single-supply operation, the EL2245C/EL2445C operate from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2245C/EL2445C makes them an obvious choice for applications on a single +5V or +3V supply.

The EL2245C/EL2445C also feature an extremely wide output voltage swing of \( \pm 13.6V \) with \( V_S = \pm 15V \) and \( R_L = 1000\Omega \). At \( \pm 5V \), output voltage swing is a wide \( \pm 3.8V \) with \( R_L = 500\Omega \) and \( \pm 3.2V \) with \( R_L = 150\Omega \). Furthermore, for single-supply operation at \( +5V \), output voltage swing is an excellent 0.3V to 3.8V with \( R_L = 500\Omega \).

At a gain of +2, the EL2245C/EL2445C have a -3 dB bandwidth of 100 MHz with a phase margin of 50°. They can drive unlimited load capacitance, and because of their conventional voltage-feedback topology, the EL2245C/EL2445C allow the use of reactive or non-linear elements in their feedback network. This versatility combined with low cost and 75 mA of output-current drive make the EL2245C/EL2445C an ideal choice for price-sensitive applications requiring low power and high speed.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document, QRA-1: Elantec’s Processing, Monolithic Integrated Circuits.

Ordering Information

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<th>Temp. Range</th>
<th>Package</th>
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</tr>
</thead>
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<td>Duals</td>
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<td></td>
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</tr>
<tr>
<td>EL2245CN</td>
<td>0°C to +75°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2245CS</td>
<td>0°C to +75°C</td>
<td>8-Lead SO</td>
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<td>Quads</td>
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<tr>
<td>EL2445CN</td>
<td>0°C to +75°C</td>
<td>14-Pin P-DIP</td>
<td>MDP0031</td>
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<tr>
<td>EL2445CS</td>
<td>0°C to +75°C</td>
<td>14-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagrams
### Absolute Maximum Ratings \( (T_A = 25^\circ\text{C}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Power Dissipation ( (P_D) )</th>
<th>Operating Temperature Range ( (T_A) )</th>
<th>Operating Junction Temperature ( (T_J) )</th>
<th>Storage Temperature ( (T_{ST}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ( (V_S) )</td>
<td>( \pm 18\text{V} ) or ( 36\text{V} )</td>
<td>See Curves</td>
<td>( 0^\circ\text{C} ) to ( +75^\circ\text{C} )</td>
<td>150^\circ\text{C}</td>
<td>-65^\circ\text{C} to +150^\circ\text{C}</td>
</tr>
<tr>
<td>Peak Output Current ( (I_{OP}) )</td>
<td>Short-Circuit Protected</td>
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<tr>
<td>Output Short-Circuit Duration ( (Note 1) )</td>
<td>Infinite</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage ( (V_{IN}) )</td>
<td>( \pm V_S )</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage ( (dV_{IN}) )</td>
<td>( \pm 10\text{V} )</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

### Test Levels

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at ( T_A = 25^\circ\text{C} ) and QA sample tested at ( T_A = 25^\circ\text{C} ), ( T_{MAX} ) and ( T_{MIN} ) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at ( T_A = 25^\circ\text{C} ) for information purposes only.</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics \( V_S = \pm 15\text{V}, R_L = 1000\Omega \), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>( V_S = \pm 15\text{V} )</td>
<td>25^\circ\text{C}</td>
<td>0.5</td>
<td>4.0</td>
<td>6.0</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Average Offset Voltage Drift</td>
<td>( V_S = \pm V_S )</td>
<td>25^\circ\text{C}</td>
<td>10.0</td>
<td>9.2</td>
<td>10.0</td>
<td>III</td>
<td>( \mu\text{V}^\circ\text{C} )</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>( V_S = \pm 15\text{V} )</td>
<td>25^\circ\text{C}</td>
<td>8.2</td>
<td>9.2</td>
<td>10.0</td>
<td>V</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5\text{V} )</td>
<td>25^\circ\text{C}</td>
<td>2.8</td>
<td>2.8</td>
<td>3.0</td>
<td>V</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td>( V_S = \pm 15\text{V} )</td>
<td>25^\circ\text{C}</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>I</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5\text{V} )</td>
<td>25^\circ\text{C}</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>III</td>
<td>nA</td>
</tr>
<tr>
<td>( TCI_{OS} )</td>
<td>Average Offset Current Drift</td>
<td>( V_S = \pm 15\text{V} )</td>
<td>25^\circ\text{C}</td>
<td>0.3</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
<td>( \text{nA}^\circ\text{C} )</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Open-Loop Gain</td>
<td>( V_S = \pm 15\text{V}, V_{OUT} = \pm 10\text{V}, R_L = 1000\Omega )</td>
<td>25^\circ\text{C}</td>
<td>1500</td>
<td>3000</td>
<td>3000</td>
<td>I</td>
<td>( V/V )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5\text{V}, V_{OUT} = \pm 2.5\text{V}, R_L = 500\Omega )</td>
<td>25^\circ\text{C}</td>
<td>2500</td>
<td>2500</td>
<td>2500</td>
<td>V</td>
<td>( V/V )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5\text{V}, V_{OUT} = \pm 2.5\text{V}, R_L = 150\Omega )</td>
<td>25^\circ\text{C}</td>
<td>1750</td>
<td>1750</td>
<td>1750</td>
<td>V</td>
<td>( V/V )</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S = \pm 5\text{V} ) to ( \pm 15\text{V} )</td>
<td>25^\circ\text{C}</td>
<td>65</td>
<td>80</td>
<td>60</td>
<td>III</td>
<td>dB</td>
</tr>
</tbody>
</table>

2-126
### DC Electrical Characteristics $V_S = \pm 15V, R_L = 1000\Omega$, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>$V_{CM} = \pm 12V, V_{OUT} = 0V$</td>
<td>25°C</td>
<td>70</td>
<td>90</td>
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<td>III</td>
<td>dB</td>
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<tr>
<td>CMIR</td>
<td>Common-Mode Input Range</td>
<td>$V_S = \pm 15V$</td>
<td>25°C</td>
<td>±14.0</td>
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<td></td>
<td>V</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V$</td>
<td>25°C</td>
<td>±4.2</td>
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<td></td>
<td>V</td>
<td>V</td>
</tr>
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<td></td>
<td></td>
<td>$V_S = +5V$</td>
<td>25°C</td>
<td>4.2/0.1</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing</td>
<td></td>
<td>$V_S = \pm 15V, R_L = 1000\Omega$</td>
<td>25°C</td>
<td>±13.4</td>
<td>±13.6</td>
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<tr>
<td>$I_{SC}$</td>
<td>Output Short Circuit Current</td>
<td></td>
<td>25°C</td>
<td>40</td>
<td>75</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current (Per Amplifier)</td>
<td>$V_S = \pm 15V, No Load$</td>
<td>25°C</td>
<td>5.2</td>
<td>7</td>
<td>I</td>
<td>III</td>
<td>mA</td>
</tr>
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<tr>
<td>$R_{IN}$</td>
<td>Input Resistance</td>
<td></td>
<td>25°C</td>
<td>150</td>
<td></td>
<td></td>
<td>V</td>
<td>kΩ</td>
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<td>$C_{IN}$</td>
<td>Input Capacitance</td>
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<td>25°C</td>
<td>15</td>
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<td></td>
<td>V</td>
<td>MΩ</td>
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<tr>
<td>$R_{OUT}$</td>
<td>Output Resistance</td>
<td></td>
<td>25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>mΩ</td>
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<tr>
<td>$PS_{OR}$</td>
<td>Power-Supply Operating Range</td>
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<td>V</td>
<td>V</td>
</tr>
</tbody>
</table>

### Closed-Loop AC Electrical Characteristics $V_S = \pm 15V, A_V = +1, R_L = 1000\Omega$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>−3 dB Bandwidth</td>
<td>$V_S = \pm 15V, A_V = +2$</td>
<td>25°C</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
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<tr>
<td></td>
<td>(V_{OUT} = 0.4 V_{pp})</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V, A_V = -1$</td>
<td>25°C</td>
<td>75</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V, A_V = +5$</td>
<td>25°C</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V, A_V = +10$</td>
<td>25°C</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V, A_V = +20$</td>
<td>25°C</td>
<td>5</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V, A_V = +2$</td>
<td>25°C</td>
<td>75</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain-Bandwidth Product</td>
<td>$V_S = \pm 15V$</td>
<td>25°C</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V$</td>
<td>25°C</td>
<td>75</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
</tbody>
</table>
Closed-Loop AC Electrical Characteristics

\( V_S = \pm 15V, A_V = +2, R_L = 1000\Omega \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM</td>
<td>Phase Margin</td>
<td>( R_L = 1 \text{ k}\Omega, C_L = 10 \text{ pF} )</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>°</td>
</tr>
<tr>
<td>CS</td>
<td>Channel Separation</td>
<td>( f = 5 \text{ MHz} )</td>
<td>25°C</td>
<td>85</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (Note 3)</td>
<td>( V_S = \pm 15V, R_L = 1000\Omega )</td>
<td>25°C</td>
<td>200</td>
<td>275</td>
<td></td>
<td>I</td>
<td>V/\mu s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, R_L = 500\Omega )</td>
<td>25°C</td>
<td>200</td>
<td></td>
<td></td>
<td>V</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>FPBW</td>
<td>Full-Power Bandwidth (Note 4)</td>
<td>( V_S = \pm 15V )</td>
<td>25°C</td>
<td>3.2</td>
<td>4.4</td>
<td></td>
<td>I</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>25°C</td>
<td>12.7</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>( t_r, t_f )</td>
<td>Rise Time, Fall Time</td>
<td>0.1V Step</td>
<td>25°C</td>
<td>3.0</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>0.1V Step</td>
<td>25°C</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>( t_{PD} )</td>
<td>Propagation Delay</td>
<td>0.1V Step</td>
<td>25°C</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( t_s )</td>
<td>Settling to +0.1% (( A_V = +1 ))</td>
<td>( V_S = \pm 15V, 10V \text{ Step} )</td>
<td>25°C</td>
<td>80</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, 5V \text{ Step} )</td>
<td>25°C</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td>0.02</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase (Note 5)</td>
<td>NTSC/PAL</td>
<td>25°C</td>
<td>0.07</td>
<td></td>
<td></td>
<td>V</td>
<td>°</td>
</tr>
<tr>
<td>( eN )</td>
<td>Input Noise Voltage</td>
<td>10 kHz</td>
<td>25°C</td>
<td>15.0</td>
<td></td>
<td></td>
<td>V</td>
<td>nV/\sqrt{\text{Hz}}</td>
</tr>
<tr>
<td>( iN )</td>
<td>Input Noise Current</td>
<td>10 kHz</td>
<td>25°C</td>
<td>1.50</td>
<td></td>
<td></td>
<td>V</td>
<td>pA/\sqrt{\text{Hz}}</td>
</tr>
<tr>
<td>CI STAB</td>
<td>Load Capacitance Stability</td>
<td>( A_V = +1 )</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
</tbody>
</table>

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: Measured from \( T_{\text{MIN}} \) to \( T_{\text{MAX}} \).
Note 3: Slew rate is measured on rising edge.
Note 4: For \( V_S = \pm 15V \), \( V_{\text{OUT}} = 20 \text{ V}_{\text{pp}} \). For \( V_S = \pm 5V \), \( V_{\text{OUT}} = 5 \text{ V}_{\text{pp}} \). Full-power bandwidth is based on slew rate measurement using: \( \text{FPBW} = \frac{\text{SR}}{2\pi \times V_{\text{peak}}} \).
Note 5: Video Performance measured at \( V_S = \pm 15V, A_V = +2 \) with 2 times normal video level across \( R_L = 150\Omega \). This corresponds to standard video levels across a back-terminated 75\Omega load. For other values of \( R_L \), see curves.

**EL2245C/EL2445C Test Circuit**

![Test Circuit Diagram](image)
Typical Performance Curves

(T_A = 25°C, R_F = 1 kΩ, C_P = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified)

Non-Inverting Frequency Response

Inverting Frequency Response

Frequency Response for Various Load Resistances

Open-Loop Gain and Phase vs Frequency

Output Voltage Swing vs Frequency

2nd and 3rd Harmonic Distortion vs Frequency

Settling Time vs Output Voltage Change

CMRR, PSRR and Closed-Loop Output Resistance vs Frequency

Equivalent Input Noise

Supply Voltage vs Supply Voltage

Common-Mode Input Range vs Supply Voltage

Output Voltage Range vs Supply Voltage

Typical Performance Curves

(T_A = 25°C, R_F = 1 kΩ, C_P = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified)
Typical Performance Curves
(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 10000, A_V = +2 unless otherwise specified) — Contd.

- Gain-Bandwidth Product vs Supply Voltage
- Open-Loop Gain vs Supply Voltage
- Slew-Rate vs Supply Voltage

- Bias and Offset Current vs Input Common-Mode Voltage
- Open-Loop Gain vs Load Resistance
- Voltage Swing vs Load Resistance

- Offset Voltage vs Temperature
- Bias and Offset Current vs Temperature
- Supply Current vs Temperature

- Gain-Bandwidth Product vs Temperature
- Open-Loop Gain PSRR and CMRR vs Temperature
- Slew Rate vs Temperature
Typical Performance Curves

(T_A = 25°C, R_P = 1 kΩ, C_P = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified) — Contd.

- Short-Circuit Current vs Temperature
- Gain-Bandwidth Product vs Load Capacitance
- Overshoot vs Load Capacitance
- Small-Signal Step Response
- Large-Signal Step Response
- Differential Gain and Phase vs DC Input Offset at 3.58 MHz
- Differential Gain and Phase vs DC Input Offset at 4.43 MHz
- Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz
- 8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature
- 8-Lead SO Maximum Power Dissipation vs Ambient Temperature
Typical Performance Curves
(T<sub>A</sub> = 25°C, R<sub>F</sub> = 1 kΩ, C<sub>F</sub> = 3 pF, R<sub>L</sub> = 1000Ω, A<sub>V</sub> = +1 unless otherwise specified) — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

14-Lead SO
Maximum Power Dissipation vs Ambient Temperature

Channel Separation vs Frequency

Simplified Schematic (Per Amplifier)

Burn-In Circuit (Per Amplifier)

All Packages Use the Same Schematic
Applications Information

Product Description
The EL2245C/EL2445C are dual and quad low-power wideband monolithic operational amplifiers built on Elantec’s proprietary high-speed complementary bipolar process. The EL2245C/EL2445C use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2245C/EL2445C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2245C/EL2445C are an excellent choice for applications such as fast log amplifiers.

Power Dissipation
With the wide power supply range and large output drive capability of the EL2245C/EL2445C, it is possible to exceed the 150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature \(T_{J_{\text{max}})} for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2245C/EL2445C to remain in the safe operating area. These parameters are related as follows:

\[
T_{J_{\text{max}}} = T_{\text{max}} + (\theta_{JA} \times (\text{PDmax}_{\text{total}}))
\]

where PDmax_{total} is the sum of the maximum power dissipation of each amplifier in the package (PDmax). PDmax for each amplifier can be calculated as follows:

\[
\text{PDmax} = (2 \times V_{S} \times I_{S_{\text{max}}} + (V_{S} - V_{\text{out}_{\text{max}}}) \times (V_{\text{out}_{\text{max}}}/R_{L}))
\]

where:

\(T_{\text{max}}\) = Maximum Ambient Temperature
\(\theta_{JA}\) = Thermal Resistance of the Package
PDmax = Maximum Power Dissipation of 1 Amplifier
\(V_{S}\) = Supply Voltage

\(I_{S_{\text{max}}}\) = Maximum Supply Current of 1 Amplifier
\(V_{\text{out}_{\text{max}}}\) = Maximum Output Voltage Swing of the Application
\(R_{L}\) = Load Resistance

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that \(T_{J_{\text{max}}} = 150°C\), \(T_{\text{max}} = 75°C\), \(I_{S_{\text{max}}} = 7.6\) mA, and the package \(\theta_{JA}\)s are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the maximum average value (over duty-cycle) of \(V_{\text{out}_{\text{max}}}\) is 1.4V, and \(R_{L} = 150Ω\), giving the results seen in Table 1.

Table 1

<table>
<thead>
<tr>
<th></th>
<th>Package</th>
<th>(\theta_{JA})</th>
<th>Max PDiss @ (T_{\text{max}})</th>
<th>Max (V_{S})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duals</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2245CN</td>
<td>PDIP8</td>
<td>95°C/W</td>
<td>0.789W @ 75°C</td>
<td>±16.6V</td>
</tr>
<tr>
<td>EL2245CS</td>
<td>SO8</td>
<td>150°C/W</td>
<td>0.500W @ 75°C</td>
<td>±10.7V</td>
</tr>
<tr>
<td>QUADS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2445CN</td>
<td>PDIP14</td>
<td>70°C/W</td>
<td>1.071W @ 75°C</td>
<td>±11.5V</td>
</tr>
<tr>
<td>EL2445CS</td>
<td>SO14</td>
<td>110°C/W</td>
<td>0.682W @ 75°C</td>
<td>±7.5V</td>
</tr>
</tbody>
</table>

Single-Supply Operation
The EL2245C/EL2445C have been designed to have a wide input and output voltage range. This design also makes the EL2245C/EL2445C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground \(R_{L} = 500Ω\), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and \(R_{L} = 500Ω\). This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2245C/EL2445C still have 1V of output swing.

Gain-Bandwidth Product and the 3 dB Bandwidth
The EL2245C/EL2445C have a gain-bandwidth product of 100 MHz while using only 5.2 mA of supply current per amplifier. For gains greater
Applications Information — Contd.

than 4, their closed-loop \( -3 \) dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifiers’ transfer function contribute to even higher closed loop bandwidths. For example, the EL2245C/EL2445C have a \( -3 \) dB bandwidth of 100 MHz at a gain of +2, dropping to 20 MHz at a gain of +5. It is important to note that the EL2245C/EL2445C have been designed so that this “extra” bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2245C/EL2445C in a gain of +2 only exhibit 1.0 dB of peaking with a 1000\( \Omega \) load.

Video Performance

An industry-standard method of measuring the video distortion of components such as the EL2245C/EL2445C is to measure the amount of differential gain (\( dG \)) and differential phase (\( dP \)) that they introduce. To make these measurements, a 0.286 \( V_{pp} \) (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75\( \Omega \) in series at the drive end, and 75\( \Omega \) to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2245C/EL2445C have been designed as an economical solution for applications requiring low video distortion. They have been thoroughly characterized for video performance in the topology described above, and the results have been included as typical \( dG \) and \( dP \) specifications and as typical performance curves. In a gain of +2, driving 150\( \Omega \), with standard video test levels at the input, the EL2245C/EL2445C exhibit \( dG \) and \( dP \) of only 0.02% and 0.07° at NTSC and PAL. Because \( dG \) and \( dP \) can vary with different DC offsets, the video performance of the EL2245C/EL2445C has been characterized over the entire DC offset range from \(-0.714V \) to \(+0.714V \). For more information, refer to the curves of \( dG \) and \( dP \) vs DC Input Offset.

Output Drive Capability

The EL2245C/EL2445C have been designed to drive low impedance loads. They can easily drive 6 \( V_{pp} \) into a 150\( \Omega \) load. This high output drive capability makes the EL2245C/EL2445C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2245C/EL2445C remains a minimum of 35 mA at low temperatures. The EL2245C/EL2445C are current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2245C/EL2445C have been designed to drive any capacitive load. However, the EL2245C/EL2445C remain stable by automatically reducing their gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (\( R_s \)). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2245C/EL2445C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2245C/EL2445C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum
Applications Information — Contd.

Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2245C/EL2445C Macromodel

This macromodel has been developed to assist the user in simulating the EL2245C/EL2445C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

- noise
- settling-time
- CMRR
- temperature effects
- PSRR
- non-linearities
- manufacturing variations
- noise
- settling-time
- CMRR
- temperature effects
- PSRR

* Poles
  * ep 41 0 40 0 1
  * rpa 41 42 200
  * cpa 42 0 1pF
  * rpb 42 43 200
  * cpb 43 0 1pF
  *
  * Output Stage
  *
  * ios1 7 50 1.0mA
  * ios2 51 4 1.0mA
  * q3 4 43 50 qp
  * q4 7 43 51 qn
  * q5 7 50 52 qn
  * q6 4 51 53 qp
  * ros1 52 6 25
  * ros2 6 53 25
  *
  * Power Supply Current
  *
  * ips 7 4 2.7mA
  *
  * Models
  *
  * .model qn npn(is = 800E-18 bf = 200 tf = 0.2nS)
  * .model qpa npn(is = 864E-18 bf = 100 tf = 0.2nS)
  * .model qp npn(is = 800E-18 bf = 125 tf = 0.2nS)
  .ends

* Connections: +input | -input | +Vsupply | -Vsupply | output
* 3 2 7 4 6

* Input stage
* ie 7 37 1mA
rch 36 37 400
r7 38 37 400
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
* ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.3pF
rc 34 40 1K
cc 40 0 1pF
*
EL2245C/EL2445C Macromodel — Contd.

EL2245C/EL2445C Model
**Features**

- 200 MHz $-3$ dB bandwidth, $A_v = 2$
- Disable/enable
- 12 ns settling to 0.05%
- $V_S = \pm 5V \pm 15 mA$
- Low distortion: HD2, HD3 @ $-60$ dBc at 20 MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- $\pm 1$ to $\pm 8$ closed-loop gain range
- Low cost

**Applications**

- Video gain block
- Video distribution
- HDTV amplifier
- Analog multiplexing (using disable)
- Power-down mode (using disable)
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

**General Description**

The EL2070 is a wide bandwidth, fast settling monolithic amplifier incorporating a disable/enable feature. Built using an advanced complementary bipolar process, this amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of $\pm 1$ to $\pm 8$, the EL2070 has a 200 MHz $-3$ dB bandwidth ($A_v = +2$), and 12 ns settling to 0.05% while consuming only 15 mA of supply current. Furthermore, the fast disable/enable times of 200 ns/100 ns allow rapid analog multiplexing.

The EL2070 is an obvious high-performance solution for video distribution and line-driving applications, especially when its disable feature can be used for fast analog multiplexing. Furthermore, the low 15 mA supply current, and the very low 5 mA of supply current when disabled suggest use in systems where power is critical. With differential gain/phase of 0.02%/0.01°, guaranteed video specifications, and a minimum 50 mA output drive, performance in these areas is assured.

The EL2070’s settling to 0.05% in 12 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200 MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL2070, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document, QRA-1: *Elantec’s Processing, Monolithic Integrated Circuits.*

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2070CN</td>
<td>$-40^\circ C$ to $+85^\circ C$</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2070CS</td>
<td>$-40^\circ C$ to $+85^\circ C$</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

**Connection Diagram**

DIP and SO Package

OFFSET ADJUST 1 8 DISABLE
IN 2 7 V+
IN+ 3 6 OUT
V 4 5 NC

Top View

Manufactured under U.S. Patent No. 4,893,091

December 1995 Rev E
Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Supply Voltage ((V_S))</td>
<td>±7V</td>
</tr>
<tr>
<td>Output Current</td>
<td>±7V</td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>±Vs</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±Vs</td>
</tr>
<tr>
<td>Disable Input Voltage</td>
<td>+Vs, -1V</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>(\theta_J = 95^\circ C/W) P-DIP</td>
</tr>
<tr>
<td></td>
<td>(\theta_J = 175^\circ C/W) SO-8</td>
</tr>
<tr>
<td>Applied Output Voltage</td>
<td>(Disabled) (±V_S)</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>See Curves</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>EL2070C</td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>300°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-60°C to +150°C</td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Open Loop DC Electrical Characteristics \(V_S = ±5V, R_L = 100\Omega\) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td></td>
<td>25°C</td>
<td>2</td>
<td>5.5</td>
<td>I</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(T_{MIN})</td>
<td>8.2</td>
<td>III</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(T_{MAX})</td>
<td>9.0</td>
<td>III</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>(d(V_{OS})/dT)</td>
<td>Average Offset Voltage Drift</td>
<td>(Note 1)</td>
<td>All</td>
<td>10.0</td>
<td>40.0</td>
<td>IV</td>
<td></td>
<td>(\mu V/^\circ C)</td>
</tr>
<tr>
<td>(+I_{IN})</td>
<td>+ Input Current</td>
<td></td>
<td>25°C, (T_{MAX})</td>
<td>10</td>
<td>25.0</td>
<td>II</td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(T_{MIN})</td>
<td>36.0</td>
<td>III</td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(d(+I_{IN})/dT)</td>
<td>Average + Input Current Drift</td>
<td>(Note 1)</td>
<td>All</td>
<td>50.0</td>
<td>200.0</td>
<td>IV</td>
<td></td>
<td>(nA/^\circ C)</td>
</tr>
<tr>
<td>(-I_{IN})</td>
<td>- Input Current</td>
<td></td>
<td>25.0°C</td>
<td>10</td>
<td>30</td>
<td>I</td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td>46</td>
<td>III</td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(d(-I_{IN})/dT)</td>
<td>Average - Input Current Drift</td>
<td>(Note 1)</td>
<td>All</td>
<td>50.0</td>
<td>200.0</td>
<td>IV</td>
<td></td>
<td>(nA/^\circ C)</td>
</tr>
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### Open Loop DC Electrical Characteristics — Contd.

\( V_S = \pm 5V, R_L = 100\Omega \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>All</td>
<td>45.0</td>
<td>50.0</td>
<td></td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>All</td>
<td>40.0</td>
<td>50.0</td>
<td></td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current—Quiescent</td>
<td>No Load</td>
<td>All</td>
<td>16.0</td>
<td>20.0</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{SOFF} )</td>
<td>Supply Current—Disabled</td>
<td>(Note 2)</td>
<td>All</td>
<td>4.0</td>
<td>7.0</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td>( +R_{IN} )</td>
<td>+ Input Resistance</td>
<td>25°C, ( T_{MAX} )</td>
<td>100.0</td>
<td>200.0</td>
<td></td>
<td>II</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td>All</td>
<td>0.5</td>
<td>2.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>pF</td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>Output Impedance (DC)</td>
<td>All</td>
<td>0.1</td>
<td>0.2</td>
<td></td>
<td></td>
<td>IV</td>
<td>Ω</td>
</tr>
<tr>
<td>( R_{OUTD} )</td>
<td>Output Resistance (DC)</td>
<td>Disabled</td>
<td>All</td>
<td>100.0</td>
<td>200.0</td>
<td></td>
<td>IV</td>
<td>kΩ</td>
</tr>
<tr>
<td>( C_{OUTD} )</td>
<td>Output Capacitance (DC)</td>
<td>Disabled</td>
<td>All</td>
<td>0.5</td>
<td>2.0</td>
<td></td>
<td>IV</td>
<td>pF</td>
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<tr>
<td>CMIR</td>
<td>Common-Mode Input Range</td>
<td>(Note 3)</td>
<td>25°C, ( T_{MAX} )</td>
<td>2.0</td>
<td>2.1</td>
<td></td>
<td>IV</td>
<td>V</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output Current</td>
<td>25°C, ( T_{MAX} )</td>
<td>50.0</td>
<td>70.0</td>
<td></td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Voltage Swing</td>
<td>No Load</td>
<td>All</td>
<td>3.3</td>
<td>3.5</td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OUTL} )</td>
<td>Output Voltage Swing</td>
<td>100Ω</td>
<td>25°C</td>
<td>3.0</td>
<td>3.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( -ICMR )</td>
<td>Input Current Common Mode Rejection</td>
<td>25°C</td>
<td>8.0</td>
<td>33.0</td>
<td></td>
<td>I</td>
<td>( \mu A/V )</td>
<td></td>
</tr>
<tr>
<td>( +IPSR )</td>
<td>+ Input Current Power Supply Rejection</td>
<td>25°C</td>
<td>1.0</td>
<td>3.6</td>
<td></td>
<td>I</td>
<td>( \mu A/V )</td>
<td></td>
</tr>
<tr>
<td>( -IPSR )</td>
<td>— Input Current Power Supply Rejection</td>
<td>25°C</td>
<td>20</td>
<td>24</td>
<td></td>
<td>I</td>
<td>( \mu A/V )</td>
<td></td>
</tr>
<tr>
<td>( R_{OL} )</td>
<td>Transimpedance</td>
<td>25°C</td>
<td>30.0</td>
<td>125.0</td>
<td></td>
<td>II</td>
<td>V/( \mu A )</td>
<td></td>
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<tr>
<td>( I_{LOGIC} )</td>
<td>Pin 8 Current @ 0V</td>
<td>All</td>
<td>0.8</td>
<td>1.2</td>
<td></td>
<td>II</td>
<td>mA</td>
<td></td>
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<tr>
<td>( V_{DIS} )</td>
<td>Maximum Pin 8 V to Disable</td>
<td>All</td>
<td>0.5</td>
<td></td>
<td></td>
<td>II</td>
<td>V</td>
<td></td>
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<tr>
<td>( V_{EN} )</td>
<td>Minimum Pin 8 V to Enable</td>
<td>All</td>
<td>3.5</td>
<td></td>
<td></td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{DIS} )</td>
<td>Minimum Pin 8 I to Disable</td>
<td>All</td>
<td>350.0</td>
<td></td>
<td></td>
<td>II</td>
<td>( \mu A )</td>
<td></td>
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<tr>
<td>( I_{EN} )</td>
<td>Maximum Pin 8 I to Enable</td>
<td>All</td>
<td>60.0</td>
<td></td>
<td></td>
<td>II</td>
<td>( \mu A )</td>
<td></td>
</tr>
</tbody>
</table>
## Closed-Loop AC Electrical Characteristics

\( V_S = \pm 5V, R_F = 250\Omega, A_V = +2, R_L = 100\Omega \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td><strong>FREQUENCY RESPONSE</strong></td>
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<td>SSBW</td>
<td>-3 dB Bandwidth ((V_{OUT} &lt; 0.5 \text{ Vpp}))</td>
<td></td>
<td>25°C</td>
<td>150.0</td>
<td>200.0</td>
<td>V</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
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<td>( T_{\text{MIN}} )</td>
<td>150.0</td>
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<td>V</td>
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<tr>
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<td>( T_{\text{MAX}} )</td>
<td>120.0</td>
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<td>V</td>
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<tr>
<td>LSBW</td>
<td>-3 dB Bandwidth ((V_{OUT} &lt; 5.0 \text{ Vpp}))</td>
<td>( A_V = +5 )</td>
<td>All</td>
<td>35.0</td>
<td>50.0</td>
<td></td>
<td>IV</td>
<td>MHz</td>
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<td><strong>GAIN FLATNESS</strong></td>
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<td>GFPL</td>
<td>Peaking ( V_{OUT} &lt; 0.5 \text{ Vpp} )</td>
<td>&lt;40 MHz</td>
<td>25°C</td>
<td>0.0</td>
<td>0.3</td>
<td>V</td>
<td>dB</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{\text{MIN}}, T_{\text{MAX}} )</td>
<td>0.4</td>
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<td>V</td>
<td>dB</td>
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<td>GFPH</td>
<td>Peaking ( V_{OUT} &lt; 0.5 \text{ Vpp} )</td>
<td>&gt;40 MHz</td>
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<td>GFR</td>
<td>Rolloff ( V_{OUT} &lt; 0.5 \text{ Vpp} )</td>
<td>&lt;75 MHz</td>
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<td>0.6</td>
<td>1.0</td>
<td>V</td>
<td>dB</td>
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<td>( T_{\text{MIN}}, T_{\text{MAX}} )</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td>dB</td>
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<td>( T_{\text{MAX}} )</td>
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<td>LPD</td>
<td>Linear Phase Deviation ( V_{OUT} &lt; 0.5 \text{ Vpp} )</td>
<td>&lt;75 MHz</td>
<td>25°C, ( T_{\text{MIN}} )</td>
<td>0.2</td>
<td>1.0</td>
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<td>*</td>
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<td></td>
<td></td>
<td></td>
<td>( T_{\text{MAX}} )</td>
<td>1.2</td>
<td></td>
<td>IV</td>
<td>*</td>
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<td><strong>TIME-DOMAIN RESPONSE</strong></td>
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<td>( t_{r1}, t_{f1} )</td>
<td>Rise Time, Fall Time</td>
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<td>1.6</td>
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<td>ns</td>
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<tr>
<td>( t_{r2}, t_{f2} )</td>
<td>Rise Time, Fall Time</td>
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<tr>
<td>( t_{s1} )</td>
<td>Settling Time to 0.1%</td>
<td>2.0V Step</td>
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<td>13.0</td>
<td>IV</td>
<td>ns</td>
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<td>( t_{s2} )</td>
<td>Settling Time to 0.05%</td>
<td>2.0V Step</td>
<td>All</td>
<td>12.0</td>
<td>15.0</td>
<td>IV</td>
<td>ns</td>
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<td>OS</td>
<td>Overshoot ( V_{OUT} &lt; 0.5 \text{ Vpp} )</td>
<td>0.5V Step</td>
<td>25°C, ( T_{\text{MAX}} )</td>
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<td>10.0</td>
<td>IV</td>
<td>%</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td>( T_{\text{MIN}} )</td>
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<td>IV</td>
<td>%</td>
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<td>Slew Rate ( A_V = +2 )</td>
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<td>IV</td>
<td>V/μs</td>
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<td></td>
<td></td>
<td>( A_V = -2 )</td>
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<td>1600.0</td>
<td>V</td>
<td>V/μs</td>
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<td><strong>DISTORTION</strong></td>
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<td>HD2</td>
<td>2nd Harmonic Distortion at 20 MHz</td>
<td>2 Vpp</td>
<td>25°C</td>
<td>-60.0</td>
<td>-45.0</td>
<td>V</td>
<td>dBC</td>
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<td>( T_{\text{MIN}} )</td>
<td>-40.0</td>
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<td>V</td>
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<td>( T_{\text{MAX}} )</td>
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<td>V</td>
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<td>HD3</td>
<td>3rd Harmonic Distortion at 20 MHz</td>
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<td>25°C</td>
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<td>( T_{\text{MIN}}, T_{\text{MAX}} )</td>
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<td></td>
<td>V</td>
<td>dBC</td>
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Closed-Loop AC Electrical Characteristics — Contd.

\( V_S = \pm 5V, R_F = 2500\, \Omega, \, A_V = +2, R_L = 100\, \Omega \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<tr>
<td>NF</td>
<td>Noise Floor &gt;100 kHz</td>
<td>(Note 4)</td>
<td>25°C</td>
<td>-157.0</td>
<td>-154.0</td>
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<td>dBm (1 Hz)</td>
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<td>dBm (1 Hz)</td>
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<td>TMAX</td>
<td>-153.0IV</td>
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<td>dBm (1 Hz)</td>
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<td>INV</td>
<td>Integrated Noise 100 kHz to 200 MHz</td>
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<td>( \mu V )</td>
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DISABLE/ENABLE PERFORMANCE

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<th>Disable Time to &gt;50 dB</th>
<th>10 MHz</th>
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<th>V</th>
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<td>TON</td>
<td>Enable Time</td>
<td>All</td>
<td>200.0</td>
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<td>OFFISO</td>
<td>Off Isolation</td>
<td>10 MHz</td>
<td>All</td>
<td>55.0</td>
<td>59.0</td>
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VIDEO PERFORMANCE

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<th>Differential Gain (Note 5)</th>
<th>NTSC/PAL</th>
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<th>0.08</th>
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<th>% pp</th>
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<td>° pp</td>
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<td>dQ</td>
<td>Differential Phase (Note 5)</td>
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<td>° pp</td>
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<td></td>
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<td>° pp</td>
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<td>dQ</td>
<td>Differential Gain (Note 5)</td>
<td>30 MHz</td>
<td>25°C</td>
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<td>% pp</td>
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<td></td>
<td>° pp</td>
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<td>VBW</td>
<td>-0.1 dB Bandwidth (Note 5)</td>
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<td>25°C</td>
<td>0.05</td>
<td>0.18</td>
<td>IV</td>
<td>° pp</td>
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</tbody>
</table>

Note 1: Measured from \( T_{MIN} \) to \( T_{MAX} \).
Note 2: Supply current when disabled is measured at the negative supply.
Note 3: Common-mode input range for rated performance.
Note 4: Noise Tests are performed from 5 MHz to 200 MHz.
Note 5: Differential gain/phase tests are with \( R_L = 100\, \Omega \). For other values of \( R_L \), see curves.
Typical Performance Curves

Non-Inverting Frequency Response

Inverting Frequency Response

Frequency Response for Various R<sub>1</sub>

Open-Loop Transimpedance Gain and Phase

2nd and 3rd Harmonic Distortion

2-Tone 3rd Order Intermodulation Intercept

Equivalent Input Noise

Power-Supply Rejection Ratio

Common-Mode Rejection Ratio
Typical Performance Curves — Contd.

### Settling Time

\[ A_v = \pm 2 \]
\[ R_L = 100 \Omega \]
\[ \pm 2V \text{ Output Step} \]

**Recommended \( R_S \) vs Load Capacitance**

### Long-Term Settling Time

\[ A_v = \pm 2 \]
\[ R_L = 100 \Omega \]
\[ \pm 2V \text{ Output Step} \]

### Settling Time vs Load Capacitance

\[ 0.2 \text{ Ay} = +2 \]
\[ RL = 100D. \]

**Pulse Response \( A_v = +2 \)**

**Pulse Response \( A_v = +2 \)**

2070-4

2070-5

2070-6
Typical Performance Curves — Contd.

Differential Gain and Phase (3.58 MHz)

Differential Gain and Phase (4.43 MHz)

Differential Gain and Phase (30 MHz)

Forward and Reverse Gain during Disable

Enable/Disable Response
Equivalent Circuit

Burn-In Circuit

ALL PACKAGES USE THE SAME SCHEMATIC.
Applications Information

Theory of Operation
The EL2070 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2070 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the trans-impedance ($R_{OL}$) of the EL2070 [$V_{OUT} = (R_{OL}) \times (-I_{IN})$]. Since $R_{OL}$ is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:
1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2070. The nominal value for the feedback resistor is 250Ω, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing and eventually oscillations. Increasing the feedback resistor results in a lower $-3$ dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase
An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IREpp reference signal is applied to the device with 0V DC offset (0 IRE) at 3.58 MHz for NTSC, 4.43 MHz for PAL, and 30 MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100 IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75Ω in series at the drive end and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of 2 Vpp, with each back-terminated load at 150Ω. The EL2070 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback
The EL2070 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor’s impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.
Applications Information — Contd.

Offset Adjustment Pin
Output offset voltage of the EL2070 can be nulled by tying a 10k potentiometer between $+V_S$ and $-V_S$ with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to ±5V results in an offset voltage adjustment of at least ±10 mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout
As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2070 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation
The EL2070 has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or tied to pin 7. When more than 350 µA is pulled from pin 8, the EL2070 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced by ⅔. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (0.8 mA) if pin 8 is grounded.

To draw current out of pin 8 an open-collector TTL output, a 5V CMOS output, or an NPN transistor can be used.
EL2070 Macromodel

* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections: +input
*          |               -input
*          |               +Vs supply
*          |               -Vs supply
*          |               output

.subckt M2070 3 2 7 4 6

* Input Stage
 e1 10 0 3 0 1.0
 vis 10 9 0V
 h2 9 12 vxx 1.0
 r1 2 11 50
 l1 11 12 48nH
 iinp 3 0 8μA
 iinm 2 0 8μA

* Slew Rate Limiting
 h1 13 0 vis 600
 r2 13 14 1K
 d1 14 0 dclamp
 d2 0 14 dclamp

* High Frequency Pole
 e2 30 0 14 0 0.00166666666
 l3 30 17 0.1μH
 c5 17 0 0.1pF
 r5 17 0 500

* Transimpedance Stage
 g1 0 18 17 0 1.0
 rol 18 0 150K
 cdp 18 0 2.8pF

* Output Stage
 q1 4 18 19 qp
 q2 7 18 20 qu
 q3 7 19 21 qu
 q4 4 20 22 qp
 r7 21 6 2
 r8 22 6 2
EL2070 Macromodel — Contd.

ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is = 5e−15 bf = 200 tf = 0.05nS)
.model qp pnp (is = 5e−15 bf = 200 tf = 0.05nS)
.model dclamp d (is = 1e−30 ibv = 0.266 bv = 1.3 n = 4)
.ends
EL2070 Macromodel — Contd.
Features

- 200 MHz - 3 dB bandwidth, $A_V = 2$
- 12 ns settling to 0.05%
- $V_S = \pm 5V @ 15\ mA$
- Low distortion: HD2, HD3 @ $-60\ dBc$ at 20 MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- $\pm 1$ to $\pm 8$ closed-loop gain range
- Low cost
- Direct replacement for CLC400

Applications

- Video gain block
- Video distribution
- HDTV amplifier
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

General Description

The EL400 is a wide bandwidth, fast settling monolithic amplifier built using an advanced complementary bipolar process. This amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of $\pm 1$ to $\pm 8$, the EL400 has a 200 MHz - 3 dB bandwidth ($A_V = +2$), and 12 ns settling to 0.05% while consuming only 15 mA of supply current.

The EL400 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current, differential gain/phase of 0.02%/0.01°, and a minimum 50 mA output drive, performance in these areas is assured.

The EL400's settling to 0.05% in 12 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200 MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL400, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: Elantec's Processing, Monolithic Integrated Circuits.

Connection Diagram

DIP and SO Package

```
OFFSET ADJUST 1 8 NC
IN- 2 7 V+
IN+ 3 6 OUT
V- 4 5 NC
```

Top View

Manufactured under U.S. Patent No. 4,893,091
Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

- **Supply Voltage** \( (V_S) \): ±7V
- **Output Current**: ±7V
- **Common-Mode Input Voltage**: ±\( V_S \)
- **Differential Input Voltage**: 5V
- **Power Dissipation**: See Curves
- **Operating Temperature**: \(-40^\circ C \) to \(+85^\circ C\)

**Lead Temperature** (Soldering, 5 Seconds) 300°C
**Junction Temperature** 175°C
**Storage Temperature** \(-60^\circ C \) to \(+150^\circ C\)
**Thermal Resistance** \( \theta_{JA} = 95^\circ C/W \) P-DIP  
\( \theta_{JA} = 175^\circ C/W \) SO-8

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_P = T_C = T_A \).

**Open Loop DC Electrical Characteristics** \( V_S = \pm 5V, R_L = 100\Omega \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
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<tbody>
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<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
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<td>5.5</td>
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<td></td>
<td>( T_{MIN} )</td>
<td>8.7</td>
<td></td>
<td></td>
<td>III</td>
</tr>
<tr>
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<td>( T_{MAX} )</td>
<td>9.5</td>
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<td></td>
<td>III</td>
</tr>
<tr>
<td>( d(V_{OS})/dT )</td>
<td>Average Offset Voltage Drift</td>
<td>(Note 1)</td>
<td>All</td>
<td>10.0</td>
<td>40.0</td>
<td>IV</td>
<td>( \mu V/\circ C )</td>
</tr>
<tr>
<td>( +I_{IN} )</td>
<td>+ Input Current</td>
<td></td>
<td>25°C, ( T_{MAX} )</td>
<td>10.0</td>
<td>25.0</td>
<td></td>
<td>II</td>
</tr>
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<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>41.0</td>
<td></td>
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<td>III</td>
</tr>
<tr>
<td>( d(+I_{IN})/dT )</td>
<td>Average + Input Current Drift</td>
<td>(Note 1)</td>
<td>All</td>
<td>50.0</td>
<td>200.0</td>
<td>IV</td>
<td>( nA/\circ C )</td>
</tr>
<tr>
<td>( -I_{IN} )</td>
<td>- Input Current</td>
<td></td>
<td>25°C</td>
<td>10.0</td>
<td>25.0</td>
<td></td>
<td>I</td>
</tr>
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<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>41.0</td>
<td></td>
<td></td>
<td>III</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td>35.0</td>
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<td>III</td>
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<tr>
<td>( d(-I_{IN})/dT )</td>
<td>Average - Input Current Drift</td>
<td>(Note 1)</td>
<td>All</td>
<td>100.0</td>
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<td>( nA/\circ C )</td>
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<td>Power Supply Rejection Ratio</td>
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<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
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<tr>
<td>( I_S )</td>
<td>Supply Current—Quiescent</td>
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<td>15.0</td>
<td>23.0</td>
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2-152
### Open Loop DC Electrical Characteristics

$V_S = \pm 5V, R_L = 100\Omega$ unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+R_{IN}$</td>
<td>$+ Input Resistance$</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>100.0</td>
<td>200.0</td>
<td></td>
<td></td>
<td>II</td>
<td>kΩ</td>
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<tr>
<td>$T_{MIN}$</td>
<td></td>
<td>$50.0$</td>
<td></td>
<td></td>
<td></td>
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<td>III</td>
<td>kΩ</td>
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<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>All</td>
<td>0.5</td>
<td>2.0</td>
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<td>IV</td>
<td>pF</td>
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<td>$R_{OUT}$</td>
<td>Output Impedance (DC)</td>
<td>All</td>
<td>0.1</td>
<td>0.2</td>
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<td>IV</td>
<td>Ω</td>
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<tr>
<td>$CMIR$</td>
<td>Common-Mode Input Range</td>
<td>(Note 2)</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>2.0</td>
<td>2.1</td>
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<td>IV</td>
<td>V</td>
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<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>$25^\circ C, T_{MAX}$</td>
<td>50.0</td>
<td>70.0</td>
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<td></td>
<td>II</td>
<td>mA</td>
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<td>$T_{MIN}$</td>
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<td>$35.0$</td>
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<td></td>
<td></td>
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<td>III</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing</td>
<td>No Load</td>
<td>All</td>
<td>3.2</td>
<td>3.5</td>
<td></td>
<td>II</td>
<td>V</td>
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<tr>
<td>$V_{OUTL}$</td>
<td>Output Voltage Swing</td>
<td>$100\Omega$</td>
<td>25$^\circ C$</td>
<td>3.0</td>
<td>3.4</td>
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<td>I</td>
<td>V</td>
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<td>$R_{OL}$</td>
<td>Transimpedance</td>
<td>$25^\circ C$</td>
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<td>V</td>
<td>V/mA</td>
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<td>$T_{MAX}$</td>
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<td>V</td>
<td>V/mA</td>
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### Closed-Loop AC Electrical Characteristics

$V_S = \pm 5V, R_F = 250\Omega, A_V = +2, R_L = 100\Omega$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSBW</td>
<td>$-3\ dB$ Bandwidth ($V_{OUT} &lt; 0.5 \text{ Vpp}$)</td>
<td>$25^\circ C$</td>
<td>150.0</td>
<td>200.0</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}$</td>
<td>150.0</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
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<td></td>
<td></td>
<td>$T_{MAX}$</td>
<td>120.0</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>LSBW</td>
<td>$-3\ dB$ Bandwidth ($V_{OUT} &lt; 5.0 \text{ Vpp}$)</td>
<td>$A_V = +5$</td>
<td>All</td>
<td>35.0</td>
<td>50.0</td>
<td></td>
<td>IV</td>
<td>MHz</td>
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### Frequency Response

**FREQUENCY RESPONSE**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>GFPL</td>
<td>Peaking $V_{OUT} &lt; 0.5 \text{ Vpp}$</td>
<td>$&lt;40 \text{ MHz}$</td>
<td>$25^\circ C$</td>
<td>0.0</td>
<td>0.3</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
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<td></td>
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<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>GFPH</td>
<td>Peaking $V_{OUT} &lt; 0.5 \text{ Vpp}$</td>
<td>$&gt;40 \text{ MHz}$</td>
<td>$25^\circ C$</td>
<td>0.0</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
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<td></td>
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<td>0.7</td>
<td>V</td>
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<tr>
<td>GFR</td>
<td>Rolloff $V_{OUT} &lt; 0.5 \text{ Vpp}$</td>
<td>$&lt;75 \text{ MHz}$</td>
<td>$25^\circ C$</td>
<td>0.6</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td>dB</td>
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<tr>
<td></td>
<td></td>
<td>$T_{MIN}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
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<td></td>
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<td>1.3</td>
<td>V</td>
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<tr>
<td>LPD</td>
<td>Linear Phase Deviation $V_{OUT} &lt; 0.5 \text{ Vpp}$</td>
<td>$&lt;75 \text{ MHz}$</td>
<td>$25^\circ C, T_{MIN}$</td>
<td>0.2</td>
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<td>IV</td>
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<td>$T_{MAX}$</td>
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### Closed-Loop AC Electrical Characteristics — Contd.

\( V_S = \pm 5\text{V}, R_P = 250\Omega, A_V = \pm 2, R_L = 100\Omega \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{11}, t_{12} )</td>
<td>Rise Time, Fall Time</td>
<td>0.5V Step</td>
<td>( 25^\circ\text{C}, T_{\text{MIN}} )</td>
<td>1.6</td>
<td>2.4</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>( T_{\text{MAX}} )</td>
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<td>2.9</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td>( t_{21}, t_{22} )</td>
<td>Rise Time, Fall Time</td>
<td>5.0V Step</td>
<td>All</td>
<td>6.5</td>
<td>10.0</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td>( t_s )</td>
<td>Settling Time to 0.1%</td>
<td>2.0V Step</td>
<td>All</td>
<td>10.0</td>
<td>13.0</td>
<td>IV</td>
<td>ns</td>
<td></td>
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<tr>
<td>( t_s )</td>
<td>Settling Time to 0.05%</td>
<td>2.0V Step</td>
<td>All</td>
<td>12.0</td>
<td>15.0</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td>OS</td>
<td>Overshoot</td>
<td>0.5V Step</td>
<td>( 25^\circ\text{C} )</td>
<td>0.0</td>
<td>10.0</td>
<td>IV</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_{\text{MIN}}, T_{\text{MAX}} )</td>
<td></td>
<td>15.0</td>
<td>IV</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>( A_V = \pm 2 )</td>
<td>All</td>
<td>430.0</td>
<td>700.0</td>
<td>IV</td>
<td>V/\mu\text{s}</td>
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<tr>
<td></td>
<td></td>
<td>( A_V = \mp 2 )</td>
<td>All</td>
<td>1600.0</td>
<td></td>
<td>V</td>
<td>V/\mu\text{s}</td>
<td></td>
</tr>
</tbody>
</table>

### Distortion

- **HD2**: 2nd Harmonic Distortion at 20 MHz
  - 2 Vpp
  - \( 25^\circ\text{C} \)
  - \( T_{\text{MIN}} \): -60.0 dB
  - \( T_{\text{MAX}} \): -45.0 dB

- **HD3**: 3rd Harmonic Distortion at 20 MHz
  - 2 Vpp
  - \( 25^\circ\text{C} \)
  - \( T_{\text{MIN}} \): -60.0 dB
  - \( T_{\text{MAX}} \): -50.0 dB

### Equivalent Input Noise

- **NF**: Noise Floor > 100 kHz (Note 3)
  - \( 25^\circ\text{C} \)
  - \( T_{\text{MIN}} \): -157.0 dBm
  - \( T_{\text{MAX}} \): -154.0 dBm

- **INV**: Integrated Noise 100 kHz to 200 MHz (Note 3)
  - \( 25^\circ\text{C} \)
  - \( T_{\text{MIN}} \): 40.0 \mu\text{V}
  - \( T_{\text{MAX}} \): 63.0 \mu\text{V}

### Video Performance

- **d_Q**: Differential Gain
  - NTSC/PAL
  - \( 25^\circ\text{C} \)
  - 0.02 V

- **d_P**: Differential Phase
  - NTSC/PAL
  - \( 25^\circ\text{C} \)
  - 0.01 V

- **d_Q**: Differential Gain
  - 30 MHz
  - \( 25^\circ\text{C} \)
  - 0.05 V

- **d_P**: Differential Phase
  - 30 MHz
  - \( 25^\circ\text{C} \)
  - 0.05 V

- **VBW**: -0.1 dB Bandwidth
  - \( 25^\circ\text{C} \)
  - 60.0 MHz

**Note 1**: Measured from \( T_{\text{MIN}} \) to \( T_{\text{MAX}} \).
**Note 2**: Common-Mode Input Range for Rated Performance.
**Note 3**: Noise Tests are Performed from 5 MHz to 200 MHz.
**Note 4**: Differential Gain/Phase Tests are \( R_L = 100\Omega \). For other values of \( R_L \), see curves.
Typical Performance Curves

Non-Inverting Frequency Response

Inverting Frequency Response

Frequency Response for Various $R_L$

Open-Loop Transimpedance Gain and Phase

2nd and 3rd Harmonic Distortion

2-Tone 3rd Order Intermodulation Intercept

Equivalent Input Noise

Power-Supply Rejection Ratio

Common-Mode Rejection Ratio

Settling Time

Long-Term Settling Time

Settling Time vs Load Capacitance

EL400C
200 MHz Current Feedback Amplifier
Typical Performance Curves — Contd.

**Recommended $R_s$ vs Load Capacitance**

![Graph showing $R_s$ vs Load Capacitance](image)

**Pulse Response $A_V = +2$**

![Graph showing pulse response](image)

**Differential Gain and Phase (3.58 MHz)**

![Graph showing differential gain and phase](image)

**Differential Gain and Phase (4.43 MHz)**

![Graph showing differential gain and phase](image)

**Differential Gain and Phase (30 MHz)**

![Graph showing differential gain and phase](image)
Applications Information

Theory of Operation
The EL400 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL400 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance ($R_{OL}$) of the EL400 ($V_{OUT} = (R_{OL}) \times (-I_{IN})$). Since $R_{OL}$ is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:
1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL400. The nominal value for the feedback resistor is 250Ω, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase
An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IREpp reference signal is applied to the device with 0V DC offset (0IRE) at 3.58 MHz for NTSC, 4.43 MHz for
Applications Information — Contd.

PAL, and 30 MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75Ω in series at the drive end and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of 2 VPP, with each back-terminated load at 150Ω. The EL400 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback

The EL400 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Offset Adjustment Pin

Output offset voltage of the EL400 can be nulled by tying a 10k potentiometer between +Vs and −Vs with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to ±5V results in an offset voltage adjustment of at least ±10 mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL400 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.
EL400 Macromodel

* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:

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+input
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+input

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-Vsupply

-Vsupply

output

* Input Stage

e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 8µA
iinm 2 0 8µA

* Slew Rate Limiting

h1 13 0 via 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp

* High Frequency Pole

e2 30 0 14 0 0.001666666666
l3 30 17 0.1µH
c5 17 0 0.1pF
r5 17 0 500

* Transimpedance Stage

g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF

* Output Stage

q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qn
r7 21 6 2
r8 22 6 2
EL400C
200 MHz Current Feedback Amplifier

EL400 Macromodel — Contd.

ios1 7 19 2.5mA
ios2 20 4 2.5mA
  *
  * Supply Current
  *
  ips 7 4 9mA
  *
  * Error Terms
  *
ivos 0 23 5mA
vxx 23 0 0V
c4 24 0 3 0 1.0
c5 25 0 7 0 1.0
c6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
  *
  * Models
  *
.model qn npn (is = 5e−15 bf = 200 tf = 0.5nS)
.model qp pnp (is = 5e−15 bf = 200 tf = 0.5nS)
.model clamp d(is = 1e−3 ibv = 0.266 bv = 1.3 n = 4)
.ends
EL400 Macromodel — Contd.
**Features**
- 150 MHz - 3 dB bandwidth, 
  \( \text{Av} = 20 \)
- 10 ns settling to 0.1%
- \( V_s = \pm 5V \) @ 15 mA
- 2.5 ns rise/fall times (2V step)
- Overload/short-circuit protected
- ±7 to ±50 closed-loop gain range
- Low cost
- EL2171 is direct replacement for CLC401
- Disable capability on EL2071

**Applications**
- Line drivers
- DC-coupled log amplifiers
- High-speed modems, radios
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications
- Analog multiplexing (using disable—EL2071)
- Power down mode (using disable—EL2071)

**General Description**
The EL2071 and EL2171 are wide bandwidth, fast settling monolithic amplifiers built using an advanced complementary bipolar process. The EL2071 has a disable/enable feature which allows power down and analog multiplexing. These amplifiers use current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±7 to ±50, the EL2071 and EL2171 have a 150 MHz - 3 dB bandwidth (\( \text{Av} = +20 \)), and 2.5 ns rise/fall time, while consuming only 15 mA of supply current. The EL2071 consumes only 1.5 mA when disabled.

The wide 150 MHz bandwidth and extremely linear phase (0.2 dB deviation from linear at 50 MHz) allow superior signal fidelity. These features make the EL2071 and EL2171 especially suited for many digital communication system applications.

The EL2071’s and EL2171’s settling to 0.1% in 10 ns and ability to drive capacitive loads make them ideal in flash A/D applications. D/A systems can also benefit from the EL2071 and EL2171, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document, QRA-1: Elantec’s Processing, Monolithic Integrated Circuits.

**Connection Diagrams**

Manufactured under U.S. Patent No. 4,893,091

2-162
### Absolute Maximum Ratings \((T_A = 25^\circ\text{C})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>Supply Voltage ((V_S))</td>
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<td></td>
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<td>Output Current</td>
<td>Output is short-circuit protected to ground, however, maximum reliability is obtained if (I_{\text{OUT}}) does not exceed 70 mA.</td>
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<td>Common Mode Input Voltage</td>
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<td>±V_S</td>
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<td>Ceramic Packages</td>
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<tr>
<td>Plastic Packages</td>
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<td>Storage Temperature</td>
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### Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LIX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

### Open Loop DC Electrical Characteristics

\(V_S = ±5\text{V}, R_L = 100\Omega, \text{unless otherwise specified}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
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<td>25°C</td>
<td>3</td>
<td>6</td>
<td>10</td>
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<td>mV</td>
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<td></td>
<td>(T_{\text{MIN}}, T_{\text{MAX}})</td>
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<tr>
<td>(T_{\text{MIN}}, T_{\text{MAX}})</td>
<td>All</td>
<td></td>
<td>All</td>
<td>20</td>
<td>50</td>
<td>IV</td>
<td></td>
<td>(\mu\text{V/}^\circ\text{C})</td>
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<tr>
<td>(+I_{IN})</td>
<td>+ Input Current</td>
<td></td>
<td>25°C, (T_{\text{MAX}})</td>
<td>10</td>
<td>20</td>
<td>II</td>
<td></td>
<td>(\mu\text{A})</td>
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<tr>
<td></td>
<td>(T_{\text{MIN}})</td>
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<td></td>
<td></td>
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<td>(-I_{IN})</td>
<td>– Input Current</td>
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<td>25°C</td>
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<td>30</td>
<td>I</td>
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<td>(\mu\text{A})</td>
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<tr>
<td>(T_{\text{MIN}}, T_{\text{MAX}})</td>
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<td></td>
<td>All</td>
<td>100</td>
<td>200</td>
<td>IV</td>
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<td>nA/°C</td>
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<tr>
<td>(T_{\text{MIN}}, T_{\text{MAX}})</td>
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<td></td>
<td>All</td>
<td>100</td>
<td>200</td>
<td>IV</td>
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<td>nA/°C</td>
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## Open Loop DC Electrical Characteristics

\( V_S = \pm 5\, \text{V}, R_L = 100\, \Omega, \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>(Note 2)</td>
<td>All</td>
<td>50</td>
<td>55</td>
<td>II</td>
<td>dB</td>
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<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>All</td>
<td>40</td>
<td>50</td>
<td></td>
<td>II</td>
<td>dB</td>
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<tr>
<td>I_S</td>
<td>Supply Current—Quiescent</td>
<td>All</td>
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<td>21</td>
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<td>II</td>
<td>mA</td>
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<td>I_{OFF}</td>
<td>Supply Current—Disabled</td>
<td>EL2071C</td>
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<td>3.0</td>
<td>II</td>
<td>mA</td>
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<tr>
<td>+R_{IN}</td>
<td>+ Input Resistance</td>
<td>25°C, ( T_{\text{MAX}} )</td>
<td>100</td>
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<td>II</td>
<td>kΩ</td>
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<td>Input Capacitance</td>
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<td>pF</td>
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<td>R_{OUT}</td>
<td>Output Resistance (DC)</td>
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<td>0.3</td>
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<td>Ω</td>
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<td>Output Resistance (DC)</td>
<td>EL2071C Disabled</td>
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<td>100</td>
<td>200</td>
<td>IV</td>
<td>kΩ</td>
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<tr>
<td>C_{OUTD}</td>
<td>Output Capacitance (DC)</td>
<td>EL2071C Disabled</td>
<td>All</td>
<td>0.5</td>
<td>2.0</td>
<td>IV</td>
<td>pF</td>
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<tr>
<td>CMIR</td>
<td>Common-Mode Input Range</td>
<td>(Note 4)</td>
<td>25°C, ( T_{\text{MAX}} )</td>
<td>±2.5</td>
<td>±2.8</td>
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<td>V</td>
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<td>I_{OUT}</td>
<td>Output Current</td>
<td>25°C, ( T_{\text{MAX}} )</td>
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<td>mA</td>
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<td>V_{OUT}</td>
<td>Output Voltage Swing</td>
<td>No Load</td>
<td>25°C, ( T_{\text{MAX}} )</td>
<td>3.2</td>
<td>3.5</td>
<td>II</td>
<td>V</td>
<td></td>
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<td>V_{OUTL}</td>
<td>Output Voltage Swing ( R_L = 100, \Omega )</td>
<td>25°C</td>
<td>3.2</td>
<td>3.4</td>
<td></td>
<td>I</td>
<td>V</td>
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<td>R_{OL}</td>
<td>Transimpedance</td>
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<td>250</td>
<td>1000</td>
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<td>I</td>
<td>V/mA</td>
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<td>I_{LOGIC}</td>
<td>Pin 8 Current @ +5V</td>
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<td>All</td>
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<td>750</td>
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<td>μA</td>
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<td>V_{DIS}</td>
<td>Minimum Pin 8 V to Disable</td>
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<td>25°C</td>
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<td>II</td>
<td>V</td>
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<td>V_{EN}</td>
<td>Maximum Pin 8 V to Enable</td>
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<td>I_{DIS}</td>
<td>Minimum Pin 8 I to Disable</td>
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<td>μA</td>
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</table>
# Closed Loop AC Electrical Characteristics

$V_S = \pm 5V, R_F = 1.5 \, k\Omega, A_V = +20, R_L = 100\Omega$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td><strong>FREQUENCY RESPONSE</strong></td>
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<tr>
<td>SSBW</td>
<td>$-3$ dB Bandwidth ($V_{OUT} &lt; 2.0 , V_{PP}$)</td>
<td>$25^\circ C$</td>
<td>100</td>
<td>150</td>
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<td></td>
<td></td>
<td>V MHz</td>
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<tr>
<td></td>
<td></td>
<td>$T_{MIN}$</td>
<td>100</td>
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<td>V MHz</td>
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<tr>
<td>LSBW</td>
<td>$-3$ dB Bandwidth ($V_{OUT} &lt; 5.0 , V_{PP}$)</td>
<td>$25^\circ C, T_{MIN}$</td>
<td>65</td>
<td>100</td>
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<td>IV MHz</td>
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<td><strong>GAIN FLATNESS</strong></td>
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<td>GFPL</td>
<td>Peaking $V_{OUT} &lt; 2.0 , V_{PP}$ &lt;25 MHz</td>
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<td>V dB</td>
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<td>GFR</td>
<td>Rolloff $V_{OUT} &lt; 2.0 , V_{PP}$ &lt;50 MHz</td>
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<td>V dB</td>
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<td>$T_{MIN}$</td>
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<td>V dB</td>
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<td>$T_{MAX}$</td>
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<td>V dB</td>
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<td>LPD</td>
<td>Linear Phase Deviation $V_{OUT} &lt; 2.0 , V_{PP}$</td>
<td>&lt;50 MHz</td>
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<td>1.0</td>
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<td>IV °</td>
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<td>$t_{r1}, t_{f1}$</td>
<td>Rise Time, Fall Time 2.0V Step</td>
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<td>$t_{r2}, t_{f2}$</td>
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<td>$t_s$</td>
<td>Settling Time to 0.1% 2.0V Step</td>
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<td>IV %</td>
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<td>OS</td>
<td>Overshoot 2.0V Step</td>
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<td>10</td>
<td></td>
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<td>IV %</td>
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<td>IV V/μs</td>
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<td>IV V/μs</td>
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<td>HD2</td>
<td>2nd Harmonic Distortion @20 MHz 2 V_{PP}</td>
<td>$25^\circ C$</td>
<td>$-45$</td>
<td>$-35$</td>
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<td>V dB</td>
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<td>$T_{MIN}, T_{MAX}$</td>
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<td>V dB</td>
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<td>HD3</td>
<td>3rd Harmonic Distortion @20 MHz 2 V_{PP}</td>
<td>$25^\circ C$</td>
<td>$-60$</td>
<td>$-50$</td>
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<td>V dB</td>
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<td>$T_{MIN}$</td>
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<td></td>
<td>V dB</td>
</tr>
</tbody>
</table>
### Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = 1.5 \text{k}\Omega$, $A_V = \pm 20$, $R_L = 100\Omega$ unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EQUIVALENT INPUT NOISE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NF</td>
<td>Noise Floor $&gt;100$ kHz</td>
<td>$25^\circ\text{C}$</td>
<td>$-158$</td>
<td>$-155$</td>
<td>IV</td>
<td>dBm (1 Hz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{\text{MIN}}$</td>
<td>$-155$</td>
<td>IV</td>
<td>dBm (1 Hz)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{\text{MAX}}$</td>
<td>$-154$</td>
<td>IV</td>
<td>dBm (1 Hz)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INV</td>
<td>Integrated Noise 100 kHz to 200 MHz</td>
<td>$25^\circ\text{C}$</td>
<td>35</td>
<td>50</td>
<td>IV</td>
<td>$\mu$V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{\text{MIN}}$</td>
<td>50</td>
<td>IV</td>
<td>$\mu$V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{\text{MAX}}$</td>
<td>55</td>
<td>IV</td>
<td>$\mu$V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DISABLE/ENABLE PERFORMANCE — EL2071C**

| $T_{\text{OFF}}$ | $V_{\text{OUT}} = 2V_{\text{PP}}$ Disable Time to $>40$ dB | 20 MHz | All | 70 | 200 | IV | ns |
| $T_{\text{ON}}$ | Enable Time | All | 40 | 100 | IV | ns |
| ISO | Off Isolation | 20 MHz | All | 50 | 55 | IV | dB |

Note 1: Measured from $T_{\text{MIN}}$ to $T_{\text{MAX}}$.
Note 2: PSRR is measured at $V_S = \pm 4.5V$ and $V_S = \pm 5.5V$. Both supplies are changed simultaneously.
Note 3: Supply current when disabled is measured at the negative supply.
Note 4: Common-Mode Input Range for Rated Performance.
Typical Performance Curves

Non-Inverting Frequency Response

Inverting Frequency Response

Frequency Response for Various R_l8

Open-Loop Transimpedance Gain and Phase

Frequency Response, \( A_v = -1, R_F = 2.5 \, k\Omega \)

Equivalent Input Noise

Single Power Supply Rejection Ratio

Common Mode Rejection Ratio (\( A_v = +20 \))

Recommended \( R_S \) vs Load Capacitance
Typical Performance Curves — Contd.

2nd and 3rd Harmonic Distortion

2·Tone 3rd Order Intermodulation Intercept

Pulse Response $A_V = +20$

1 ns/div

Pulse Response $A_V = +20$

1 ns/div
Typical Performance Curves — Contd.

Forward and Reverse Gain during Disable—EL2071C

Disabled Attenuation vs Time for Various Output Levels—EL2071C

Disable Response—EL2071C

Enable Response—EL2071C
Typical Performance Curves — Contd.

8-Lead SO
Maximum Power Dissipation vs Ambient Temperature

- INFINITE HEAT SINK
- FREE AIR NO HEAT SINK

8-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

- INFINITE HEAT SINK
- FREE AIR NO HEAT SINK

Equivalent Circuit

[Diagram of the equivalent circuit]
Applications Information

Theory of Operation
The EL2071/EL2171 have a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2071/EL2171 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (ROL) of the EL2071/EL2171 \[ V_{OUT} = (ROL) \times (-I_{IN}) \]. Since ROL is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:
1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2071/EL2171. The nominal value for the feedback resistor is 1.5 kΩ, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower -3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Capacitive Feedback
The EL2071/EL2171 rely on their feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.
Applications Information — Contd.

Printed Circuit Layout
As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2071/EL2171 allow a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation for EL2071C
The EL2071C has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to ground. When the voltage at pin 8 is brought to within 0.4V of pin 7 (VS+), the EL2071C is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced to less than 2.2 mA. There are internal resistors which limit the current at pin 8 to a safe level (±500 μA) if pin 8 is shorted to either supply.

Typically, analog and digital circuits should have separate power supplies. This usually leads to slight differences between the power supply voltages. The EL2071C’s disable feature is dependent on the voltage at pins 8 and 7. Therefore, to operate the disable feature of the EL2071C dependably over temperature, it is recommended that the logic circuitry which drives pin 8 of the EL2071C operate from the same +5V supply as the EL2071C to avoid voltage differences between the digital and analog power supplies. Since VDIS is temperature dependent, it is recommended that 5V CMOS logic (with a VOH > 4.6V sourcing > 750 μA over temperature) be used to drive the disable pin of the EL2071C.

When disabled, (as well as in enabled mode), care must be taken to prevent a differential voltage between the + and − inputs greater than 5.0V. For example, in the figure below, the EL2071C is connected in a gain of +7 configuration and is disabled while the analog bus is driven externally to +5V. Pin 2 is consequently at +0.71V, and if VIN is driven to −5V, then 5.71V appears between pins 3 and 2. Internally, this voltage appears across a forward biased VBE in series with a reverse biased VBE and is past the threshold for zenering the reverse biased VBE. In a typical application, a 50Ω or 75Ω terminating resistor from pin 3 to ground will prevent pin 3 from approaching −5V.

![Diagam of Disable/Enable Operation for EL2071C](image)
Applications Information — Contd.

Using the EL2071C as a Multiplexer
An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs in common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown. The series resistance at each output helps to further increase isolation between amplifiers.

When the EL2071C is disabled, the DC output impedance is $>100$ k$\Omega$ in parallel with 2 pF capacitance.

To operate properly, the decoder that is used must have a $V_{OH} > (V_S^+) - 0.4$V with $I_{OH} = 750$ $\mu$A, and should be connected to the same power supply as the EL2071C.
EL2071 Macromodel

* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:

   + input
   -input
   +Vs supply
   -Vs supply
   output

.subckt M2071 3 2 7 4 6

* Input Stage
* e1 10 0 3 0 1.0
   vis 10 9 0V
   h2 9 12 vxx 1.0
   r1 2 11 2
   l1 11 12 1nH
   iinp 3 0 10uA
   iinm 2 0 10uA

* Slew Rate Limiting
* h1 13 0 vis 1K
   h1 13 0 vis 600
   r2 13 14 100
   d1 14 0 dclamp
   d2 0 14 dclamp

* High Frequency Pole
* e2 30 0 14 0 0.001666666666
   e2 30 0 14 0 0.001
   13 30 17 1.0uH
   c5 17 0 0.1pF
   r5 17 0 500

* Transimpedance Stage
* g1 0 18 17 0 1.0
   rol 18 0 1Meg
   cdp 18 0 0.88pF

* Output Stage
* q1 4 18 19 qp
   q2 7 18 20 qn
   q3 7 19 21 qn
   q4 4 20 22 qp
   r7 21 6 2
   r8 22 6 2
EL2071 Macromodel — Contd.

ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 3mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 316
r10 25 23 562
r11 26 23 562
*
* Models
*
.model qn npn (is = 5e-15 bf = 500 tf = 0.05nS)
.model qp pnp (is = 5e-15 bf = 500 tf = 0.05nS)
.model dclampd(is=1e-30 ibv=1pA bv=3.5 n=4)
.ends
EL2071 Macromodel

![Circuit Diagram](image)
Features
• 730 MHz – 3 dB bandwidth (0.5 Vpp)
• 5 ns settling to 0.2%
• \( V_S = \pm 5V \) @ 15 mA
• Low distortion: HD2, HD3 of \(-65\) dBc at 20 MHz
• Overload/short-circuit protected
• Closed-loop, unity gain
• Low cost
• Direct replacement for CLC110

Applications
• Video buffer
• Video distribution
• HDTV buffer
• High-speed A/D buffer
• Photodiode, CCD preamps
• IF processors
• High-speed communications

General Description
The EL2072 is a wide bandwidth, fast settling monolithic buffer built using an advanced complementary bipolar process. This buffer is closed loop to achieve lower output impedance and higher gain accuracy. Designed for closed-loop unity gain, the EL2072 has a 730 MHz – 3 dB bandwidth and 5 ns settling to 0.2% while consuming only 15 mA of supply current.

The EL2072 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current and a 70 mA output drive, performance in these areas is assured.

The EL2072’s settling to 0.2% in 5 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 730 MHz bandwidth and extremely linear phase allow unmatched signal fidelity.

The EL2072 can be used inside an amplifier loop or PLL as its wide bandwidth and fast rise time have minimal effect on loop dynamics.

Elantec products and facilities comply with MIL-I-45028A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document QRA-I: Elantec’s Processing, Monolithic Integrated Circuits.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2072CN</td>
<td>(-40^\circ\text{C} \text{ to } +85^\circ\text{C})</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2072CS</td>
<td>(-40^\circ\text{C} \text{ to } +85^\circ\text{C})</td>
<td>8-Pin SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagram

Manufactured under U.S. Patent No. 4,893,091
## Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Operating Temperature</th>
<th>Junction Temperature (175^\circ C)</th>
<th>Storage Temperature (-60^\circ C) to (+150^\circ C)</th>
<th>Thermal Resistance (\theta_{JA} = 95^\circ C/W) P-DIP</th>
<th>(\theta_{JA} = 175^\circ C/W) SO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V_S)</td>
<td>(\pm 7V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Current</td>
<td>Output is short-circuit protected to ground, however, maximum reliability is obtained if (I_{OUT}) does not exceed 70 mA.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>(\pm V_S)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

## DC Electrical Characteristics

\(V_S = \pm 5V, R_L = 100\Omega, R_S = 50\Omega\) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Output Offset Voltage</td>
<td></td>
<td>(25^\circ C)</td>
<td>2.0</td>
<td>8.0</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>(T_{MIN})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(T_{MAX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(TC_{VOS})</td>
<td>Average Offset Voltage Drift</td>
<td></td>
<td>(25^\circ C - T_{MAX})</td>
<td>20.0</td>
<td>50.0</td>
<td></td>
<td>IV</td>
<td>(\mu V/\circ C)</td>
</tr>
<tr>
<td></td>
<td>(25^\circ C - T_{MIN})</td>
<td></td>
<td></td>
<td>20.0</td>
<td>100.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_B)</td>
<td>Input Bias Current</td>
<td></td>
<td>(25^\circ C, T_{MAX})</td>
<td>10.0</td>
<td>50.0</td>
<td></td>
<td>II</td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td>(T_{MIN})</td>
<td></td>
<td></td>
<td></td>
<td>100.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(TC_{IB})</td>
<td>Average Input Bias Current Drift</td>
<td></td>
<td>(25^\circ C - T_{MAX})</td>
<td>200.0</td>
<td>300.0</td>
<td></td>
<td>IV</td>
<td>nA/(\circ C)</td>
</tr>
<tr>
<td></td>
<td>(25^\circ C - T_{MIN})</td>
<td></td>
<td></td>
<td>200.0</td>
<td>700.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(A_{V})</td>
<td>Small Signal Gain</td>
<td>(R_L = 100\Omega)</td>
<td>(25^\circ C)</td>
<td>0.96</td>
<td>0.98</td>
<td></td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td></td>
<td></td>
<td>0.95</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(IL_{IN})</td>
<td>Integral End Point linearity</td>
<td>(\pm 2V)</td>
<td>(T_{MAX})</td>
<td>0.2</td>
<td>0.4</td>
<td></td>
<td>IV</td>
<td>%F.S.</td>
</tr>
<tr>
<td></td>
<td>(T_{MIN})</td>
<td></td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>IV</td>
<td>%F.S.</td>
</tr>
<tr>
<td></td>
<td>(T_{MAX})</td>
<td></td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>IV</td>
<td>%F.S.</td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td></td>
<td>All</td>
<td>45.0</td>
<td>65.0</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>(I_S)</td>
<td>Supply Current—Quiescent</td>
<td>No Load</td>
<td>All</td>
<td>15.0</td>
<td>20.0</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

Note: See EL2071/EL2171 for Thermal Impedance curves.
### DC Electrical Characteristics

\( V_S = \pm 5V, R_L = 1000\Omega, R_S = 500\Omega \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{IN} )</td>
<td>Input Resistance</td>
<td></td>
<td>25°C</td>
<td>100.0</td>
<td>160.0</td>
<td>I</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>50.0</td>
<td></td>
<td>V</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td>200.0</td>
<td></td>
<td>V</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td></td>
<td>25°C</td>
<td>1.6</td>
<td>2.2</td>
<td>IV</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN}, T_{MAX} )</td>
<td>2.5</td>
<td></td>
<td>IV</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>Output Impedance (DC)</td>
<td></td>
<td>25°C</td>
<td>2.0</td>
<td>3.0</td>
<td>IV</td>
<td>Ω</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>( T_{MIN}, T_{MAX} )</td>
<td>3.5</td>
<td></td>
<td>IV</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output Current</td>
<td></td>
<td>25°C, ( T_{MAX} )</td>
<td>50.0</td>
<td>70.0</td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>45.0</td>
<td></td>
<td>V</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Voltage Swing</td>
<td>( R_L = 100\Omega )</td>
<td>25°C, ( T_{MAX} )</td>
<td>±3.2</td>
<td>±4.0</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>±3.0</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

\( V_S = \pm 5V, R_L = 1000\Omega, R_S = 500\Omega \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( SSBW )</td>
<td>(-3) dB Bandwidth ((V_{OUT} &lt; 0.5 \text{ V}_{pp}))</td>
<td></td>
<td>25°C</td>
<td>400.0</td>
<td>730.0</td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>400.0</td>
<td></td>
<td>IV</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td>300.0</td>
<td></td>
<td>IV</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( LSBW )</td>
<td>(-3) dB Bandwidth ((V_{OUT} = 5.0 \text{ V}_{pp}))</td>
<td></td>
<td>25°C</td>
<td>55.0</td>
<td>90.0</td>
<td>IV</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN}, T_{MAX} )</td>
<td>50.0</td>
<td></td>
<td>IV</td>
<td>MHz</td>
<td></td>
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</tbody>
</table>

#### FREQUENCY RESPONSE

#### GAIN FLATNESS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( GFPL )</td>
<td>Peaking ( V_{OUT} &lt; 0.5 \text{ V}_{pp} )</td>
<td>(&lt;200 \text{ MHz})</td>
<td>25°C</td>
<td>0.0</td>
<td>0.5</td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td>0.6</td>
<td></td>
<td>IV</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>0.8</td>
<td></td>
<td>IV</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( GFR )</td>
<td>Rolloff ( V_{OUT} &lt; 0.5 \text{ V}_{pp} )</td>
<td>(&lt;200 \text{ MHz})</td>
<td>25°C</td>
<td>0.0</td>
<td>0.8</td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td>1.0</td>
<td></td>
<td>IV</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td>1.2</td>
<td></td>
<td>IV</td>
<td>dB</td>
<td></td>
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<tr>
<td>( GDL )</td>
<td>Group Delay</td>
<td>(&lt;200 \text{ MHz})</td>
<td>25°C, ( T_{MIN} )</td>
<td>0.75</td>
<td>1.0</td>
<td>IV</td>
<td>ns</td>
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<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td>1.2</td>
<td></td>
<td>IV</td>
<td>ns</td>
<td></td>
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<tr>
<td>( LPD )</td>
<td>Linear Phase Deviation ( V_{OUT} &lt; 0.5 \text{ V}_{pp} )</td>
<td>(&lt;200 \text{ MHz})</td>
<td>25°C, ( T_{MIN} )</td>
<td>0.7</td>
<td>1.5</td>
<td>IV</td>
<td>°</td>
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<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td>2.0</td>
<td></td>
<td>IV</td>
<td>°</td>
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</table>
**AC Electrical Characteristics — Contd.**

\( V_S = \pm 5V, R_L = 100\Omega, R_S = 50\Omega \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<td><strong>TIME-DOMAIN RESPONSE</strong></td>
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<tr>
<td>TR1, TF1</td>
<td>Rise Time, Fall Time</td>
<td>0.5V Step</td>
<td>25°C, ( T_{MIN} )</td>
<td>0.4</td>
<td>1.0</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td></td>
<td>Input Signal Rise/Fall ( = 300 ) ps</td>
<td>( T_{MAX} )</td>
<td>1.4</td>
<td>IV</td>
<td>ns</td>
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<td></td>
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<tr>
<td>TR2, TF2</td>
<td>Rise Time, Fall Time</td>
<td>5.0V Step</td>
<td>25°C</td>
<td>4.5</td>
<td>7.5</td>
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<td>ns</td>
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<tr>
<td></td>
<td>Input Signal Rise/Fall ( \leq 1 ) ns</td>
<td>( T_{MIN}, T_{MAX} )</td>
<td>8.5</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td>TS1</td>
<td>Settling Time to 0.2%</td>
<td>2.0V Step</td>
<td>All</td>
<td>5.0</td>
<td>10.0</td>
<td>IV</td>
<td>ns</td>
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<td>Input Signal Rise/Fall ( \leq 1 ) ns</td>
<td>( T_{MIN}, T_{MAX} )</td>
<td>15.0</td>
<td>IV</td>
<td>%</td>
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<td>OS</td>
<td>Overshoot</td>
<td>0.5V Step</td>
<td>25°C</td>
<td>0.0</td>
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<tr>
<td></td>
<td>Input Signal Rise/Fall ( = 300 ) ps</td>
<td>( T_{MIN}, T_{MAX} )</td>
<td>15.0</td>
<td>IV</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td>SR</td>
<td>Slew Rate</td>
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<td></td>
<td></td>
<td>25°C</td>
<td>500.0</td>
<td>800.0</td>
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<td>V/( \mu )s</td>
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<td></td>
<td></td>
<td>( T_{MIN}, T_{MAX} )</td>
<td>450.0</td>
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<td>IV</td>
<td>V/( \mu )s</td>
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<td><strong>DISTORTION</strong></td>
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<tr>
<td>HD2</td>
<td>2nd Harmonic Distortion at 20 MHz</td>
<td>2 ( V_{PP} )</td>
<td>25°C</td>
<td>-55.0</td>
<td>-50.0</td>
<td>V</td>
<td>dBC</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td></td>
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<td>dBC</td>
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<td>-55.0</td>
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<td>dBC</td>
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<tr>
<td>HD2A</td>
<td>2nd Harmonic Distortion at 50 MHz</td>
<td>2 ( V_{PP} )</td>
<td>25°C, ( T_{MAX} )</td>
<td>-50.0</td>
<td>-45.0</td>
<td>IV</td>
<td>dBC</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MIN} )</td>
<td></td>
<td></td>
<td>-40.0</td>
<td>IV</td>
<td>dBC</td>
</tr>
<tr>
<td>HD3</td>
<td>3rd Harmonic Distortion at 20 MHz</td>
<td>2 ( V_{PP} )</td>
<td>25°C</td>
<td>-65.0</td>
<td>-55.0</td>
<td>V</td>
<td>dBC</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>( T_{MIN}, T_{MAX} )</td>
<td></td>
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<td>-55.0</td>
<td>IV</td>
<td>dBC</td>
</tr>
<tr>
<td>HD3A</td>
<td>3rd Harmonic Distortion at 50 MHz</td>
<td>2 ( V_{PP} )</td>
<td>25°C, ( T_{MIN} )</td>
<td>-60.0</td>
<td>-50.0</td>
<td>IV</td>
<td>dBC</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td></td>
<td></td>
<td>-45.0</td>
<td>IV</td>
<td>dBC</td>
</tr>
<tr>
<td><strong>EQUIVALENT INPUT NOISE</strong></td>
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<tr>
<td>NF</td>
<td>Noise Floor ( &gt; 100 ) kHz</td>
<td>25°C, ( T_{MIN} )</td>
<td>-158.0</td>
<td>-155.0</td>
<td>IV</td>
<td>dBm (1 Hz)</td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td></td>
<td></td>
<td>-154.0</td>
<td>IV</td>
<td>dBm (1 Hz)</td>
</tr>
<tr>
<td>INV</td>
<td>Integrated Noise ( 100 ) kHz to 200 MHz</td>
<td>25°C, ( T_{MIN} )</td>
<td>40.0</td>
<td>57.0</td>
<td>IV</td>
<td>( \mu )V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{MAX} )</td>
<td></td>
<td></td>
<td>63.0</td>
<td>IV</td>
<td>( \mu )V</td>
</tr>
</tbody>
</table>
Typical Performance Curves \((V_S = \pm 5V, R_L = 1000\Omega, R_S = 500\Omega)\)

Forward Gain and Phase

Gain Flatness & Deviation from Linear Phase

Reverse Gain and Phase

Input Impedance

Output Impedance

Recommended \(R_S\) vs Load Capacitance

Integral Linearity Error

Frequency Response vs \(R_{load}\)

\(|S_{21}|\) vs \(C_{load}\) with Recommended \(R_S\)
**Typical Performance Curves** 

(V_S = ±5V, R_L = 100Ω, R_S = 50Ω) — Contd.

**Small Signal Pulse Response**

![Small Signal Pulse Response Graph]

**Large Signal Pulse Response**

![Large Signal Pulse Response Graph]

**Long-Term Settling Time**

![Long-Term Settling Time Graph]

**2nd Harmonic Distortion**

![2nd Harmonic Distortion Graph]

**3rd Harmonic Distortion**

![3rd Harmonic Distortion Graph]

**2-Tone, 3rd Order Intermodulation Intercept**

![2-Tone, 3rd Order Intermodulation Intercept Graph]
Burn-In Circuit

Printed Circuit Layout
As with any high-frequency device, good PCB layout is necessary for optimum performance. This is especially important for the EL2072, which has a typical bandwidth of 730 MHz. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. A closely-placed 0.01 μF ceramic capacitor between each supply pin and the ground plane is usually sufficient decoupling.

Pins 2, 3, 6, and 7 should be connected to the ground-plane to minimize capacitive feed-through, and all input and output traces should be laid out as transmission lines and terminated as close to the EL2072 package as possible.

Increasing capacitance on the output of the EL2072 will add phase shift, decreasing phase margin and increasing frequency-response peaking. A small series resistor before the capacitance decouples this effect, and should be used for large capacitance values. Please refer to the graphs for the appropriate resistor value to be used.
Features
- 200 MHz gain-bandwidth product
- Unity-gain stable
- Ultra low video distortion = 0.01%/0.015° @ NTSC/PAL
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%
- Low distortion = -60 dB HD2, -70 dB HD3 @ 20 MHz, 2 Vpp, Av = +1

Applications
- High resolution video
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2073CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2073CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

General Description

The EL2073 is a precision voltage-feedback amplifier featuring a 200 MHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2073 is unity-gain stable with a −3 dB bandwidth of 400 MHz. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2073 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2073 the ideal choice for all op-amp applications requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2073 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document, QRA-1: Elantec’s Processing, Monolithic Integrated Circuits.

Connection Diagram

DIP and SO Package
EL2073C
200 MHz Unity-Gain Stable Operational Amplifier

Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Test Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ((V_S))</td>
<td>(\pm 7) V</td>
<td>I</td>
</tr>
<tr>
<td>Output Current</td>
<td>Output is short-circuit protected to ground, however, maximum reliability is obtained if (I_{OUT}) does not exceed 70 mA.</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Input</td>
<td>(\pm V_S)</td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>(\pm 5) V</td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Thermal Resistance

- \(\theta_{JA} = 95^\circ C/W\) P-DIP
- \(\theta_{JA} = 175^\circ C/W\) SO-8

Operating Temperature
- \(-40^\circ C\) to \(+85^\circ C\)

Junction Temperature
- \(+175^\circ C\)

Storage Temperature
- \(-60^\circ C\) to \(+150^\circ C\)

Open Loop DC Electrical Characteristics

\(V_S = \pm 5\) V, \(R_L = 100\) k\(\Omega\), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(V_{CM} = 0) V</td>
<td>(25^\circ C)</td>
<td>0.2</td>
<td>1.5</td>
<td>I</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(T_{MIN}-T_{MAX})</td>
<td></td>
<td></td>
<td>(3)</td>
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<td></td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>(T_{MIN}-T_{MAX})</td>
<td>Average Offset Voltage Drift</td>
<td>(\text{All})</td>
<td>(8)</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
<td>(\mu V/\circ C)</td>
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<td>(I_B)</td>
<td>Input Bias Current</td>
<td>(25^\circ C)</td>
<td>(2)</td>
<td>6</td>
<td>I</td>
<td>I</td>
<td>(\mu A)</td>
<td></td>
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<tr>
<td>(I_{OS})</td>
<td>Input Offset Current</td>
<td>(V_{CM} = 0) V</td>
<td>(25^\circ C)</td>
<td>0.1</td>
<td>1</td>
<td>I</td>
<td>I</td>
<td>(\mu A)</td>
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<tr>
<td>(T_{MIN}-T_{MAX})</td>
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<td>(2)</td>
<td></td>
<td></td>
<td></td>
<td>(\mu A)</td>
<td></td>
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<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td>(\text{No Load})</td>
<td>(25^\circ C)</td>
<td>60</td>
<td>80</td>
<td>I</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(T_{MIN}-T_{MAX})</td>
<td></td>
<td></td>
<td>(60)</td>
<td></td>
<td></td>
<td></td>
<td>(\mu A)</td>
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</tr>
<tr>
<td>(CMRR)</td>
<td>Common Mode Rejection Ratio</td>
<td>(\text{No Load})</td>
<td>(25^\circ C)</td>
<td>65</td>
<td>90</td>
<td>I</td>
<td>I</td>
<td>dB</td>
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<tr>
<td>(I_S)</td>
<td>Supply Current—Quiescent</td>
<td>No Load</td>
<td>(25^\circ C)</td>
<td>21</td>
<td>25</td>
<td>I</td>
<td>I</td>
<td>mA</td>
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<tr>
<td>(R_{IN})</td>
<td>(R_{IN}) (Differential)</td>
<td>Open-Loop</td>
<td>(25^\circ C)</td>
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<td></td>
<td>k(\Omega)</td>
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<tr>
<td>(C_{IN})</td>
<td>(C_{IN}) (Differential)</td>
<td>Open-Loop</td>
<td>(25^\circ C)</td>
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<td></td>
<td>p(\Phi)</td>
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<tr>
<td>(R_{IN})</td>
<td>(R_{IN}) (Common-Mode)</td>
<td>Open-Loop</td>
<td>(25^\circ C)</td>
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<td></td>
<td>M(\Omega)</td>
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<tr>
<td>(C_{IN})</td>
<td>(C_{IN}) (Common-Mode)</td>
<td>Open-Loop</td>
<td>(25^\circ C)</td>
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<td></td>
<td></td>
<td>p(\Phi)</td>
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Note: See EL2071/EL2171 for Thermal Impedance curves.
### Open Loop DC Electrical Characteristics

$V_S = \pm 5V, R_L = 100\Omega$, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>$R_{OUT}$</td>
<td>Output Resistance</td>
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<td>25°C</td>
<td>20</td>
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<td>V mΩ</td>
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<tr>
<td>CMIR</td>
<td>Common-Mode Input Range</td>
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<td>25°C</td>
<td>±3</td>
<td>±3.5</td>
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<td></td>
<td>IV V</td>
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<tr>
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<td></td>
<td>$T_{MIN} - T_{MAX}$</td>
<td>±2.5</td>
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<td></td>
<td></td>
<td>IV V</td>
<td>V/V</td>
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<td>$I_{OUT}$</td>
<td>Output Current</td>
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<td>25°C</td>
<td>50</td>
<td>70</td>
<td></td>
<td></td>
<td>I mA</td>
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<td>$T_{MIN} - T_{MAX}$</td>
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<td>IV V</td>
<td>V/V</td>
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<td>$V_{OUT}$</td>
<td>Output Voltage Swing</td>
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<td>±3.5</td>
<td>±4</td>
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<td></td>
<td>I V</td>
</tr>
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<td></td>
<td>$T_{MIN} - T_{MAX}$</td>
<td>±3.5</td>
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<td></td>
<td>IV V</td>
<td>V/V</td>
</tr>
<tr>
<td>$V_{OUT;100}$</td>
<td>Output Voltage Swing</td>
<td>100Ω</td>
<td>25°C</td>
<td>±3</td>
<td>±3.6</td>
<td></td>
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</tr>
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<td></td>
<td>$T_{MIN} - T_{MAX}$</td>
<td>±3</td>
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<td></td>
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<td>IV V</td>
<td>V/V</td>
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<tr>
<td>$V_{OUT;50}$</td>
<td>Output Voltage Swing</td>
<td>50Ω</td>
<td>25°C</td>
<td>±3</td>
<td>±3.4</td>
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<td>$T_{MIN} - T_{MAX}$</td>
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<td>IV V</td>
<td>V/V</td>
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<tr>
<td>$A_{VOL;100}$</td>
<td>Open-Loop Gain</td>
<td>100Ω</td>
<td>25°C</td>
<td>500</td>
<td>1000</td>
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<td>I V/V</td>
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<td>IV V/V</td>
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<td>$A_{VOL;50}$</td>
<td>Open-Loop Gain</td>
<td>50Ω</td>
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<td>$T_{MIN} - T_{MAX}$</td>
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<td>IV V/V</td>
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<td>$cN@ &gt; 1;MHz$</td>
<td>Noise Voltage 1–100 MHz</td>
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<td>V pA/Hz</td>
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### Closed Loop AC Electrical Characteristics

$V_S = \pm 5V, A_V = +1, R_f = 0\Omega, R_L = 100\Omega$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
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<td>SSBW</td>
<td>$-3;dB$ Bandwidth</td>
<td>$A_V = +1$</td>
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<td>$A_V = -1$</td>
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<td>$A_V = +2$</td>
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<td>$T_{MIN} - T_{MAX}$</td>
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<td>IV MHz</td>
<td>V MHz</td>
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<td>$A_V = +5$</td>
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<td>GBWP</td>
<td>Gain-Bandwidth Product</td>
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<td>LSBWa</td>
<td>$-3;dB$ Bandwidth</td>
<td>$V_{OUT} = 2;V_{PP}$ (Note 4)</td>
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<td>LSBWb</td>
<td>$-3;dB$ Bandwidth</td>
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<td>GFPL</td>
<td>Peaking (&lt;50 MHz)</td>
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<td>dB</td>
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<td>IV dB</td>
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<td>IV dB</td>
<td>dB</td>
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Closed Loop AC Electrical Characteristics

\( V_S = \pm 5V, A_V = +1, R_f = 0\Omega, R_L = 100\Omega \) unless otherwise specified — Contd.

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<th>Test Level</th>
<th>Units</th>
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<td>1.8</td>
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<td>PM</td>
<td>Phase Margin</td>
<td>( A_V = +1 )</td>
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<td>60</td>
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<td>V</td>
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<td>Rise Time, Fall Time</td>
<td>0.4V Step, ( A_V = +2 )</td>
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<td>2</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>tr2, tf2</td>
<td>Rise Time, Fall Time</td>
<td>5V Step, ( A_V = +2 )</td>
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<td>15</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
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<tr>
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<td>Settling to 0.1% ((A_V = -1))</td>
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<tr>
<td>ts2</td>
<td>Settling to 0.01% ((A_V = -1))</td>
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<td>25</td>
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<td>V</td>
<td>%</td>
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<td>SR</td>
<td>Slew Rate</td>
<td>2V Step</td>
<td>All</td>
<td>175</td>
<td>250</td>
<td></td>
<td>IV</td>
<td>V/\mu s</td>
</tr>
</tbody>
</table>

DISTORTION (Note 5)

|          | 2nd Harmonic Distortion                          | @ 10 MHz, \( A_V = +2 \) | 25°C | −65 | −55 |     | IV         | dBC   |
| HD2a      |                                                  | @ 20 MHz, \( A_V = +1 \)   | 25°C | −60 | −50 |     | IV*        | dBC   |
| HD2b      |                                                  | @ 20 MHz, \( A_V = +2 \)   | 25°C | −55 | −50 |     | IV         | dBC   |
| HD3a      | 3rd Harmonic Distortion                          | @ 10 MHz, \( A_V = +2 \)   | TMIN-TMAX | −45 |     | IV         | dBC   |
| HD3b      | 3rd Harmonic Distortion                          | @ 20 MHz, \( A_V = +1 \)   | 25°C | −70 | −60 |     | IV         | dBC   |
| HD3c      | 3rd Harmonic Distortion                          | @ 20 MHz, \( A_V = +2 \)   | 25°C | −70 | −60 |     | IV         | dBC   |

VIDEO PERFORMANCE (Note 6)

|          | Differential Gain                               | NTSC                     | 25°C | 0.01 | 0.05 |     | IV         | %pp   |
| dG        |                                                  |                         |      |      |      |     |           |       |
| dp        | Differential Phase                              | NTSC                     | 25°C | 0.015| 0.05 |     | IV*        | %pp   |
| dG        | Differential Gain                               | 30 MHz                   | 25°C | 0.1  |     |     | V          | %pp   |
| dp        | Differential Phase                              | 30 MHz                   | 25°C | 0.1  |     |     | V          | %pp   |
| VBW       | ±0.1 dB Bandwidth Flatness                      |                         | 25°C | 25   | 50   |     | IV         | MHz   |

Note 1: Measured from \( T_{MIN}, T_{MAX} \).
Note 2: \( \pm V_{CC} = \pm 4.5V \) to 5.5V.
Note 3: \( \pm V_{IN} = \pm 2.5V, V_{OUT} = 0V \).
Note 4: Large-signal bandwidth calculated using \( LSBW = \frac{Slew\,Rate}{2\pi V_{PEAK}} \).
Note 5: All distortion measurements are made with \( V_{OUT} = 2 V_{PP}, R_L = 100\Omega \).
Note 6: Video performance measured at \( A_V = +1 \) with 2 times normal video level across \( R_L = 100\Omega \). This corresponds to standard video levels across a back-terminated 50\(\Omega \) load, i.e., 0–100 IRE, 40IRE\text{pp} giving a 1 V\text{pp} video signal across the 50\(\Omega \) load. For other values of \( R_L \), see curves.
Typical Performance Curves (\(T_A = 25^\circ C\))

- **Non-Inverting Frequency Response**
- **Inverting Frequency Response**
- **Open Loop Gain and Phase**
- **Output Voltage Swing vs Frequency**
- **Equivalent Input Noise**
- **PSRR, CMRR, and Closed-Loop \(R_O\) vs Frequency**
- **2nd and 3rd Harmonic Distortion vs Frequency**
- **2-Tone, 3rd Order Intermodulation Intercept**

---

**Frequency Response for Various \(R_f\)**

- **Gain**
- **Phase**

---

**PSRR, CMRR, and Closed-Loop \(R_O\) vs Frequency**

- **Gain**
- **Phase**

---

**2nd and 3rd Harmonic Distortion vs Frequency**

- **Gain**
- **Phase**

---

**2-Tone, 3rd Order Intermodulation Intercept**

- **Gain**
- **Phase**
Typical Performance Curves (T_A = 25°C unless otherwise specified) — Contd.

Series Resistor and Resulting Bandwidth vs Capacitive Load

Settling Time vs Output Voltage Change

Settling Time vs Closed-Loop Gain

Common-Mode Rejection Ratio vs Input Common-Mode Voltage

Bias and Offset Current vs Input Common-Mode Voltage

Supply Current vs Temperature

Bias and Offset Current vs Temperature

Offset Voltage vs Temperature

AVOL, PSRR, and CMRR vs Temperature
Typical Performance Curves ($T_A = 25^\circ C$) — Contd.

Small Signal Transient Response

Differential Gain and Phase vs DC Input Offset at 3.58 MHz

Differential Gain and Phase vs DC Input Offset at 4.43 MHz

Differential Gain and Phase vs DC Input Offset at 30 MHz

Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz

Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz

Differential Gain and Phase vs Number of 150Ω Loads at 30 MHz

2072-4

2072-5

2073-6
Equivalent Circuit

Burn-In Circuit

All Packages Use The Same Schematic
Applications Information

Product Description
The EL2073 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2073 uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2073 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2073 is an excellent choice for applications such as log amplifiers.

The EL2073 also has excellent DC specifications: 200 µV, VΩS, 2 µA IΩ, 0.1 µA IΩS, and 90 dB of CMRR. These specifications allow the EL2073 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2073 is only 3.2 pA/√Hz, making it an excellent choice for high-sensitivity trans-impedance amplifier configurations.

Gain-Bandwidth Product
The EL2073 has a gain-bandwidth product of 200 MHz. For gains greater than 4, its closed-loop -3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2073 has a -3 dB bandwidth of 400 MHz at a gain of +1, dropping to 200 MHz at a gain of +2. It is important to note that the EL2073 has been designed so that this “extra” bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2073 in a gain of +1 only exhibits 1 dB of peaking with a 100Ω load.

Video Performance
An industry-standard method of measuring the video distortion of a component such as the EL2073 is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 Vpp (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC, 4.43 MHz for PAL, or 30 MHz for HDTV. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2073 has been designed to be among the best video amplifiers in the marketplace today. It has been thoroughly characterized for video performance in the topology described above, and the results have been included as minimum dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2073 exhibits dG and dP of only 0.01% and 0.015° at NTSC and PAL. Because dG and dP vary with different DC offsets, the superior video performance of the EL2073 has been characterized over the entire DC offset range from -0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The excellent output drive capability of the EL2073 allows it to drive up to 4 back-terminated loads with excellent video performance. With 4 150Ω loads, dG and dP are only 0.15% and 0.08° at NTSC and PAL. For more information, refer to the curves for Video Performance vs Number of 150Ω Loads.

Output Drive Capability
The EL2073 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 Vpp into a 50Ω load. This high output drive capability makes the EL2073 an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2073 remains a minimum of 50 mA at low temperatures. The EL2073 is current-limited at
Applications Information
the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads
Although the EL2073 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without peaking.

Printed-Circuit Layout
As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 μF – 10 μF tantalum capacitor is recommended in parallel with a 0.01 μF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2073 directly to the PCB board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.
EL2073C
200 MHz Unity-Gain Stable Operational Amplifier

EL2073 Macromodel

* Connections:
+input
-input
+Vsupply
-Vsupply
output

.subckt M2073

* Input Stage
ie 37 4 1mA
r6 36 37 125
r7 38 37 125
rcl 7 30 200
rc2 7 39 200
ql 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1Meg

* Compensation Section
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 1.2pF
rc 34 40 400
cc 40 0 0.3pF

* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 0.5pF
rpb 42 43 50
cpb 43 0 0.5pF

* Output Stage
ios1 7 50 3.0mA
ios2 51 4 3.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2

* Power Supply Current
ips 7 4 11.4mA

* Models
.model qna npn(is=800e-18 bf=170 tf=0.2ns)
.model qn npn(is=810e-18 bf=200 tf=0.2ns)
.model qp pnp(is=800e-18 bf=200 tf=0.2ns)
.ends
EL2073 Macromodel — Contd.
**Features**

- 400 MHz gain-bandwidth product
- Gain-of-2 stable
- Ultra low video distortion = 0.01%/0.015° @ NTSC/PAL
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%
- Low distortion = -55 dB HD2, -70 dB HD3 @ 20 MHz, 2 Vpp, \( A_v = +2 \)

**Applications**

- High resolution video
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

**General Description**

The EL2074 is a precision voltage-feedback amplifier featuring a 400 MHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2074 is gain-of-2 stable with a −3 dB bandwidth of 400 MHz at \( A_v = +2 \). It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2074 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2074 the ideal choice for all op-amp applications at a noise gain of 2 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2074 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document, QRA-1: *Elantec’s Processing, Monolithic Integrated Circuits*.

**Connection Diagram**

![Connection Diagram](image)
Absolute Maximum Ratings \((T_A = 25^\circ C)\)

Supply Voltage \((V_S)\) \(\pm 7V\)

Output Current

Common-Mode Input \(\pm V_S\)

Differential Input Voltage \(5V\)

Output is short-circuit protected to ground, however, maximum reliability is obtained if \(I_{OUT}\) does not exceed 70 mA.

Thermal Resistance \(\theta_{JA} = 95^\circ C/W \text{ P-DIP}\)

Operating Temperature \(0^\circ C\) to \(+75^\circ C\)

Junction Temperature \(175^\circ C\)

Storage Temperature \(-60^\circ C\) to \(+150^\circ C\)

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Test Level   Test Procedure
---   -------------------------------
I   100% production tested and QA sample tested per QA test plan QCX0002.
II  100% production tested at \(T_A = 25^\circ C\) and QA sample tested at \(T_A = 25^\circ C\), \(T_{MAX}\) and \(T_{MIN}\) per QA test plan QCX0002.
III QA sample tested per QA test plan QCX0002.
IV Parameter is guaranteed (but not tested) by Design and Characterization Data.
V  Parameter is typical value at \(T_A = 25^\circ C\) for information purposes only.

Open Loop DC Electrical Characteristics

\(V_S = \pm 5V, R_L = 100\Omega\), unless otherwise specified

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<td>IB</td>
<td>Input Bias Current</td>
<td>(V_{CM} = 0V)</td>
<td></td>
<td></td>
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<tr>
<td>IOS</td>
<td>Input Offset Current</td>
<td>(V_{CM} = 0V)</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>(Note 2)</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>(Note 3)</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>(I_S)</td>
<td>Supply Current—Quiescent</td>
<td>No Load</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>RIN (diff)</td>
<td>(R_{IN}) (Differential)</td>
<td>Open-Loop</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>CIN (diff)</td>
<td>(C_{IN}) (Differential)</td>
<td>Open-Loop</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>RIN (cm)</td>
<td>(R_{IN}) (Common-Mode)</td>
<td>(25^\circ C)</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CIN (cm)</td>
<td>(C_{IN}) (Common-Mode)</td>
<td>(25^\circ C)</td>
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</table>
### Open Loop DC Electrical Characteristics

$V_S = \pm 5\text{V}, R_L = 100\Omega$, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>$R_{OUT}$</td>
<td>Output Resistance</td>
<td></td>
<td>$25^\circ\text{C}$</td>
<td>20</td>
<td>V</td>
<td></td>
<td></td>
<td>V/mΩ</td>
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<tr>
<td>CMIR</td>
<td>Common-Mode Input Range</td>
<td></td>
<td>$25^\circ\text{C}$</td>
<td>±3</td>
<td>±3.5</td>
<td>IV</td>
<td>V</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{\text{MIN}}, T_{\text{MAX}}$</td>
<td>±2.5</td>
<td></td>
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<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>No Load</td>
<td>All</td>
<td>50</td>
<td>70</td>
<td>II</td>
<td>mA</td>
<td></td>
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<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing</td>
<td>100Ω</td>
<td>All</td>
<td>±3.5</td>
<td>±4</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT\ 100}$</td>
<td>Output Voltage Swing</td>
<td>50Ω</td>
<td>All</td>
<td>±2.5</td>
<td>±3.6</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT\ 50}$</td>
<td>Open-Loop Gain</td>
<td>100Ω</td>
<td>$25^\circ\text{C}$</td>
<td>500</td>
<td>1000</td>
<td>I</td>
<td>V/V</td>
<td></td>
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<td>$T_{\text{MIN}}, T_{\text{MAX}}$</td>
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<tr>
<td>$A_{VOL\ 100}$</td>
<td>Open-Loop Gain</td>
<td>50Ω</td>
<td>$25^\circ\text{C}$</td>
<td>400</td>
<td>800</td>
<td>I</td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{\text{MIN}}, T_{\text{MAX}}$</td>
<td>300</td>
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<tr>
<td>$eN@ &gt; 1\text{ MHz}$</td>
<td>Noise Voltage 1–100 MHz</td>
<td>All</td>
<td>25°C</td>
<td>2.3</td>
<td></td>
<td>V</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>$iN@ &gt; 100\text{ kHz}$</td>
<td>Noise Current 100k–100 MHz</td>
<td>All</td>
<td>25°C</td>
<td>3.2</td>
<td></td>
<td>V</td>
<td>pA/√Hz</td>
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</tbody>
</table>

### Closed Loop AC Electrical Characteristics

$V_S = \pm 5\text{V}, A_V = +2, R_f = R_g = 2500\Omega, C_f = 3\text{pF}, R_L = 100\Omega$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSBW</td>
<td>$-3\text{ dB Bandwidth}$ ((V_{OUT} = 0.4\text{Vpp}))</td>
<td>$A_V = -1$</td>
<td>$25^\circ\text{C}$</td>
<td>400</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$A_V = +2$</td>
<td>$25^\circ\text{C}$</td>
<td>250</td>
<td>400</td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{\text{MIN}}, T_{\text{MAX}}$</td>
<td>250</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>$A_V = +5$</td>
<td>$25^\circ\text{C}$</td>
<td>100</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$A_V = +10$</td>
<td>$25^\circ\text{C}$</td>
<td>40</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain-Bandwidth Product</td>
<td>$A_V = +10$</td>
<td>$25^\circ\text{C}$</td>
<td>400</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>LSBWa</td>
<td>$-3\text{ dB Bandwidth}$ ((V_{OUT} = 2\text{Vpp}))</td>
<td>$V_{OUT} = 2\text{Vpp}$ ((\text{Note 4}))</td>
<td>All</td>
<td>43</td>
<td>63</td>
<td>IV</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>LSBWb</td>
<td>$-3\text{ dB Bandwidth}$ ((V_{OUT} = 5\text{Vpp})) ((\text{Note 4}))</td>
<td>$V_{OUT} = 5\text{Vpp}$ ((\text{Note 4}))</td>
<td>All</td>
<td>17</td>
<td>25</td>
<td>IV</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>GFPL</td>
<td>Peaking (&lt;50 MHz)</td>
<td>$V_{OUT} = 0.4\text{Vpp}$</td>
<td>$25^\circ\text{C}$</td>
<td>0</td>
<td>1</td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{\text{MIN}}, T_{\text{MAX}}$</td>
<td></td>
<td>1</td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>GFPH</td>
<td>Peaking (&gt;50 MHz)</td>
<td>$V_{OUT} = 0.4\text{Vpp}$</td>
<td>$25^\circ\text{C}$</td>
<td>0</td>
<td>2</td>
<td>V</td>
<td>dB</td>
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<td></td>
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<td>$T_{\text{MIN}}, T_{\text{MAX}}$</td>
<td></td>
<td>2</td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>GFR</td>
<td>Rolloff (&lt;100 MHz)</td>
<td>$V_{OUT} = 0.4\text{Vpp}$</td>
<td>$25^\circ\text{C}$</td>
<td>0.1</td>
<td>0.5</td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{\text{MIN}}, T_{\text{MAX}}$</td>
<td></td>
<td>0.5</td>
<td>V</td>
<td>dB</td>
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</tr>
</tbody>
</table>
**Closed Loop AC Electrical Characteristics**

\[ V_S = \pm 5V, \ AV = +2, \ RF = RG = 250\Omega, \ CF = 3pF, \ RL = 1000\Omega \] 

unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPD</td>
<td>Linear Phase Deviation ((&lt; 100 \text{ MHz}))</td>
<td>( V_{\text{OUT}} = 0.4 \text{ V}_{\text{PP}} )</td>
<td>All</td>
<td>1</td>
<td>1.8</td>
<td>IV.</td>
<td>°</td>
<td></td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
<td>( AV = +2 )</td>
<td>25°C</td>
<td>50</td>
<td>V</td>
<td>°</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tr1, tf1</td>
<td>Rise Time, Fall Time</td>
<td>0.4V Step, ( AV = +2 )</td>
<td>25°C</td>
<td>1.8</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tr2, tf2</td>
<td>Rise Time, Fall Time</td>
<td>5V Step, ( AV = +2 )</td>
<td>25°C</td>
<td>8</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>ts1</td>
<td>Settling to 0.1% (( AV = -1 ))</td>
<td>2V Step</td>
<td>25°C</td>
<td>13</td>
<td>V</td>
<td>ns</td>
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<tr>
<td>ts2</td>
<td>Settling to 0.01% (( AV = -1 ))</td>
<td>2V Step</td>
<td>25°C</td>
<td>25</td>
<td>V</td>
<td>ns</td>
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<tr>
<td>OS</td>
<td>Overshoot</td>
<td>2V Step</td>
<td>25°C</td>
<td>5</td>
<td>V</td>
<td>%</td>
<td></td>
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<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>2V Step</td>
<td>All</td>
<td>275</td>
<td>400</td>
<td>IV</td>
<td>V/μs</td>
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**DISTORTION** (Note 5)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD2a</td>
<td>2nd Harmonic Distortion</td>
<td>@ 10 MHz, ( AV = +2 )</td>
<td>25°C</td>
<td>-65</td>
<td>-55</td>
<td>V</td>
<td>dBC</td>
</tr>
<tr>
<td>HD2c</td>
<td>2nd Harmonic Distortion</td>
<td>@ 20 MHz, ( AV = +2 )</td>
<td>25°C</td>
<td>-55</td>
<td>-45</td>
<td>V</td>
<td>dBC</td>
</tr>
<tr>
<td>HD3a</td>
<td>3rd Harmonic Distortion</td>
<td>@ 10 MHz, ( AV = +2 )</td>
<td>( T_{\text{MIN}}, T_{\text{MAX}} )</td>
<td>-45</td>
<td>V</td>
<td>dBC</td>
<td></td>
</tr>
<tr>
<td>HD3c</td>
<td>3rd Harmonic Distortion</td>
<td>@ 20 MHz, ( AV = +2 )</td>
<td>25°C</td>
<td>-70</td>
<td>-60</td>
<td>V</td>
<td>dBC</td>
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</table>

**VIDEO PERFORMANCE** (Note 6)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>NTSC</td>
<td>25°C</td>
<td>0.01</td>
<td>0.05</td>
<td>V</td>
<td>%pp</td>
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<tr>
<td>dP</td>
<td>Differential Phase</td>
<td>NTSC</td>
<td>25°C</td>
<td>0.015</td>
<td>0.05</td>
<td>V</td>
<td>°pp</td>
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<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>30 MHz</td>
<td>25°C</td>
<td>0.1</td>
<td>V</td>
<td>%pp</td>
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<tr>
<td>dP</td>
<td>Differential Phase</td>
<td>30 MHz</td>
<td>25°C</td>
<td>0.1</td>
<td>V</td>
<td>°pp</td>
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<tr>
<td>VBW</td>
<td>±0.1 dB Bandwidth Flatness</td>
<td>25°C</td>
<td>25</td>
<td>50</td>
<td>V</td>
<td>MHz</td>
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</tr>
</tbody>
</table>

**Notes:**

1. Measured from \( T_{\text{MIN}}, T_{\text{MAX}} \).
2. \( \pm V_{\text{CC}} = \pm 4.5V \) to 5.5V.
3. \( \pm V_{\text{IN}} = \pm 2.5V, V_{\text{OUT}} = 0V \)

4. Large-signal bandwidth calculated using \( \text{LSBW} = \frac{\text{Slew Rate}}{2\pi \ V_{\text{PEAK}}} \).

5. All distortion measurements are made with \( V_{\text{OUT}} = 2 \text{ V}_{\text{PP}}, RL = 100\Omega \).

6. Video performance measured at \( AV = +2 \) with 2 times normal video level across \( RL = 100\Omega \). This corresponds to standard video levels across a back-terminated 50Ω load, i.e., 0–100 IRE, 40IREpp giving a 1 Vpp video signal across the 50Ω load. For other values of \( RL \), see curves.
Typical Performance Curves \((T_A = 25^\circ C)\)

- **Non-Inverting Frequency Response**
- **Inverting Frequency Response**
- **Frequency Response for Various \(R_L\)**
- **Open Loop Gain and Phase**
- **Output Voltage Swing vs Frequency**
- **Equivalent Input Noise**
- **PSRR, CMRR, and Closed-Loop \(R_Q\) vs Frequency**
- **2nd and 3rd Harmonic Distortion vs Frequency**
- **2-Tone, 3rd Order Intermodulation Intercept**
Typical Performance Curves \( (T_A = 25^\circ C \text{ unless otherwise specified}) - \text{Contd.} \)

**Series Resistor and Resulting Bandwidth vs Capacitive Load**

- Capacitive Load \( (C_L) \) (pF)
- Series Resistance \( (R_S) \) (Ω)
- 3 dB Bandwidth (kHz)

**Settling Time vs Output Voltage Change**

- Output Voltage Change
- Closed-Loop Gain

**Settling Time vs Closed-Loop Gain**

- Closed-Loop Gain (V/V)

**Common-Mode Rejection Ratio vs Input Common-Mode Voltage**

- Input Common-Mode Voltage (V)
- Common-Mode Rejection Ratio (dB)

**Bias and Offset Current vs Input Common-Mode Voltage**

- Input Common-Mode Voltage (V)
- Bias Current (mA)
- Offset Current (μA)

**Supply Current vs Temperature**

- Ambient Temperature (°C)
- Supply Current (mA)

**Bias and Offset Current vs Temperature**

- Ambient Temperature (°C)
- Bias Current (mA)
- Offset Current (μA)

**Offset Voltage vs Temperature**

- Ambient Temperature (°C)
- Offset Voltage (mV)

**AVOL, PSRR, and CMRR vs Temperature**

- Ambient Temperature (°C)
- CMRR
- PSRR
- AVOL
Typical Performance Curves ($T_A = 25^\circ C$) — Contd.

**Small Signal Transient Response**

- $A_0 = +2 \text{ V/V}$
- $R_I = 100\Omega$
- $R_P = R_D = 250\Omega$
- $C_F = 3 \text{ pF}$

**Large Signal Transient Response**

- $A_0 = +2 \text{ V/V}$
- $R_I = 100\Omega$
- $R_P = R_D = 250\Omega$
- $C_F = 3 \text{ pF}$

**Differential Gain and Phase vs DC Input Offset at 3.58 MHz**

- $A_0 = +2$
- $R_I = 100\Omega$
- $V_{IN} = 40\text{ IRE}$ NTSC/50 MHz, swept 100 IRE of $V_{OFFSET}$

**Differential Gain and Phase vs DC Input Offset at 4.43 MHz**

- $A_0 = +2$
- $R_I = 100\Omega$
- $V_{IN} = 40\text{ IRE}$ PAL/50 MHz, swept 100 IRE of $V_{OFFSET}$

**Differential Gain and Phase vs DC Input Offset at 30 MHz**

- $A_0 = +2$
- $R_I = 100\Omega$
- $V_{IN} = 40\text{ IRE}$ 30 MHz, swept 100 IRE of $V_{OFFSET}$

**Differential Gain and Phase vs Number of 150\(\Omega\) Loads at 3.58 MHz**

- $A_0 = +2$
- $R_I = 100\Omega$
- 0 IRE to 100 IRE input stop
- 0 IRE = 0 V

**Differential Gain and Phase vs Number of 150\(\Omega\) Loads at 4.43 MHz**

- $A_0 = +2$
- $R_I = 100\Omega$
- 0 IRE to 100 IRE input stop
- 0 IRE = 0 V

**Differential Gain and Phase vs Number of 150\(\Omega\) Loads at 30 MHz**

- $A_0 = +2$
- $R_I = 100\Omega$
- 0 IRE to 100 IRE input stop
- 0 IRE = 0 V
Equivalent Circuit

Burn-In Circuit

All Packages Use The Same Schematic
Applications Information

Product Description
The EL2074 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2074 uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain $g^2$ where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2074 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2074 is an excellent choice for applications such as log amplifiers.

The EL2074 also has excellent DC specifications: $200 \mu V$, $V_{OS} = 2 \mu A I_{B}$, $0.1 \mu A I_{OS}$, and 90 dB of CMRR. These specifications allow the EL2074 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2074 is only $3.2 \mu A/\sqrt{Hz}$, making it an excellent choice for high-sensitivity trans-impedance amplifier configurations.

Gain-Bandwidth Product
The EL2074 has a gain-bandwidth product of 400 MHz. For gains greater than 8, its closed-loop $-3$ dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 8, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2074 has a $-3$ dB bandwidth of 400 MHz at a gain of +2, dropping to 200 MHz at a gain of +4. It is important to note that the EL2074 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2074 in a gain of +2 only exhibits 1 dB of peaking with a 100$\Omega$ load.

Parasitic Capacitances and Stability
When used in positive-gain configurations, the EL2074 can be quite sensitive to parasitic capacitances at the inverting input, especially with values $\geq 250 \Omega$ for the gain resistor. The problem stems from the feedback and gain resistance in conjunction with the approximately 3pF of board-related parasitic capacitance from the inverting input to ground. Assuming a gain-of-2 configuration with $R_f = R_g = 250\Omega$, a feedback pole occurs at 424 MHz, which is equivalent to a zero in the forward path at the same frequency. This zero reduces stability by reducing the effective phase-margin from about 50° to about 30°.

A common solution to this problem is to add an additional capacitor from the inverting input to the output. This capacitor, in conjunction with the parasitic capacitance, maintains a constant voltage-divider between the output and the inverting input. This technique is used for AC testing of the EL2074. A 3pF capacitor is placed in parallel with the feedback resistor for all AC tests. When this capacitor is used, it is also possible to increase the resistance values of the feedback and gain resistors without loss of stability, resulting in less loading of the EL2074 from the feedback network.

Video Performance
An industry-standard method of measuring the video distortion of a component such as the EL2074 is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 Vpp (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC, 4.43 MHz for PAL, or 30 MHz for HDTV. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.
Applications Information — Contd.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2074 has been designed to be among the best video amplifiers in the marketplace today. It has been thoroughly characterized for video performance in the topology described above, and the results have been included as minimum $d_G$ and $d_P$ specifications and as typical performance curves. In a gain of $+2$, driving 1500Ω, with standard video test levels at the input, the EL2074 exhibits $d_G$ and $d_P$ of only 0.01% and 0.015° at NTSC and PAL. Because $d_G$ and $d_P$ vary with different DC offsets, the superior video performance of the EL2074 has been characterized over the entire DC offset range from $-0.714V$ to $+0.714V$. For more information, refer to the curves of $d_G$ and $d_P$ vs DC Input Offset.

The excellent output drive capability of the EL2074 allows it to drive up to 4 back-terminated loads with excellent video performance. With 4 150Ω loads, $d_G$ and $d_P$ are only 0.15% and 0.08° at NTSC and PAL. For more information, refer to the curves for Video Performance vs Number of 150Ω Loads.

Output Drive Capability

The EL2074 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 Vpp into a 50Ω load. This high output drive capability makes the EL2074 an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2074 remains a minimum of 50 mA at low temperatures. The EL2074 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2074 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor ($R_s$) to isolate the load capacitance from the amplifier output. A curve of recommended $R_s$ vs $C_{load}$ has been included for reference. Values of $R_s$ were chosen to maximize resulting bandwidth without peaking.

Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 µF – 10 µF tantalum capacitor is recommended in parallel with a 0.01 µF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2074 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.
EL2074 Macromodel

* Connections:
  
  .subckt M2074
  
  * Input Stage
  
  ie 37 4 1 mA
  r6 36 37 125
  r7 38 37 125
  rcl 7 30 200
  rc2 7 39 200
  q1 30 3 36 qn
  q2 39 2 38 qna
  ediff 33 0 39 30 1
  rdiff 33 0 1 Meg

  * Compensation Section
  
  ga 0 34 33 0 2m
  rh 34 0 500K
  ch 34 0 0.8 pF
  re 34 40 50
  cc 40 0 0.05 pF

  * Poles
  
  ep 41 0 40 0 1
  rpa 41 42 150
  cpa 42 0 0.5 pF
  rpb 42 43 50
  cpb 43 0 0.5 pF

  * Output Stage
  
  iosl 7 50 3.0 mA
  ies2 51 4 3.0 mA
  q3 4 43 50 qp
  q4 7 43 51 qn
  q5 7 50 52 qn
  q6 4 51 53 qp
  ros1 52 6 2
  ros2 6 53 2

  Power Supply Current
  
  ips 7 4 11.4 mA

  Models
  
  .model qna npn(is=800e-18 bf=170 tf=0.2 ns)
  .model qn npn(is=810e-18 bf=200 tf=0.2 ns)
  .model qp pnp(is=800e-18 bf=200 tf=0.2 ns)
  .ends
EL2074 Macromodel — Contd.
**Features**
- 2 GHz gain-bandwidth product
- Gain-of-10 stable
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%

**Applications**
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

**General Description**
The EL2075 is a precision voltage-feedback amplifier featuring a 2 GHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2075 is gain-of-10 stable with a $-3$ dB bandwidth of 400 MHz at $A_v = +10$. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2075 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2075 the ideal choice for all op-amp applications at a gain of 10 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2075 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document, QRA-1: Elantec’s Processing, Monolithic Integrated Circuits.

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2075CN</td>
<td>0°C to +75°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2075CS</td>
<td>0°C to +75°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

**Connection Diagram**

DIP and SO Package

```
 NC 1
 IN- 2
 IN+ 5
 V- 4

 NC 8
 OUT 6
 V+ 7

 2075-1
```
**Absolute Maximum Ratings** \( (T_A = 25°C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ( (V_S) )</td>
<td></td>
<td>( ±7V )</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>Output Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Common-Mode Input</td>
<td></td>
<td>( ±V_S )</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>pA</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td></td>
<td>( 3V )</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>pF</td>
</tr>
<tr>
<td>Output is short-circuit protec-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>ed to ground, however, maxi-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>mum reliability is obtained if</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>( I_{OUT} ) does not exceed 70 mA.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>Thermal Resistance ( \theta_{JA} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>°C</td>
</tr>
<tr>
<td>Note: See EL2071/EL2171 for Thermal Impedance curves.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

**Open Loop DC Electrical Characteristics**
\( V_S = ±5V, R_L = 1000Ω \), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} ) Input Offset Voltage</td>
<td>( V_{CM} = 0V )</td>
<td></td>
<td>25°C</td>
<td>0.2</td>
<td>1</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( T_{CV_{OS}} ) Average Offset Voltage Drift</td>
<td>( V_{CM} = 0V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( I_B ) Input Bias Current</td>
<td>( V_{CM} = 0V )</td>
<td></td>
<td>25°C</td>
<td>0.1</td>
<td>1</td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( I_{OS} ) Input Offset Current</td>
<td>( V_{CM} = 0V )</td>
<td></td>
<td>25°C</td>
<td>0.2</td>
<td>1</td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( I_S ) Supply Current—Quiescent</td>
<td>No Load</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( R_{IN} ) (diff) ( R_{IN} ) (Differential)</td>
<td>Open-Loop</td>
<td></td>
<td>25°C</td>
<td>15</td>
<td></td>
<td></td>
<td>I</td>
<td>kΩ</td>
</tr>
<tr>
<td>( C_{IN} ) (diff) ( C_{IN} ) (Differential)</td>
<td>Open-Loop</td>
<td></td>
<td>25°C</td>
<td>1</td>
<td></td>
<td></td>
<td>I</td>
<td>pF</td>
</tr>
<tr>
<td>( R_{IN} ) (cm) ( R_{IN} ) (Common-Mode)</td>
<td>Open-Loop</td>
<td></td>
<td>25°C</td>
<td>1</td>
<td></td>
<td></td>
<td>I</td>
<td>MΩ</td>
</tr>
<tr>
<td>( C_{IN} ) (cm) ( C_{IN} ) (Common-Mode)</td>
<td>Open-Loop</td>
<td></td>
<td>25°C</td>
<td>1</td>
<td></td>
<td></td>
<td>I</td>
<td>pF</td>
</tr>
</tbody>
</table>
## Open Loop DC Electrical Characteristics

$V_S = \pm 5V, R_L = 100\Omega$, unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{OUT}$</td>
<td>Output Resistance</td>
<td></td>
<td>25°C</td>
<td>50</td>
<td>V</td>
<td>V</td>
<td>EL2075C</td>
<td>mA</td>
</tr>
<tr>
<td>CMIR</td>
<td>Common-Mode Input Range</td>
<td></td>
<td>25°C</td>
<td>±3</td>
<td>±3.5</td>
<td>IV</td>
<td>EL2075C</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>No Load</td>
<td>All</td>
<td>50</td>
<td>70</td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing</td>
<td>100Ω</td>
<td>All</td>
<td>±3.5</td>
<td>4</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT \ 50}$</td>
<td>Output Voltage Swing</td>
<td>50Ω</td>
<td>All</td>
<td>±2.5</td>
<td>3.4</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$A_{VOL \ 100}$</td>
<td>Open-Loop Gain</td>
<td>100Ω</td>
<td>25°C</td>
<td>1000 2800</td>
<td>III</td>
<td>V/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{VOL \ 50}$</td>
<td>Open-Loop Gain</td>
<td>50Ω</td>
<td>25°C</td>
<td>800 2300</td>
<td>III</td>
<td>V/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$eN@ &gt; 1 \text{ MHz}$</td>
<td>Noise Voltage 1–100 MHz</td>
<td>25°C</td>
<td>2.3</td>
<td>V</td>
<td>nV/\sqrt{Hz}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$iN@ &gt; 100 \text{ kHz}$</td>
<td>Noise Current 100k–100 MHz</td>
<td>25°C</td>
<td>3.2</td>
<td>V</td>
<td>pA/\sqrt{Hz}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Closed Loop AC Electrical Characteristics

$V_S = \pm 5V, A_V = +20, R_f = 15000\Omega, R_L = 100\Omega$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSBW</td>
<td>$-3 \text{ dB Bandwidth}$ ($V_{OUT} = 0.4\text{ Vpp}$)</td>
<td>$A_V = +10$</td>
<td>25°C</td>
<td>400</td>
<td>V</td>
<td>V</td>
<td>EL2075C</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$A_V = +20$</td>
<td>25°C</td>
<td>150 200</td>
<td>V</td>
<td>V</td>
<td>EL2075C</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>125</td>
<td></td>
<td>V</td>
<td>V</td>
<td>EL2075C</td>
<td>MHz</td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain-Bandwidth Product</td>
<td>$A_V = +100$</td>
<td>25°C</td>
<td>2.0</td>
<td>V</td>
<td>V</td>
<td>EL2075C</td>
<td>GHz</td>
</tr>
<tr>
<td>LSBWa</td>
<td>$-3 \text{ dB Bandwidth}$ ($V_{OUT} = 2\text{ Vpp}$ (Note 4))</td>
<td>All 80 128</td>
<td>IV</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LSBWb</td>
<td>$-3 \text{ dB Bandwidth}$ ($V_{OUT} = 5\text{ Vpp}$ (Note 4))</td>
<td>All 32 50</td>
<td>IV</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GFPL</td>
<td>Peaking (&lt;50 MHz) ($V_{OUT} = 0.4\text{ Vpp}$)</td>
<td>25°C</td>
<td>0 0.5</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GFPH</td>
<td>Peaking (&gt;50 MHz) ($V_{OUT} = 0.4\text{ Vpp}$)</td>
<td>25°C</td>
<td>0 1</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>1</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GFR</td>
<td>Rolloff (&lt;100 MHz) ($V_{OUT} = 0.4\text{ Vpp}$)</td>
<td>25°C</td>
<td>0.1 0.5</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Closed Loop AC Electrical Characteristics

\[ V_S = \pm 5V, A_V = +20, R_f = 1500\Omega, R_L = 100\Omega \] unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPD</td>
<td>Linear Phase Deviation (&lt;100 MHz)</td>
<td>(V_{OUT} = 0.4 \text{ Vpp} )</td>
<td>All</td>
<td>1</td>
<td>1.8</td>
<td>IV</td>
<td></td>
<td>°</td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
<td>(A_V = +10 )</td>
<td>25°C</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td>tr1, tf1</td>
<td>Rise Time, Fall Time</td>
<td>0.4V Step, (A_V = +10 )</td>
<td>25°C</td>
<td>1.2</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tr2, tf2</td>
<td>Rise Time, Fall Time</td>
<td>5V Step, (A_V = +10 )</td>
<td>25°C</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>ts1</td>
<td>Settling to 0.1% ((A_V = -20 ))</td>
<td>2V Step</td>
<td>25°C</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>ts2</td>
<td>Settling to 0.01% ((A_V = -20 ))</td>
<td>2V Step</td>
<td>25°C</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>2V Step, (A_V = +10 )</td>
<td>25°C</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>2V Step, (A_V = +10 )</td>
<td>All</td>
<td>500</td>
<td>800</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### DISTORTION (Note 5)

| HD2       | 2nd Harmonic Distortion | @ 20 MHz, \(A_V = +20 \) | 25°C | -40 | -30 | V  | dBC     |
| HD3       | 3rd Harmonic Distortion | @ 20 MHz, \(A_V = +20 \) | 25°C | -65 | -50 | V  | dBC     |

Note 1: Measured from \(T_{MIN}, T_{MAX}\).
Note 2: \(\pm V_{CC} = \pm 4.5V \) to 5.5V.
Note 3: \(\pm V_{IN} = \pm 2.5V, V_{OUT} = 0V\)

Note 4: Large-signal bandwidth calculated using \(LSBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}\)

Note 5: All distortion measurements are made with \(V_{OUT} = 2 \text{ Vpp}, R_L = 100\Omega\).
Typical Performance Curves \((T_A = 25^\circ C)\)

- **Non-Inverting Frequency Response**
- **Inverting Frequency Response**
- **Frequency Response for Various \(R_f\)**
- **Open Loop Gain and Phase**
- **Output Voltage Swing vs Frequency**
- **Equivalent Input Noise**
- **PSRR, CMRR, and Closed-Loop \(R_f\) Frequency**
- **2nd and 3rd Harmonic Distortion vs Frequency**
- **2-Tone, 3rd Order Intermodulation Intercept**
Typical Performance Curves (TA = 25°C unless otherwise specified) — Contd.

- **Series Resistor and Resulting Bandwidth vs Capacitive Load**
- **Settling Time vs Output Voltage Change**
- **Settling Time vs Closed-Loop Gain**
- **Common-Mode Rejection Ratio vs Input Common-Mode Voltage**
- **Bias and Offset Current vs Input Common-Mode Voltage**
- **Supply Current vs Temperature**
- **Bias and Offset Current vs Temperature**
- **Offset Voltage vs Temperature**
- **AVOL, PSRR, and CMRR vs Temperature**
Typical Performance Curves (TA = 25°C) — Contd.

Small Signal Transient Response

Large Signal Transient Response
**Equivalent Circuit**

![Equivalent Circuit Diagram]

**Burn-In Circuit**

![Burn-In Circuit Diagram]

All Packages Use The Same Schematic
Applications Information

Product Description
The EL2075 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2075 uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain $\geq 10$ where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2075 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2075 is an excellent choice for applications such as log amplifiers.

The EL2075 also has excellent DC specifications: $200 \mu V$, $V_{OS}$, $2 \mu A$ $I_B$, $0.1 \mu A$ $I_{OS}$, and $90$ dB of CMRR. These specifications allow the EL2075 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2075 is only $3.2 \mu A/\sqrt{Hz}$, making it an excellent choice for high-sensitivity trans-impedance amplifier configurations.

Gain-Bandwidth Product
The EL2075 has a gain-bandwidth product of $2$ GHz. For gains greater than 40, its closed-loop $-3$ dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 40, higher-order poles in the amplifier’s transfer function contribute to even higher closed loop bandwidths. For example, the EL2075 has a $-3$ dB bandwidth of $400$ MHz at a gain of $+10$, dropping to $200$ MHz at a gain of $+20$. It is important to note that the EL2075 has been designed so that this “extra” bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2075 in a gain of $+10$ only exhibits $1.5$ dB of peaking with a $100 \Omega$ load.

Output Drive Capability
The EL2075 has been optimized to drive $50 \Omega$ and $75 \Omega$ loads. It can easily drive $6 \text{ Vpp}$ into a $50 \Omega$ load. This high output drive capability makes the EL2075 an ideal choice for RF and IF applications. Furthermore, the current drive of the EL2075 remains a minimum of $50$ mA at low temperatures. The EL2075 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads
Although the EL2075 has been optimized to drive resistive loads as low as $50 \Omega$, capacitive loads will decrease the amplifier’s phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than $10 \,\text{pF}$ should be buffered with a series resistor ($R_s$) to isolate the load capacitance from the amplifier output. A curve of recommended $R_s$ vs $C_{load}$ has been included for reference. Values of $R_s$ were chosen to maximize resulting bandwidth without additional peaking.

Printed-Circuit Layout
As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A $1 \,\mu F - 10 \,\mu F$ tantalum capacitor is recommended in parallel with a $0.01 \,\mu F$ ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under $1000 \Omega$ to $2000 \Omega$ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2075 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.
EL2075 Macromodel

* Connections:
* +input
  +Vsupply  -input
  -Vsupply  output
  3  2  7  4  6

.subckt M2075
*
*Input Stage
*
ie 37 4 l mA
r6 36 37 15
r7 38 37 15
rc1 7 30 200
rc2 7 39 200
ql 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 l
rdiff 33 0 1 Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 0.4 pF
rc 34 40 50
cc 40 0 0.05 pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 250
cpa 42 0 0.8 pF
rpb 42 43 50
cpb 43 0 0.5 pF
*
* Output Stage
*
iosl 7 50 3.0 mA
ios2 51 4 3.0 mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
* Power Supply Current
*
ips 7 4 11.4 mA
*
* Models
*
.model qna npn(is=800e-18 bf=170 tf=0.2 ns)
.model qn npn(is=810e-18 bf=200 tf=0.2 ns)
.model qp pnp(is=800e-18 bf=200 tf=0.2 ns)
.ends

2-217
EL2075 Macromodel — Contd.
**Features**

- 50 MHz \(-3\) dB bandwidth, \(A_v = +2\)
- Differential gain 0.03%
- Differential phase 0.05°
- Output short circuit current 800 mA
- Can drive six 75Ω double terminated cables ±11V
- Slew rate = 1000V/μs
- Wide supply voltage range ±5V to ±15V

**Applications**

- Video line driver
- ATE pin driver
- High speed data acquisition

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2099CT</td>
<td>0°C to +75°C</td>
<td>5-Pin</td>
<td>TO-220 MDP0028</td>
</tr>
</tbody>
</table>

**General Description**

The EL2099C is a high speed, monolithic operational amplifier* featuring excellent video performance and high output current capability. Built using Elantec’s Complementary Bipolar process, the EL2099C uses current mode feedback to achieve wide bandwidth, and is stable in unity gain configuration.

Operation from power supplies ranging from ±5V to ±15V makes the EL2099C extremely versatile. With supplies at ±15V, the EL2099C can deliver ±11V into 25Ω at slew rates of 1000V/μs. At ±5V supplies, output voltage range is ±3V into 25Ω. Its speed and output current capability make this device ideal for video line driver and automatic test equipment applications.

Differential Gain and Phase of the EL2099C are 0.03% and 0.05° respectively, and \(-3\) dB bandwidth is 50 MHz. These features make the EL2099C especially well suited for video distribution applications.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec’s processing, see Elantec document, QRA-1: Elantec’s Processing, Monolithic Integrated Circuits.

**Connection Diagram**

![Connection Diagram](image)

EL2099C Video Distribution Amplifier

Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between (V_{S+}) and (V_{S-})</td>
<td>(25^\circ C)</td>
<td>+33V</td>
<td>Internal Power Dissipation</td>
<td>See Curves</td>
<td></td>
</tr>
<tr>
<td>Voltage at (V_{S+})</td>
<td></td>
<td>+16.5V</td>
<td>Operating Ambient Temperature Range</td>
<td>0°C to +75°C</td>
<td></td>
</tr>
<tr>
<td>Voltage at (V_{S-})</td>
<td></td>
<td>−16.5V</td>
<td>Operating Junction Temperature</td>
<td>150°C</td>
<td></td>
</tr>
<tr>
<td>Voltage between (V_{IN+}) and (V_{IN-})</td>
<td></td>
<td>±6V</td>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Current into (V_{IN+}) or (V_{IN-})</td>
<td></td>
<td>±10 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Open Loop DC Electrical Characteristics

\(V_S = \pm 15V, R_L = 25\Omega, T_A = 25^\circ C\) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(25^\circ C)</td>
<td>5</td>
<td>20</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td>25</td>
<td>IV</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{C_{VOS}})</td>
<td>Average Offset Voltage Drift</td>
<td>Full</td>
<td>20</td>
<td>V</td>
<td>(\mu V/\circ C)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(+I_{IN})</td>
<td>+ Input Current</td>
<td>(25^\circ C)</td>
<td>5</td>
<td>20</td>
<td>I</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td>30</td>
<td>IV</td>
<td>(\mu A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(-I_{IN})</td>
<td>− Input Current</td>
<td>(25^\circ C)</td>
<td>8</td>
<td>35</td>
<td>I</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td>50</td>
<td>IV</td>
<td>(\mu A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(CMRR)</td>
<td>Common Mode Rejection Ratio (Note 1)</td>
<td>(25^\circ C)</td>
<td>50</td>
<td>60</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio (Note 2)</td>
<td>(25^\circ C)</td>
<td>60</td>
<td>70</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Transimpedance</td>
<td>(25^\circ C)</td>
<td>85</td>
<td>140</td>
<td>I</td>
<td>k(\Omega)</td>
<td></td>
</tr>
<tr>
<td>(+R_{IN})</td>
<td>+ Input Resistance (Note 3)</td>
<td>(25^\circ C)</td>
<td>700</td>
<td>1000</td>
<td>I</td>
<td>k(\Omega)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{MIN}, T_{MAX})</td>
<td>600</td>
<td>IV</td>
<td>k(\Omega)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(+C_{IN})</td>
<td>+ Input Capacitance</td>
<td>(25^\circ C)</td>
<td>3</td>
<td>V</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(CMIR)</td>
<td>Common Mode Input Range</td>
<td>(25^\circ C)</td>
<td>±12.5</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15V, R_L = 25\Omega, T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing $V_S = \pm 15V$</td>
<td>$25^\circ C$</td>
<td>$\pm 9$</td>
<td>$\pm 11$</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Voltage Swing $V_S = \pm 5V$</td>
<td>$25^\circ C$</td>
<td>$\pm 2.4$</td>
<td>$\pm 3.0$</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>$25^\circ C$</td>
<td>$360$</td>
<td>$440$</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Output Short-Circuit Current</td>
<td>$25^\circ C$</td>
<td>$600$</td>
<td>$800$</td>
<td>$800$</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$25^\circ C$</td>
<td>$32$</td>
<td>$45$</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

### Closed Loop AC Electrical Characteristics

$V_S = \pm 15V, A_V = +2, R_F = 510\Omega, R_L = 25\Omega, T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate (Notes 4, 7)</td>
<td>500</td>
<td>1000</td>
<td></td>
<td>IV</td>
<td>V/μs</td>
</tr>
<tr>
<td>BW</td>
<td>$-3$ dB Bandwidth (Note 7)</td>
<td>50</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Peaking</td>
<td>(Note 7)</td>
<td>0.3</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Rise Time, Fall Time (Notes 5, 7)</td>
<td>7</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain; DC Input Offset from 0V through $+0.714V$, AC Amplitude $286 mV_{pp}, f = 3.58 MHz$ (Notes 6, 7)</td>
<td>0.03</td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase; DC Input Offset from 0V through $+0.714V$, AC Amplitude $286 mV_{pp}, f = 3.58 MHz$ (Notes 6, 7)</td>
<td>0.05</td>
<td></td>
<td>V</td>
<td>deg. (°)</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The input is moved from $-10V$ to $+10V$.
Note 2: The supplies are moved from $\pm 5V$ to $\pm 15V$.
Note 3: $V_{IN} = \pm 5V$. See typical performance curve for larger values of $V_{IN}$.
Note 4: Slew Rate is with $V_{OUT}$ from $+5V$ to $-5V$ and measured at 20% and 80%.
Note 5: Rise and Fall Times are with $V_{OUT}$ between $-0.5V$ and $+0.5V$ and measured at 10% and 90%.
Note 6: See typical performance curves for other conditions.
Note 7: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
Typical Performance Curves \((T_A = 25^\circ C, R_L = 25\Omega, A_V = +2, R_F = 510\) unless otherwise specified)
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_v = +2, R_P = 510 unless otherwise specified) — Contd.

Frequency Response for Various R_P & R_G

Transimpedance (R_{OL})

PSRR & CMRR vs Frequency

Closed-Loop Output Impedance vs Frequency

2nd and 3rd Harmonic Distortion vs Frequency

Voltage and Current Noise vs Frequency
Typical Performance Curves
(T_A = 25°C, R_L = 25Ω, A_v = +2, R_F = 510 unless otherwise specified) — Contd.

1. Supply Current vs Die Temperature
2. Output Voltage vs Die Temperature
3. Transimpedance (R_OI) vs Die Temperature
4. Input Current vs Die Temperature
5. PSRR & CMRR vs Die Temperature
6. Offset Voltage vs Die Temperature (4 Samples)
Typical Performance Curves

$T_A = 25^\circ C$, $R_L = 25\Omega$, $A_v = +2$, $R_F = 510$ unless otherwise specified — Contd.
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified) — Contd.

-3 dB Bandwidth vs R_F

Peaking vs R_F

Overshoot vs R_F

Rise Time vs R_F

5-Lead TO-220 Maximum Power Dissipation vs Ambient Temperature

Small Signal Pulse Response

Large Signal Pulse Response
Simplified Schematic

Burn-In Circuit
Applications Information

Product Description
The EL2099C is a current mode feedback amplifier that has high output current drive capability. It is built using Elantec’s proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The high output current can be useful to drive many standard video loads in parallel, as well as digital sync pulses that are 8V or greater.

+ Input Resistor Value
A small value resistor located in the + Input lead is necessary to keep the EL2099C from oscillating under certain conditions. A 50Ω resistor is recommended for all applications, although smaller values will work under some circumstances. All tests listed in this datasheet are performed with 50Ω in the + Input lead, as well as all typical performance curves. The 50Ω resistor along with the + Input bias current creates an additional typical Offset Voltage of only 250 μV at T = 25°C, and a maximum of 1.25 mV over temperature variations.

Feedback Resistor Values
The EL2099C has been designed and specified with RF = 510Ω and AV = +2. This value of feedback resistor yields extremely flat frequency response with little to no peaking. However, 3 dB bandwidth is reduced somewhat because of this. Wider bandwidth, at the expense of slight peaking, can be accomplished by reducing the value of the feedback resistor. For example, at a gain of +2, reducing the feedback resistor to 330Ω increases the -3 dB bandwidth to 70 MHz with 3 dB of peaking. Inversely, larger values of feedback resistor will cause roll off to occur at a lower frequency. There is essentially no peaking with RF > 510Ω.

Power Supplies
The EL2099C may be operated with single or split supplies as low as ±5V (10V total) to as high as ±18V (36V total). Bandwidth and slew rate are almost constant from Vsy = ±10V to ±18V, and decrease slightly as supplies are reduced to ±5V, as shown in the characteristic curves. It is not necessary to use equal value split supplies. For example, –5V and –12V would be fine for 0V to 1V video signals.

Good power supply bypassing should be used to reduce the risk of oscillation. A 1 μF to 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor is recommended for bypassing each supply pin. They should be kept as close as possible to the device pins.

Due to the internal construction of the TO-220 package, the tab of the EL2099C is connected to the Vsy – pin. Therefore, care must be taken to avoid connecting the tab to the ground plane of the system.

Printed Circuit Board Layout
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input, which is sensitive to stray capacitance. This implies keeping the ground plane away from this pin. Metal film and carbon resistors are both acceptable, while use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

Driving Cables and Capacitive Loads
The EL2099C was designed with driving multiple coaxial cables in mind. With 440 mA of output drive and low output impedance, driving six 75Ω double terminated coaxial cables to ±11V with one EL2099C is practical.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2099C from the capacitive cable and allow extensive capacitive drive. For a discussion on some of the other ways to drive cables, see the application section on driving cables in the EL2003 data sheet.
Applications Information — Contd.
Other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking.

The schematic below shows the EL2099C driving 6 double terminated cables, each of average length of 50 feet.

This represents driving an effective load of 25Ω to over ±10V. The resulting performance is shown in the scope photo. Notice that double termination results in reflection free performance.
EL2099 Macromodel

* Connections: + input
* | - input
* | + Vsupply
* | - Vsupply
* | output
* | .subckt M2099 4 5 1 3 2
*
* Input Stage
* c1 10 0 4 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 5 11 50
l1 11 12 48nH
iinp 4 0 5µA
iinm 5 0 -8µA
*
* Slew Rate Limiting
* h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
* e2 30 0 14 0 0.001667
13 30 17 1.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
* g1 0 18 17 0 1.0
ro1 18 0 150K
cdp 18 0 8pF
*
* Output Stage
* q1 3 18 19 qp
q2 1 18 20 qn
q3 1 19 21 qn
q4 3 20 22 qp
r7 21 2 1
r8 22 2 1
EL2099 Macromodel — Contd.

ios1 1 19 5mA
ios2 20 3 5mA

* Supply Current

ips 13 19mA

* Error Terms

ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 2 0 1.0
e5 25 0 1 0 1.0
e6 26 0 3 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K

* Models

.model qn npn (is = 5e-15  bf = 200  tf = 0.1nS)
.model qp pnp (is = 5e-15  bf = 200  tf = 0.1nS)
.model dclamp d (is = 1e-30  ibv = 0.266  bv = 5  n = 4)
.ends
Features
- Excellent differential gain and phase on ±5V to ±15V supplies
- 100 MHz - 3 dB bandwidth from gains of ±1 to ±10
- 700 V/µs slew rate
- 0.1 dB flatness to 20 MHz
- Output disable in 50 ns - remains high impedance even when driven with large slew rates
- Single +5V supply operation
- AC characteristics are lot and temperature stable
- Available in small SO-8 package

Applications
- Video gain block
- Residue amplifier
- Multiplexer
- Current to voltage converter
- Coax cable driver with gain of 2
- ADC driver

General Description
The EL2120C is a wideband current feedback amplifier optimized for video performance. Its 0.01% differential gain and 0.03 degree differential phase performance when at ±5V supplies exceeds the performance of other amplifiers running on ±15V supplies. Operating on ±8 to ±15V supplies reduces distortions to 0.01% and 0.01 degrees and below. The EL2120C can operate with supplies as low as ±2.5V or a single +5V supply.

Being a current feedback design, bandwidth is a relatively constant 100 MHz over the ±1 to ±10 gain range. The EL2120C has been optimized for flat gain over frequency and all characteristics are maintained at positive unity gain. Because the input slew rate is similar to the 700 V/µs output slew rate the part makes an excellent high-speed buffer.

The EL2120C has a superior output disable function. Time to enable or disable is 50 ns and does not change markedly with temperature. Furthermore, in disable mode the output does not draw excessive currents when driven with 1000 V/µs slew rates. The output appears as a 3 pF load when disabled.

Simplified Schematic

Connection Diagrams

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2120CN</td>
<td>0°C to +75°C</td>
<td>8-Pin P-DIP</td>
<td>MD00031</td>
</tr>
<tr>
<td>EL2120CS</td>
<td>0°C to +75°C</td>
<td>8-Lead SO</td>
<td>MD0027</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings (\(T_A = 25^\circ C\))

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{os})</td>
<td>Input Offset Voltage</td>
<td>Full</td>
<td>4</td>
<td>20</td>
<td>II</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>(V_{os} = \pm 15V)</td>
<td>Full</td>
<td>2</td>
<td>25</td>
<td>II</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{os}/\Delta T)</td>
<td>Input Offset Drift</td>
<td>Full</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu V^\circ C)</td>
</tr>
<tr>
<td>(I_{b+})</td>
<td>+ (V_{IN}) Input Bias Current</td>
<td>Full</td>
<td>5</td>
<td>15</td>
<td>II</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(I_{b-})</td>
<td>- (V_{IN}) Input Bias Current</td>
<td>Full</td>
<td>10</td>
<td>50</td>
<td>II</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection (Note 1)</td>
<td>Full</td>
<td>50</td>
<td>55</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(-ICMR)</td>
<td>- Input Current Common-Mode Rejection (Note 1)</td>
<td>Full</td>
<td>8</td>
<td>20</td>
<td>II</td>
<td>(\mu A/V)</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection (Note 2)</td>
<td>Full</td>
<td>65</td>
<td>80</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>+IPSR</td>
<td>+ Input Current Power Supply Rejection (Note 2)</td>
<td>(25^\circ C)</td>
<td>0.03</td>
<td></td>
<td>V</td>
<td>(\mu A/V)</td>
<td></td>
</tr>
<tr>
<td>-IPSR</td>
<td>- Input Current Power Supply Rejection (Note 2)</td>
<td>Full</td>
<td>0.6</td>
<td>5</td>
<td>II</td>
<td>(\mu A/V)</td>
<td></td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Transimpedance</td>
<td>Full</td>
<td>70</td>
<td>140</td>
<td>II</td>
<td>k(\Omega)</td>
<td></td>
</tr>
<tr>
<td>(A_{VOL})</td>
<td>Voltage Gain</td>
<td>Full</td>
<td>58</td>
<td>66</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>+(R_{IN})</td>
<td>+ (V_{IN}) Input Impedance</td>
<td>(25^\circ C)</td>
<td>2</td>
<td></td>
<td></td>
<td>M(\Omega)</td>
<td></td>
</tr>
</tbody>
</table>

Open Loop DC Electrical Characteristics

\(V_S = \pm 5V; R_L = 1500\, \Omega; T_A = 25^\circ C\) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>(V_{os})</td>
<td>Input Offset Voltage</td>
<td>Full</td>
<td>4</td>
<td>20</td>
<td>II</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>(V_{os} = \pm 15V)</td>
<td>Full</td>
<td>2</td>
<td>25</td>
<td>II</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{os}/\Delta T)</td>
<td>Input Offset Drift</td>
<td>Full</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu V^\circ C)</td>
</tr>
<tr>
<td>(I_{b+})</td>
<td>+ (V_{IN}) Input Bias Current</td>
<td>Full</td>
<td>5</td>
<td>15</td>
<td>II</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(I_{b-})</td>
<td>- (V_{IN}) Input Bias Current</td>
<td>Full</td>
<td>10</td>
<td>50</td>
<td>II</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection (Note 1)</td>
<td>Full</td>
<td>50</td>
<td>55</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(-ICMR)</td>
<td>- Input Current Common-Mode Rejection (Note 1)</td>
<td>Full</td>
<td>8</td>
<td>20</td>
<td>II</td>
<td>(\mu A/V)</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection (Note 2)</td>
<td>Full</td>
<td>65</td>
<td>80</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>+IPSR</td>
<td>+ Input Current Power Supply Rejection (Note 2)</td>
<td>(25^\circ C)</td>
<td>0.03</td>
<td></td>
<td>V</td>
<td>(\mu A/V)</td>
<td></td>
</tr>
<tr>
<td>-IPSR</td>
<td>- Input Current Power Supply Rejection (Note 2)</td>
<td>Full</td>
<td>0.6</td>
<td>5</td>
<td>II</td>
<td>(\mu A/V)</td>
<td></td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Transimpedance</td>
<td>Full</td>
<td>70</td>
<td>140</td>
<td>II</td>
<td>k(\Omega)</td>
<td></td>
</tr>
<tr>
<td>(A_{VOL})</td>
<td>Voltage Gain</td>
<td>Full</td>
<td>58</td>
<td>66</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>+(R_{IN})</td>
<td>+ (V_{IN}) Input Impedance</td>
<td>(25^\circ C)</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
<td>M(\Omega)</td>
</tr>
</tbody>
</table>
### Open Loop DC Electrical Characteristics — Contd.

\( V_S = \pm 5V; R_L = 150\Omega; T_A = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>+ ( V_{IN} ) Range</td>
<td>Full</td>
<td>\pm 3.0</td>
<td>\pm 3.5</td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing</td>
<td>Full</td>
<td>\pm 3.0</td>
<td>\pm 3.5</td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Output Short-Circuit Current</td>
<td>25(^{\circ} C)</td>
<td>100</td>
<td></td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{O,DIS} )</td>
<td>Output Current, Disabled</td>
<td>Full</td>
<td>5</td>
<td>50</td>
<td></td>
<td>II</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{DIS,ON} )</td>
<td>Disable Pin Voltage for Output Enabled</td>
<td>Full</td>
<td>( (V+) - 1 )</td>
<td></td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( V_{DIS,OFF} )</td>
<td>Disable Pin Voltage for Output Disabled</td>
<td>Full</td>
<td>( (V+) - 4 )</td>
<td></td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( I_{DIS,ON} )</td>
<td>Disable Pin Current for Output Enabled</td>
<td>Full</td>
<td>5</td>
<td></td>
<td></td>
<td>II</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{DIS,OFF} )</td>
<td>Disable Pin Current for Output Disabled</td>
<td>Full</td>
<td>1.0</td>
<td></td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{S} )</td>
<td>Supply Current ( (V_S = \pm 15V) )</td>
<td>Full</td>
<td>17</td>
<td>20</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes:
1. The input is moved from \(-3V\) to \(+3V\).
2. The supplies are moved from \(\pm 5V\) to \(\pm 15V\).

### Closed Loop AC Electrical Characteristics

\( V_S = \pm 15V; A_V = \pm 2; R_F = R_G = 270\Omega; R_L = 150\Omega; C_L = 7 \text{ pF}; C_{IN-} = 2 \text{ pF}; T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate; ( V_{OUT} ) from (-3V) to (+3V)</td>
<td>( V_S = \pm 15V )</td>
<td>750</td>
<td></td>
<td>V</td>
<td>( V/\mu s )</td>
</tr>
<tr>
<td></td>
<td>Measured at (-2V) and (+2V)</td>
<td>( V_S = \pm 5V )</td>
<td>550</td>
<td></td>
<td>V</td>
<td>( V/\mu s )</td>
</tr>
<tr>
<td>( t_S )</td>
<td>Settling Time to 0.25% of a</td>
<td>0 to +10V Swing; ( A_V = +1 ) with ( R_F = 270\Omega, R_G = \infty ), and ( R_L = 400\Omega )</td>
<td>50</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>(-3\ dB)</td>
<td>95</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>( \pm 1\ dB)</td>
<td>50</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \pm 0.1\ dB)</td>
<td>16</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td><a href="mailto:BW@2.5V">BW@2.5V</a></td>
<td>Bandwidth at ( V_S = \pm 2.5V )</td>
<td>(-3\ dB)</td>
<td>75</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>( \pm 1\ dB)</td>
<td>35</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \pm 0.1\ dB)</td>
<td>11</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Peaking</td>
<td></td>
<td></td>
<td>0.5</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
</tbody>
</table>
Closed Loop AC Electrical Characteristics — Contd.

\[ V_S = \pm 15V; A_V = +2 \text{ } (R_F = R_G = 270\Omega); R_L = 150\Omega; C_L = 7 \text{ pF}; C_{IN-} = 2 \text{ pF}; T_A = 25^\circ C \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th></th>
<th></th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(dG)</td>
<td>Differential Gain; DC Offset from (-0.7V) through (0.7V), AC Amplitude 286 mVp–p</td>
<td>(V_S = \pm 15V, f = 3.58 MHz)</td>
<td>(&lt;0.01)</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 15V, f = 30 MHz)</td>
<td>0.1</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5V, f = 3.58 MHz)</td>
<td>0.01</td>
<td>V</td>
<td>%</td>
</tr>
</tbody>
</table>

| \(d\theta\) | Differential Phase; DC Offset from \(-0.7V\) through \(0.7V\), AC Amplitude 286 mVp–p | \(V_S = \pm 15V, f = 3.58 MHz\) | 0.01 | V | ° |
| | | \(V_S = \pm 15V, f = 30 MHz\) | 0.1 | V | ° |
| | | \(V_S = \pm 5V, f = 3.58 MHz\) | 0.06 | V | ° |

Typical Performance Curves

![Typical Performance Curves Diagram](image)

2120-3

2-236
Typical Performance Curves — Contd.

Gain Flatness vs \( R_F \)

\[
\begin{align*}
&\text{Gain (dB)} \\
&6.4 \quad 6.3 \quad 6.2 \quad 6.1 \quad 6.0 \quad 5.9 \quad 5.8 \quad 5.7 \quad 5.6 \\
&\text{FREQUENCY (Hz)} \\
&1M \quad 10M \quad 100M
\end{align*}
\]

-3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at \( V_S \pm 15V \)

\[
\begin{align*}
&\text{3 dB BANDWIDTH} \\
&(0.1 dB BANDWIDTH (MHz)) \\
&(6)70 \\
&DIE TEMPERATURE (°C)
\end{align*}
\]

Gain Flatness vs \( C_{IN} \)

\[
\begin{align*}
&\text{Gain (dB)} \\
&6.7 \quad 6.6 \quad 6.5 \quad 6.4 \quad 6.3 \quad 6.2 \quad 6.1 \\
&\text{FREQUENCY (Hz)} \\
&1M \quad 10M \quad 100M
\end{align*}
\]

-3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at \( V_S \pm 15V \)

\[
\begin{align*}
&\text{3 dB BANDWIDTH} \\
&(0.1 dB BANDWIDTH (MHz)) \\
&(6)70 \\
&DIE TEMPERATURE (°C)
\end{align*}
\]

Deviation From Linear Phase vs Frequency

\[
\begin{align*}
&\text{Deviation From Linear Phase (°)} \\
&100K \quad 1M \quad 10M \quad 100M \\
&\text{FREQUENCY (Hz)}
\end{align*}
\]

\( T_{\text{delay}} = 3.63 \text{ nsec} \)
Typical Performance Curves — Contd.

Differential Gain vs DC Input Offset at 3.58 MHz

Differential Phase vs DC Input Offset at 3.58 MHz

Differential Gain vs DC Input Offset at 30 MHz

Differential Phase vs DC Input Offset at 30 MHz

Differential Gain and Phase vs Supply Voltage (VIN: DC from 0 to +0.7V)

Input Noise Voltage and Current

- $A_v = +2$
- $R_o = R_p = 270\,\Omega$
- $R_i = 150\,\Omega$
- $V_o = \pm 5\,V$
- $V_o = \pm 15\,V$
- $V = \pm 5\,V$
- $V = \pm 9\,V$
- $V = \pm 15\,V$

DC INPUT VOLTAGE (V)

DC INPUT VOLTAGE (V)

DC INPUT VOLTAGE (V)

DC INPUT VOLTAGE (V)

DC INPUT VOLTAGE (V)

SUPPLY VOLTAGE (V)

INPUT NOISE VOLTAGE OR CURRENT (V/\sqrt{Hz} or \mu A/\mu V)

FREQUENCY (Hz)
Typical Performance Curves — Contd.

Undistorted Output Swing vs Frequency

- $V_S = \pm 15V, R_F = 1K\Omega$
- $V_S = \pm 15V, R_F = 2700\Omega, R_L = 150\Omega$
- $V_S = \pm 9V, R_F = 150\Omega$
- $V_S = \pm 5V, R_F = 150\Omega$
- $V_S = \pm 2.5V, R_F = 150\Omega$

Frequency (Hz)

Slew Rate vs Temperature

- $V_S = \pm 15V$
- $V_S = \pm 9V$
- $V_S = \pm 5V$

Temperature (°C)

Small-Signal Transient Response

- $A_V = \pm 2, R_P = R_G = 270\Omega,$
- $R_L = 150\Omega$

Large-Signal Transient Response

- $A_V = \pm 2, R_P = R_G = 270\Omega,$
- $R_L = 150\Omega, V_S = \pm 15V$

Settling Time vs Swing

- $A_V = \pm 1$
- $R_P = 270\Omega$
- $R_L = 400\Omega$
- $Q_L = 20\text{ pF}$

Output Swing (V)

Settling Time (nsec)

Long Term Settling Error

- $\Delta V = \pm 10V$
- $A_V = \pm 1$
- $R_P = 270\Omega$
- $R_L = 400\Omega$
- $V_S = \pm 15V$

Residual Settling Error (%)

Time (µsec)
Typical Performance Curves — Contd.

Enable Response for a Family of Inputs

\[ AV = +2, \quad RL = 150\Omega, \quad VS = \pm 5V \]

Disable Response for a Family of Inputs

\[ AV = +2, \quad RL = 150\Omega, \quad VS = \pm 5V \]

Supply Current vs Supply Voltage

8-Lead SO Maximum Power Dissipation vs Ambient Temperature
Applications Information

The EL2120C represents the third generation of current-feedback amplifier design. It is designed to provide good high-frequency performance over wide supply voltage, load impedance, gain, temperature, and manufacturing lot variations. It is a well-behaved amplifier in spite of its 100 MHz bandwidth, but a few precautions should be taken to obtain maximum performance.

The power supply pins must be well bypassed. 0.01 µF ceramic capacitors are adequate, but lead length should be kept below 1/4" and a ground plane is recommended. Bypassing with 4.7 µF tantalum capacitors can improve settling characteristics, and smaller capacitors in parallel will not be needed. The lead length of sockets generally deteriorates the amplifier's frequency response by exaggerating peaking and increasing ringing in response to transients. Short sockets cause little degradation.

Load capacitance also increases ringing and peaking. Capacitance greater than 35 pF should be isolated with a series resistor. Capacitance at the VIN− terminal has a similar effect, and should be kept below 5 pF. Often, the inductance of the leads of a load capacitance will be self-resonant at frequencies from 40 MHz to 200 MHz and can cause oscillations. A resonant load can be de-Q'ed with a small series or parallel resistor. A "snubber" can sometimes be used to reduce resonances. This is a resistor and capacitor in series connected from output to ground. Values of 68Ω and 33 pF are typical. Increasing the feedback resistor can also improve frequency flatness.

The VIN+ pin can oscillate in the 200 MHz to 500 MHz realm if presented with a resonant or inductive source impedance. A series 27Ω to 68Ω resistor right on the VIN+ pin will suppress such oscillations without affecting frequency response.

−3 dB bandwidth is inversely proportional to the value of feedback resistor $R_F$. The EL2120C will tolerate values as low as 180Ω for a maximum bandwidth of about 140 MHz, but peaking will increase and tolerance to stray capacitance will reduce. At gains greater than 5, −3 dB bandwidth begins to reduce, and a smaller $R_F$ can be used to maximize frequency response.

The greatest frequency response flatness (to 0.1 dB, for instance) occurs with $R_F = 300Ω$ to 330Ω. Even the moderate peaking caused by lower values of $R_F$ will cause the gain to peak out of the 0.1 dB window, and higher values of $R_F$ will cause an overcompensated response where the gain falls below the 0.1 dB level. Parasitic capacitances will generally degrade the frequency flatness.

The EL2120C should not output a continuous current above 50 mA, as stated in the ABSOLUTE MAXIMUM RATINGS table. The output current limit is set to 120 mA at a die temperature of 25°C and reduces to 85 mA at a die temperature of 150°C. This large current is needed to slew load capacitance and drive low impedance loads with low distortion but cannot be supported continuously. Furthermore, package dissipation capabilities cannot be met under short-circuit conditions. Current limit should not occur longer than a few seconds.

The /Disable pin logic level is referred to V+. With ±5V supplies, a CMOS or TTL driver with pull-up resistor will suffice. ±15V supplies require a +14/+11V drive span, or +15/+10V nominally. Open-collector TTL with a tapped pull-up resistor can provide these spans. The impedance of the divider should be 1k or less for optimum enable/disable speed.

The EL2120C enables in 50 ns or less. When $V_{IN} = 0$, only a small switching glitch occurs at the output. When $V_{IN}$ is some other value, the output overshoots by about 0.7V when settling toward its new enabled value.
Applications Information — Contd.
When the EL2120C disables, it turns off very rapidly for inputs of ±1V or less, and the output sags more slowly for inputs larger than this. For inputs as large as ±2.5V the output current can be absorbed by another EL2120C simultaneously enabled. Under these conditions, switching will be properly completed in 50 ns or less.

The greater thermal resistance of the SO-8 package requires that the EL2120C be operated from ±10V supplies or less to maintain the 150°C maximum die temperature over the commercial temperature range. The P-DIP package allows the full ±16.5V supply operation.

Typical Applications Circuit—A High Quality Two-Input Multiplexer
The EL2120C Macromodel
This macromodel has been developed to assist the user in simulating the EL2120C with surrounding circuitry. It was developed for the PSPICE simulator (copyrighted by the Microsim corporation), and may need to be rearranged for other simulators, particularly the H operator. It approximates frequency response and small-signal transients as well, although the effects of load capacitance does not show. This model is slightly more complicated than the models used for low-frequency op-amps, but is much more accurate for AC.

The model does not simulate these characteristics accurately:
- noise
- slew rate limitations
- temperature effects
- settling time
- non-linearities
- manufacturing variations
- input or output resonances
- CMRR and PSRR

* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting

* Connections:  + input  - input
  + | - | input
  + | - | Vsupply
  + | - | -Vsupply
  + | - | output

.subckt M2120 3 2 7 4 6

* Input Stage
* e1 10 0 3 0 1.0
  vis 10 9 0V
  h2 9 12 vxx 1.0
  r1 2 11 25
  l1 11 12 20nH
  iinp 3 0 10j tA
  innm 2 0 5j tA
  r12 3 0 2Meg

* Slew Rate Limiting
* h1 13 0 0 vi 600
  r2 13 14 1K
  d1 14 0 dclamp
  s2 0 14 dclamp

* High Frequency Pole
* e2 30 0 14 0 0.00166666666
  15 30 17 μH
  c5 17 0 0.5pF
  r5 17 0 600

* Transimpedance Stage
* g1 0 18 17 0 1.0
  rol 18 0 140K
  cdp 18 0 7.9pF

* Output Stage

.models qn npn (is = 5e-15 bf= 500 tf= 0.1nS)
.models qp pnp (is = 5e-15 bf= 500 tf= 0.1nS)
.models dclamp d(is = 1e-30 ibv = 0.02 bv = 4 n = 4)
.ends
The EL2120C Macromodel — Contd.
Features
- 3 dB bandwidth = 85 MHz, Av = 1
- 3 dB bandwidth = 75 MHz, Av = 2
- NTSC/PAL dG ≤ 0.03%, dP ≤ 0.1°
- 50 mA output current
- Drives ±2.5V into 100Ω load
- Low voltage noise = 4 nV/√Hz
- Current mode feedback
- Low cost

Applications
- Video amplifier
- Video distribution amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coaxial cable driver

General Description
The EL2130 is a wideband current mode feedback amplifier optimized for gains between -10 and +10 while operating on ±5V power supplies. Built using Elantec’s Complementary Bipolar process, this device exhibits -3 dB bandwidths in excess of 85 MHz at unity gain and 75 MHz at a gain of two. The EL2130 is capable of output currents in excess of 50 mA giving it the ability to drive either double or single terminated 50Ω coaxial cables.

Exhibiting a Differential Gain of 0.03% and a Differential Phase of 0.1° at NTSC and PAL frequencies. The EL2130 is an excellent low cost solution to most video applications.

In addition, the EL2130 exhibits very low gain peaking, typically below 0.1 dB to frequencies in excess of 40 MHz as well as 50 ns settling time to 0.2% making it an excellent choice for driving flash A/D converters.

The device is available in the plastic 8-lead narrow-body small outline (SO) and the 8-pin mini DIP packages, and operates over the temperature range of 0°C to +75°C.

Connection Diagram

Manufactured under U.S. Patent No. 4,893,091.
**EL2130C**  
*85 MHz Current Feedback Amplifier*

### Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_S)</td>
<td>Supply Voltage</td>
<td></td>
<td>±6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Input Voltage</td>
<td></td>
<td>±6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{IN})</td>
<td>Differential Input Voltage</td>
<td></td>
<td>±6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(P_D)</td>
<td>Maximum Power Dissipation</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{IN})</td>
<td>Input Current</td>
<td></td>
<td>±10mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:** All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

### Test Procedures

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25°C) and QA sample tested at (T_A = 25°C).</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25°C) for information purposes only.</td>
</tr>
</tbody>
</table>

### Open Loop DC Electrical Characteristics \(V_S = \pm 5V; R_L = \infty\), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td></td>
<td></td>
<td>2.0</td>
<td>10</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(\Delta V_{OS}/\Delta T)</td>
<td>Offset Voltage Drift</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>III</td>
<td>mV/°C</td>
</tr>
<tr>
<td>(+ I_{IN})</td>
<td>+ Input Current</td>
<td></td>
<td></td>
<td>5.5</td>
<td>15</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>(- I_{IN})</td>
<td>+ Input Current</td>
<td></td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>III</td>
<td>μA</td>
</tr>
<tr>
<td>(+ R_{IN})</td>
<td>+ Input Resistance</td>
<td></td>
<td></td>
<td>1.0</td>
<td>2.0</td>
<td></td>
<td>I</td>
<td>MΩ</td>
</tr>
<tr>
<td>(C_{IN})</td>
<td>+ Input Capacitance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>(V_{CM} = \pm 2.5V)</td>
<td></td>
<td>50</td>
<td>60</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(- ICMR)</td>
<td>Input Current Common Mode Rejection</td>
<td>(V_{CM} = \pm 2.5V)</td>
<td></td>
<td>5</td>
<td>10</td>
<td></td>
<td>I</td>
<td>μA/V</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>(\pm 4.5V \leq V_S \leq \pm 6V)</td>
<td></td>
<td>60</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(+ IPSR)</td>
<td>+ Input Current Power Supply Rejection</td>
<td>(\pm 4.5V \leq V_S \leq \pm 6V)</td>
<td></td>
<td>0.1</td>
<td>0.5</td>
<td></td>
<td>I</td>
<td>μA/V</td>
</tr>
<tr>
<td>(- IPSR)</td>
<td>- Input Current Power Supply Rejection</td>
<td>(\pm 4.5V \leq V_S \leq \pm 6V)</td>
<td></td>
<td>0.5</td>
<td>5.0</td>
<td></td>
<td>I</td>
<td>μA/V</td>
</tr>
</tbody>
</table>
Open Loop DC Electrical Characteristics

\( V_S = \pm 5V; R_L = \infty \), unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{OL} )</td>
<td>Transimpedance</td>
<td>( V_{OUT} = \pm 2.5V, R_L = 100\Omega )</td>
<td>25°C</td>
<td>80</td>
<td>145</td>
<td></td>
<td>I</td>
<td>V/mA</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Open Loop DC Voltage Gain</td>
<td>( V_{OUT} = \pm 2.5V, R_L = 100\Omega )</td>
<td>25°C</td>
<td>60</td>
<td>66</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing</td>
<td>( R_L = 100\Omega )</td>
<td>25°C</td>
<td>3</td>
<td>3.5</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output Current</td>
<td></td>
<td>25°C</td>
<td>30</td>
<td>50</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>Output Resistance</td>
<td></td>
<td>25°C</td>
<td>5</td>
<td></td>
<td></td>
<td>V</td>
<td>Ω</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Quiescent Supply Current</td>
<td></td>
<td>Full</td>
<td>17</td>
<td>21</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Short Circuit Current</td>
<td></td>
<td>25°C</td>
<td>85</td>
<td></td>
<td></td>
<td>V</td>
<td>mA</td>
</tr>
</tbody>
</table>

Closed Loop AC Electrical Characteristics

\( V_S = \pm 5V, A_V = +2, R_F = R_G = 820\Omega, R_L = 100\Omega, T_A = 25°C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( SR )</td>
<td>Slew Rate (Note 1)</td>
<td>( V_O = 5\ V_{p-p} )</td>
<td>625</td>
<td></td>
<td></td>
<td>V</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Rise Time</td>
<td>( V_O = 200\ mV )</td>
<td>4.6</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Fall Time</td>
<td>( V_O = 200\ mV )</td>
<td>4.6</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{pd} )</td>
<td>Prop Delay</td>
<td>( V_O = 200\ mV )</td>
<td>4.0</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( SSBW )</td>
<td>3 dB Bandwidth</td>
<td>( V_O = 100\ mV )</td>
<td>75</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>( dG )</td>
<td>NTSC/PAL Diff Gain</td>
<td></td>
<td>0.03</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>( dP )</td>
<td>NTSC/PAL Diff Phase</td>
<td></td>
<td>0.10</td>
<td></td>
<td></td>
<td>V</td>
<td>deg (°)</td>
</tr>
<tr>
<td>( GFPL )</td>
<td>Gain Flatness</td>
<td>( f &lt; 40\ MHz )</td>
<td>0.08</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
</tbody>
</table>

Note 1: Slew rate is measured with \( V_O = 5V_{p-p} \) between \(-1.25V \) and \(+1.25V \) and \(+1.25V \) and \(-1.25V \).
**Typical Performance Curves**

- **Normalized Offset Voltage vs Temperature**
- **Equivalent Input Noise**
- **Common Mode Rejection Ratio vs Frequency**
- **Power Supply Rejection Ratio vs Frequency**
- **Power Supply Rejection Ratio vs Temperature**
- **Input Bias Current vs Temperature**
- **Input Bias Current vs Frequency**
- **Common Mode Rejection Ratio vs Temperature**
- **Power Supply Rejection Ratio vs Temperature**
Typical Performance Curves — Contd.

### Supply Current vs Temperature

- Supply Current (mA) vs Temperature (°C)
- Temperature range: 0 to 100°C
- Supply current varies with temperature.

### + Input Bias Current vs Temperature

- + Input Bias Current (µA) vs Temperature (°C)
- Temperature range: 0 to 100°C
- + Input bias current decreases with temperature.

### Power Supply Rejection Ratio vs Temperature

- Power Supply Rejection Ratio vs Temperature (°C)
- Temperature range: 0 to 100°C
- PSRR remains constant with temperature.

### Transimpedance (R_O) vs Temperature

- Transimpedance (V/A) vs Temperature (°C)
- Temperature range: 0 to 100°C
- Transimpedance decreases with temperature.

### Open Loop Gain vs Temperature

- Open Loop Gain (dB) vs Temperature (°C)
- Temperature range: 0 to 100°C
- Open loop gain remains constant with temperature.

### Frequency Response

- Frequency Response vs Temperature (°C)
- Frequency range: 10k to 100M Hz
- Gain (dB) varies with frequency and temperature.

### Output Voltage vs Temperature

- Output Voltage (V) vs Temperature (°C)
- Temperature range: 0 to 100°C
- Output voltage varies with temperature.

### Short Circuit Current vs Temperature

- Short Circuit Current (mA) vs Temperature (°C)
- Temperature range: 0 to 100°C
- Short circuit current increases with temperature.
Typical Performance Curves — Contd.

Large Signal Response

\[ AV = +1, \quad RF = 820\Omega \]
\[ RL = 100\Omega, \quad CL = 12 \text{ pF} \]

Large Signal Response

\[ AV = +2, \quad RF = 820\Omega \]
\[ RL = 100\Omega, \quad CL = 12 \text{ pF} \]

Small Signal Response

\[ AV = +1, \quad RF = 820\Omega \]
\[ RL = 100\Omega, \quad CL = 12 \text{ pF} \]

Small Signal Response

\[ AV = +2, \quad RF = 820\Omega \]
\[ RL = 100\Omega, \quad CL = 12 \text{ pF} \]
Applications Information

Power Supply Bypassing
The EL2130 will exhibit ringing or oscillation if the power supply leads are not adequately bypassed. 0.1 \( \mu F \) ceramic disc capacitors are suggested for both supply pins at a distance no greater than \( \frac{1}{2} \) inch from the device. Surface mounting chip capacitors are strongly recommended.

Lead Dress
A ground plane to which decoupling capacitors and gain setting resistors are terminated will eliminate overshoot and ringing. However, the ground plane should not extend to the vicinity of both the non-inverting and inverting inputs (pins 3 and 2) which would add capacitance to these nodes, and lead lengths from these pins should be made as short as possible.

Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Video Characteristics and Applications
Frequency domain testing is performed at Elantec using a computer controlled HP model 8656B Signal Generator and an HP Model 4195A Network/Spectrum Analyzer. The DUT test board is built using microwave/strip line techniques, and solid coaxial cables route the stimulus to the DUT socket. Signals are routed to and from the DUT test fixture using subminiature coaxial cable.

Differential Gain and Phase are tested at a noise gain of 2 with 100\( \Omega \) load. Gain and Phase measurements are made with a DC input reference.
Applications Information — Contd.
voltage at 0V and compared to those made at \( V_{\text{ref}} \) equal to 0.7V at frequencies extending to 30 MHz.

The EL2130 is capable of driving 100Ω to a minimum of 2.5V peak which means that it can naturally drive double terminated (50Ω) coaxial cables.

Capacitive Loads
As can be seen from the Bode plot, the EL2130 will peak into capacitive loads greater than 20 pf. In many applications such as flash A/D's, capacitive loading is unavoidable. In these cases, the use of a snubber network consisting of a 100Ω resistor in series with 47 pF capacitor from the output to ground is recommended.

Equivalent Circuit

AC Test Circuit
Features

- Specified for +3V, +5V, or ±5V Applications
- Power Down to 0 μA (EL2157C)
- Output Voltage Clamp (EL2157C)
- Large Input Common Mode Range
  0V < V<CM < Vs - 1.2V
- Output Swings to Ground Without Saturating
- −3 dB Bandwidth = 125 MHz
- ±0.1 dB Bandwidth = 30 MHz
- Low Supply Current = 5 mA
- Slew Rate = 275 V/μs
- Low Offset Voltage = 2 mV max
  (PDIP and SO Packages)
- Output Current = ±100 mA
- High Open Loop Gain = 80 dB
- Differential Gain = 0.05%
- Differential Phase = 0.05°

Applications

- Video Amplifier
- PCMCIA Applications
- A/D Driver
- Line Driver
- Portable Computers
- High Speed Communications
- RGB Applications
- Broadcast Equipment
- Active Filtering

General Description

The EL2150C/EL2157C are the electronics industry’s fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates ¼ that of the EL2150C/EL2157C. The 125 MHz bandwidth, 275 V/μs slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, this amplifier can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V, making it ideal for portable, low power applications.

The EL2157C has a high speed disable feature. Applying a low logic level to this pin reduces the supply current to 0 μA within 50 ns. This is useful for both multiplexing and reducing power consumption.

The EL2157C also has an output voltage clamp feature. This clamp is a fast recovery (~7 ns) output clamp that prevents the output voltage from going above the preset clamp voltage. This feature is desirable for A/D applications, as A/D converters can require long times to recover if overdriven.

For applications where board space is critical the EL2150C is available in the tiny 5 lead SOT23 package, which has a footprint 28% the size of an 8 lead SOIC. The EL2150C/EL2157C are also both available in 8 pin plastic DIP and SOIC packages. All parts operate over the industrial temperature range of −40°C to +85°C. For dual, triple, or quad applications, contact the factory.

Connection Diagrams

<table>
<thead>
<tr>
<th>Connection Diagrams</th>
<th>EL2150C</th>
<th>EL2157C</th>
<th>EL2150C</th>
</tr>
</thead>
<tbody>
<tr>
<td>SO, P-DIP</td>
<td>Top View</td>
<td>Top View</td>
<td>Top View</td>
</tr>
<tr>
<td></td>
<td>2150-1</td>
<td>2150-2</td>
<td>2150-3</td>
</tr>
</tbody>
</table>

*See Ordering Information section of databook.
### Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage between (V_{S+}) and GND</td>
<td>(+12.6)V</td>
</tr>
<tr>
<td>Input Voltage ((IN+), (IN-), ENABLE, CLAMP)</td>
<td>GND - 0.3V, (V_{S+}) + 0.3V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±6V</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>90 mA</td>
</tr>
<tr>
<td>Output Short Circuit Duration</td>
<td>(note 1)</td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

### Test Levels and Test Procedures
- **I** 100% production tested and QA sample tested per QA test plan QCX0002.
- **II** 100% production tested at \(T_A = 25°C\) and QA sample tested at \(T_A = 25°C\), \(T_{MAX}\) and \(T_{MIN}\) per QA test plan QCX0002.
- **III** QA sample tested per QA test plan QCX0002.
- **IV** Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V** Parameter is typical value at \(T_A = 25°C\) for information purposes only.

### DC Electrical Characteristics

(Note 2) \(V_S = +5V, GND = 0V, T_A = 25°C, V_{CM} = 1.5V, V_{OUT} = 1.5V, V_{CLAMP} = +5V, V_{ENABLE} = +5V\), unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Offset Voltage</td>
<td>PDIP and SOIC Packages</td>
<td>-2</td>
<td>2</td>
<td>-</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SOT23-5 Package</td>
<td>-3</td>
<td>3</td>
<td>-</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(TCV_{OS})</td>
<td>Offset Voltage Temperature Coefficient</td>
<td>Measured from (T_{MIN}) to (T_{MAX})</td>
<td>10</td>
<td>V</td>
<td>(V/°C)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{B})</td>
<td>Input Bias Current</td>
<td>(V_{IN} = 0V)</td>
<td>-5.5</td>
<td>-10</td>
<td>-</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input Offset Current</td>
<td>(V_{IN} = 0V)</td>
<td>-750</td>
<td>150</td>
<td>750</td>
<td>I</td>
<td>nA</td>
</tr>
<tr>
<td>(TCI_{OS})</td>
<td>Input Bias Current Temperature Coefficient</td>
<td>Measured from (T_{MIN}) to (T_{MAX})</td>
<td>50</td>
<td>V</td>
<td>(nA/°C)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td>(V_S = V_{ENABLE} = +2.7V) to (+12V, V_{CLAMP} = OPEN)</td>
<td>55</td>
<td>70</td>
<td>-</td>
<td>I</td>
<td>(dB)</td>
</tr>
<tr>
<td>(CMRR)</td>
<td>Common Mode Rejection Ratio</td>
<td>(V_{CM} = 0V) to (+3.8V)</td>
<td>55</td>
<td>65</td>
<td>-</td>
<td>I</td>
<td>(dB)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{CM} = 0V) to (+3.0V)</td>
<td>55</td>
<td>70</td>
<td>-</td>
<td>I</td>
<td>(dB)</td>
</tr>
<tr>
<td>(CMIR)</td>
<td>Common Mode Input Range</td>
<td>-</td>
<td>0</td>
<td>(V_{S} = 1.2)</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>(R_{IN})</td>
<td>Input Resistance</td>
<td>Common Mode</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>I</td>
<td>(M\Omega)</td>
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<tr>
<td>(C_{IN})</td>
<td>Input Capacitance</td>
<td>SOIC Package</td>
<td>1</td>
<td>V</td>
<td>(\mu F)</td>
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<td></td>
<td></td>
<td>PDIP Package</td>
<td>1.5</td>
<td>V</td>
<td>(\mu F)</td>
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<tr>
<td>(R_{OUT})</td>
<td>Output Resistance</td>
<td>(A_{V} = +1)</td>
<td>40</td>
<td>V</td>
<td>(m\Omega)</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>(I_{S,ON})</td>
<td>Supply Current—Enabled</td>
<td>(V_S = V_{CLAMP} = +12V, V_{ENABLE} = +12V)</td>
<td>5</td>
<td>6.5</td>
<td>-</td>
<td>I</td>
<td>(mA)</td>
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<tr>
<td>(I_{S,OFF})</td>
<td>Supply Current—Shut Down</td>
<td>(V_S = V_{CLAMP} = +10V, V_{ENABLE} = +0.5V)</td>
<td>0</td>
<td>50</td>
<td>-</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = V_{CLAMP} = +12V, V_{ENABLE} = +0.5V)</td>
<td>5</td>
<td>V</td>
<td>(\mu A)</td>
<td>I</td>
<td></td>
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<tr>
<td>(PSOR)</td>
<td>Power Supply Operating Range</td>
<td>-</td>
<td>2.7</td>
<td>12.0</td>
<td>-</td>
<td>I</td>
<td>(V)</td>
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</table>
DC Electrical Characteristics — Contd.
(Note 2) \( V_S = +5V, \ GND = 0V, \ T_A = 25^\circ C, \ V_{CM} = +1.5V, \ V_{OUT} = +1.5V, \ V_{CLAMP} = +5V, \ V_{ENABLE} = +5V, \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>PSOR</td>
<td>Power Supply Operating Range</td>
<td></td>
<td>2.7</td>
<td>12.0</td>
<td>I</td>
<td>V</td>
<td></td>
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<tr>
<td>AVOL</td>
<td>Open Loop Gain</td>
<td>( V_S = V_{CLAMP} = +12V, \ V_{OUT} = +2V to +9V, \ R_L = 1 \text{k}\Omega ) to GND</td>
<td>65</td>
<td>80</td>
<td>I</td>
<td>dB</td>
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<td></td>
<td></td>
<td>( V_{OUT} = +1.5V ) to +3.5V,</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td>( R_L = 1 \text{k}\Omega ) to GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = +1.5V ) to +3.5V,</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 150\Omega ) to GND</td>
<td></td>
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<td></td>
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<tr>
<td>( V_{OP} )</td>
<td>Positive Output Voltage Swing</td>
<td>( V_S = +12V, \ A_V = +1, \ R_L = 1 \text{k}\Omega ) to 0V</td>
<td>10.8</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +12V, \ A_V = +1, \ R_L = 150\Omega ) to 0V</td>
<td>9.6</td>
<td>10.0</td>
<td></td>
<td>V</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, \ A_V = +1, \ R_L = 1 \text{k}\Omega ) to 0V</td>
<td>4.0</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, \ A_V = +1, \ R_L = 150\Omega ) to 0V</td>
<td>3.4</td>
<td>3.8</td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +3V, \ A_V = +1, \ R_L = 150\Omega ) to 0V</td>
<td>1.8</td>
<td>1.95</td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ON} )</td>
<td>Negative Output Voltage Swing</td>
<td>( V_S = +12V, \ A_V = +1, \ R_L = 150\Omega ) to 0V</td>
<td>5.5</td>
<td>8</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, \ A_V = +1, \ R_L = 1 \text{k}\Omega ) to 0V</td>
<td>-4.0</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, \ A_V = +1, \ R_L = 150\Omega ) to 0V</td>
<td>-3.7</td>
<td>-3.4</td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output Current (Note 1)</td>
<td>( V_S = \pm 5V, \ A_V = +1, \ R_L = 10\Omega ) to 0V</td>
<td>±75</td>
<td>100</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, \ A_V = +1, \ R_L = 50\Omega ) to 0V</td>
<td>±60</td>
<td></td>
<td></td>
<td>V</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OUT, OFF} )</td>
<td>Output Current, Disabled</td>
<td>( V_{ENABLE} = +0.5V )</td>
<td>0</td>
<td>20</td>
<td></td>
<td>I</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( V_{IH-EN} )</td>
<td>ENABLE pin Voltage for Power Up</td>
<td>Relative to GND pin</td>
<td>2.0</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL-EN} )</td>
<td>ENABLE pin Voltage for Shut Down</td>
<td>Relative to GND pin</td>
<td>0.5</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( I_{IH-EN} )</td>
<td>ENABLE pin Input Current-High (Note 3)</td>
<td>( V_S = V_{CLAMP} = +12V, \ V_{DISABLE} = +12V )</td>
<td>340</td>
<td>410</td>
<td></td>
<td>I</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{IL-EN} )</td>
<td>ENABLE pin Input Current-Low (Note 3)</td>
<td>( V_S = V_{CLAMP} = +12V, \ V_{DISABLE} = +0.5V )</td>
<td>0</td>
<td>1</td>
<td></td>
<td>I</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( V_{OR-CL} )</td>
<td>Voltage Clamp Operating Range (Note 4)</td>
<td>Relative to GND pin</td>
<td>1.2</td>
<td></td>
<td></td>
<td>V_{OP}</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ACC-CL} )</td>
<td>CLAMP Accuracy (Note 5)</td>
<td>( V_{IN} = +4V, \ R_L = 1 \text{k}\Omega ) to GND</td>
<td>-250</td>
<td>100</td>
<td>250</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{CLAMP} = +1.5V ) and +3.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IH-CL} )</td>
<td>CLAMP pin Input Current—High</td>
<td>( V_S = V_{CLAMP} = +12V )</td>
<td>12</td>
<td>25</td>
<td></td>
<td>I</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{IL-CL} )</td>
<td>CLAMP pin Input Current—Low</td>
<td>( V_S = +12V, \ V_{CLAMP} = +1.2V )</td>
<td>-20</td>
<td>-15</td>
<td></td>
<td>I</td>
<td>( \mu \text{A} )</td>
</tr>
</tbody>
</table>
### Closed Loop AC Electrical Characteristics

(Notes 2 & 6) \( V_S = +5V, \) \( GND = 0V, \) \( T_A = 25^\circ C, \) \( V_{CM} = +1.5V, \) \( V_{OUT} = +1.5V, \) \( V_{CLAMP} = +5V, \) \( V_{ENABLE} = +5V, \) \( A_V = +1, \) \( R_F = 0\Omega, \) \( R_L = 150\Omega \) to GND pin, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BW</strong></td>
<td>-3 dB Bandwidth ( (V_{OUT} = 400 \text{ mVp-p}) )</td>
<td>( V_S = +5V, A_V = +1, R_F = 0\Omega )</td>
<td>125</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5V, A_V = -1, R_F = 500\Omega )</td>
<td>60</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5V, A_V = +2, R_F = 500\Omega )</td>
<td>60</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5V, A_V = +10, R_F = 500\Omega )</td>
<td>6</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +12V, A_V = +1, R_F = 0\Omega )</td>
<td>150</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +3V, A_V = +1, R_F = 0\Omega )</td>
<td>100</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>BW</strong></td>
<td>( \pm 0.1 \text{ dB Bandwidth} ) ( (V_{OUT} = 400 \text{ mVp-p}) )</td>
<td>( V_S = +12V, A_V = +1, R_F = 0\Omega )</td>
<td>25</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5V, A_V = +1, R_F = 0\Omega )</td>
<td>30</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +3V, A_V = +1, R_F = 0\Omega )</td>
<td>20</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
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<tr>
<td><strong>GBWP</strong></td>
<td>Gain Bandwidth Product</td>
<td>( V_S = +12V, A_V = +10 )</td>
<td>60</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PM</strong></td>
<td>Phase Margin</td>
<td>( R_L = 1 \text{ k}\Omega, CL = 6 \text{ pF} )</td>
<td>55</td>
<td>V</td>
<td>°</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SR</strong></td>
<td>Slew Rate</td>
<td>( V_S = +10V, R_L = 150\Omega, V_{OUT} = 0V ) to (+6V )</td>
<td>200</td>
<td>I</td>
<td>V/μs</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( V_S = +5V, R_L = 150\Omega, V_{OUT} = 0V ) to (+3V )</td>
<td>300</td>
<td>I</td>
<td>V/μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{RF} )</td>
<td>Rise Time, Fall Time</td>
<td>( \pm 0.1V ) step</td>
<td>2.8</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OS</strong></td>
<td>Overshoot</td>
<td>( \pm 0.1V ) step</td>
<td>10</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td>( t_{PD} )</td>
<td>Propagation Delay</td>
<td>( \pm 0.1V ) step</td>
<td>3.2</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_s )</td>
<td>0.1% Settling Time</td>
<td>( V_S = \pm 5V, R_L = 500\Omega, A_V = +1, V_{OUT} = \pm 3V )</td>
<td>40</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.01% Settling Time</td>
<td>( V_S = \pm 5V, R_L = 500\Omega, A_V = +1, V_{OUT} = \pm 3V )</td>
<td>75</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>( dG )</td>
<td>Differential Gain (Note 7)</td>
<td>( A_V = +2, R_F = 1 \text{ k}\Omega )</td>
<td>0.05</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td>( dP )</td>
<td>Differential Phase (Note 7)</td>
<td>( A_V = +2, R_F = 1 \text{ k}\Omega )</td>
<td>0.05</td>
<td>V</td>
<td>°</td>
<td></td>
<td></td>
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<tr>
<td>( e_N )</td>
<td>Input Noise Voltage</td>
<td>( f = 10 \text{ kHz} )</td>
<td>48</td>
<td>V</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
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<tr>
<td>( i_N )</td>
<td>Input Noise Current</td>
<td>( f = 10 \text{ kHz} )</td>
<td>1.25</td>
<td>V</td>
<td>pA/√Hz</td>
<td></td>
<td></td>
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<tr>
<td>( t_{DIS} )</td>
<td>Disable Time (Note 8)</td>
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<td>50</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>( t_{EN} )</td>
<td>Enable Time (Note 8)</td>
<td></td>
<td>25</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{CL} )</td>
<td>Clamp Overload Recovery</td>
<td></td>
<td>7</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Internal short circuit protection circuitry has been built into the EL2150C/EL2157C. See the Applications section.

**Note 2:** CLAMP pin and ENABLE pin specifications apply only to the EL2157C.

**Note 3:** If the disable feature is not desired, tie the ENABLE pin to the \( V_S \) pin, or apply a logic high level to the ENABLE pin.

**Note 4:** The maximum output voltage that can be clamped is limited to the maximum positive output Voltage, or \( V_{OP} \). Applying a Voltage higher than \( V_{OP} \) inactivates the clamp. If the clamp feature is not desired, either tie the CLAMP pin to the \( V_S \) pin, or simply let the CLAMP pin float.

**Note 5:** The clamp accuracy is affected by \( V_{IN} \) and \( R_L \). See the Typical Curves Section and the Clamp Accuracy vs. \( V_{IN} \) & \( R_L \) curve.

**Note 6:** All AC tests are performed on a "warmed up" part, except slew rate, which is pulse tested.

**Note 7:** Standard NTSC signal = 286 mVp-p, \( f = 3.58 \text{MHz} \), as \( V_{IN} \) is swept from 0.6V to 1.314V. \( R_L \) is DC coupled.

**Note 8:** Disable/Enable time is defined as the time from when the logic signal is applied to the ENABLE pin to when the supply current has reached half its final value.
Typical Performance Curves

Non-Inverting Frequency Response (Gain)
- $A_V = +1$, $R_C = 0 \Omega$
- $A_V = +2$, $R_C = 1 \kOmega$
- $A_V = +5$, $R_C = 1 \kOmega$

Frequency Response (Phase)
- $A_V = +1$, $R_C = 0 \Omega$
- $A_V = +2$, $R_C = 1 \kOmega$
- $A_V = +5$, $R_C = 1 \kOmega$

Inverting Frequency Response (Gain)
- $V_S = 5 \text{V}$
- $V_{CM} = 1.5 \text{V}$
- $R_C = 1 \kOmega$
- $R_L = 150 \Omega$

Frequency Response (Phase)
- $A_V = -2$
- $A_V = -5$

3 dB Bandwidth vs Temperature for Non-Inverting Gains
- $A_V = +1$, $R_C = 0 \Omega$
- $A_V = +2$, $R_C = 1 \kOmega$
- $A_V = +5$, $R_C = 1 \kOmega$

3 dB Bandwidth vs Temperature for Inverting Gains
- $A_V = -1$
- $A_V = -2$
- $A_V = -5$

Frequency Response for Various $R_L$
- $R_L = 1 \kOmega$
- $R_L = 50 \Omega$

Frequency Response for Various $C_L$
- $C_L = 100 \text{pF}$
- $C_L = 47 \text{pF}$
- $C_L = 22 \text{pF}$
- $C_L = 0 \text{pF}$

Non-Inverting Frequency Response vs Common Mode Voltage
- $V_C = +5 \text{V}$
- $V_{CM} = 0.5 \text{V}$
- $C_L = 100 \text{pF}$
- $V_{IN} = 400 \text{mVpp}$
- $A_V = +1$

DIE TEMPERATURE ($^\circ\text{C}$)
- Non-Inverting
- Inverting

Magnitude (Normalized) (dB)
- $+2$
- $-8$

Frequency (Hz)
- $1 \text{M}$
- $10 \text{M}$
- $100 \text{M}$

Phase (°)
- $0$
- $-360$

Temperature for Non-Inverting Gains
- $-15$
- $25$
- $65$
- $105$
- $145$

3 dB Bandwidth (MHz)
- $60$
- $40$
- $20$
- $0$

Frequency (Hz)
- $1 \text{M}$
- $10 \text{M}$
- $100 \text{M}$

2-257
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for Non-Inverting Gains

- \( A_V = +1, R_F = 0 \)
- \( A_V = +2, R_F = 1 \, \text{k}\Omega \)
- \( A_V = +5, R_F = 1 \, \text{k}\Omega \)

Frequency Response for Various Supply Voltages, \( A_V = +1 \)

- \( V_S = +10 \, \text{V} \)
- \( V_S = +5 \, \text{V} \)
- \( V_S = +3 \, \text{V} \)

PSSR and CMRR vs Frequency

PSRR and CMRR vs Die Temperature

Open Loop Gain and Phase vs Frequency

- \( V_S = +5 \, \text{V} \)

Open Loop Voltage Gain vs Die Temperature

- \( V_S = +12 \, \text{V} \)
- \( R_F = 1 \, \text{k}\Omega \) to GND
- \( V_{OUT} = +2 \, \text{V} \) to +9V

Closed Loop Output Impedance vs Frequency
Typical Performance Curves — Contd.

**Large Signal Step Response, \( V_S = +3V \)**

- \( V_{IN} = 0.2V \) to 1.45V
- \( V_S = +3V \)
- \( R_2 = 150\Omega \)
- \( A_V = +1 \)

**Large Signal Step Response, \( V_S = +5V \)**

- \( V_{IN} = 0.2V \) to 3.0V
- \( V_S = +5V \)
- \( R_2 = 150\Omega \)
- \( A_V = +1 \)

**Large Signal Step Response, \( V_S = +12V \)**

- \( V_{IN} = 0.3V \) to 8V
- \( V_S = +12V \)
- \( R_2 = 150\Omega \)
- \( A_V = +1 \)

**Small Signal Step Response**

- \( V_{IN} = 0.2V \) to 0.6V
- \( V_S = +5V \)
- \( R_2 = 150\Omega \)
- \( A_V = +1 \)

**Large Signal Step Response, \( V_S = \pm 5V \)**

- \( V_{IN} = \pm 5V \)
- \( R_2 = 150\Omega \)
- \( A_V = +1 \)

**Slew Rate vs Temperature**

- \( V_S = +5V \)
- \( R_2 = 150\Omega \) to GND
- \( A_V = +1 \)
- \( R_1 = 0 \)

**Settling Time vs Settling Accuracy**

- \( V_S = \pm 5V \)
- \( \Delta V = \pm 2.5V \)
- \( R_L = 500\Omega \)
- \( A_V = +1, R_2 = 0 \)

**Voltage and Current Noise vs Frequency**

- \( e_n = 48nV/\sqrt{Hz} \)
- \( b = 1.23pA/\sqrt{Hz} \)
Typical Performance Curves — Contd.

Differential Gain for Single Supply Operation

\[ V_S = +5V, +12V \]
\[ V_S = +3V \]
\[ V_S = +5V \]
\[ R_L = 150\Omega \]
\[ R_F = 1k\Omega \]

Differential Phase for Single Supply Operation

\[ V_S = +5V \]
\[ V_S = +12V \]
\[ R_L = 150\Omega \]
\[ A_V = +2 \]
\[ R_F = 1k\Omega \]

Differential Gain and Phase for Dual Supply Operation

\[ V_S = \pm 5V \]
\[ R_L = 150\Omega \]
\[ A_V = +2 \]
\[ R_F = 1k\Omega \]

2nd and 3rd Harmonic Distortion vs Frequency

\[ V_{\text{OUT}} = 0V \text{ to } +2V \]
\[ R_L = 100\Omega \]

2nd and 3rd Harmonic Distortion vs Frequency

\[ V_{\text{OUT}} = 0.1V \text{ to } 2.1V \]
\[ R_L = 100\Omega \]

2nd and 3rd Harmonic Distortion vs Frequency

\[ V_{\text{OUT}} = -1V \text{ to } +1V \]

Output Voltage Swing vs Frequency for THD < 0.1%

\[ V_S = +12V \]
\[ A_V = +1 \]
\[ R_L = 150\Omega \]

Output Voltage Swing vs Frequency for Unlimited Distortion

\[ V_S = +12V \]
\[ A_V = +1 \]
\[ R_L = 500\Omega \]

Output Current vs Die Temperature

\[ V_S = \pm 5V \]
\[ R_L = 10\Omega \]
Typical Performance Curves — Contd.

Supply Current vs Supply Voltage

Supply Current vs Die Temperature

Input Resistance vs Die Temperature

Offset Voltage vs Die Temperature (4 Samples)

Input Bias Current vs Input Voltage

Input Offset Current and Input Bias Current vs Die Temperature

Positive Output Voltage Swing vs Die Temperature, $R_L = 150\Omega$ to GND

Negative Output Voltage Swing vs Die Temperature, $R_L = 150\Omega$ to GND

Clamp Accuracy vs Die Temperature

$V_{CLAMP} = 3.5\text{V}$
Typical Performance Curves — Contd.

- Clamp Accuracy: $R_L = 100\Omega$

- Clamp Accuracy: $R_L = 1\, \text{k}\Omega$

- Clamp Accuracy: $R_L = 10\, \text{k}\Omega$

Enable Response for a Family of DC Inputs

$A_V = +1, R_L = 150\Omega, V_S = +5V$

Disable Response for a Family of DC Inputs

$A_V = +1, R_L = 150\Omega, V_S = +5V$

Disable/Enable Response for a Family of Sine Waves

OFF Isolation
Typical Performance Curves — Contd.

5-Lead Plastic SOT23
Maximum Power Dissipation vs Ambient Temperature

8-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

8-Lead Plastic SO
Maximum Power Dissipation vs Ambient Temperature

Burn-In Circuit

Simplified Schematic
Applications Information

Product Description
The EL2150C/EL2157C are the industry's fastest single supply operational amplifiers. Connected in voltage follower mode, their -3dB bandwidth is 125 MHz while maintaining a 275 V/μs slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2150C/EL2157C allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where pin 4 (VS-) is connected to the ground plane, a single 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor across pins 7 and 4 will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation
The EL2150C/EL2157C have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2150C/EL2157C will operate on dual supplies ranging from ±1.35V to ±6V. With a single-supply, the EL2150C/EL2157C will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 7 and 4 are the power supply pins. The positive power supply is connected to pin 7. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2150C/EL2157C have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2150C/EL2157C have an input range which spans from 0V to 3.8V.

The output range of the EL2150C/EL2157C is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ±4V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.

Choice Of Feedback Resistor, R_F
The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value which should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few picofarad range in parallel with R_F can help to reduce this ringing and peaking at the expense of reducing the bandwidth.
Applications Information — Contd.
As far as the output stage of the amplifier is concerned, $R_F + R_G$ appear in parallel with $R_L$ for gains other than $+1$. As this combination gets smaller, the bandwidth falls off. Consequently, $R_F$ has a minimum value that should not be exceeded for optimum performance.

For $A_v = +1$, $R_F = 0\Omega$ is optimum. For $A_v = -1$ or $+2$ (noise gain of 2), optimum response is obtained with $R_F$ between $500\Omega$ and $1\, k\Omega$. For $A_v = -4$ or $+5$ (noise gain of 5), keep $R_F$ between $2\, k\Omega$ and $10\, k\Omega$.

Video Performance
For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of $150\Omega$, because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2150C/EL2157C are specified with the black level of the output video signal set to $+1.2V$.

This allows ample room for the sync pulse even in a gain of $+2$ configuration. This results in $dG$ and $dP$ specifications of $0.05%$ and $0.05^\circ$ while driving $150\Omega$ at a gain of $+2$. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply $dG$ and $dP$ curves for $R_L=150\, \Omega$, if the output black level clamp is reduced from $1.2V$ to $0.6V$, $dG/dP$ will increase from $0.05%/0.05^\circ$ to $0.08%/0.25^\circ$. Note that in a gain of $+2$ configuration, this is the lowest black level allowed such that the sync tip doesn’t go below $0V$.

If your application requires that the output goes to ground, then the output stage of the EL2150C/EL2157C, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and $dG$ and $dP$ will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as $1\, k\Omega$, if the input black level is kept above $1.25V$, $dG$ and $dP$ are a respectable $0.03%$ and $0.03^\circ$.

For other biasing conditions see the Differential Gain and Differential Phase vs. Input Voltage curves.

Output Drive Capability
In spite of their moderately low $5\, mA$ of supply current, the EL2150C/EL2157C are capable of providing $\pm 100\, mA$ of output current into a $10\Omega$ load, or $\pm 60\, mA$ into $50\Omega$. With this large output current capability, a $50\Omega$ load can be driven to $\pm 3V$ with $V_S = \pm 5V$, making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2150C/EL2157C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between $5\Omega$ and $50\Omega$) can be placed in series with the output to eliminate most peaking. The gain resistor ($R_G$) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.

Disable/Power-Down
The EL2157C amplifier can be disabled, placing its output in a high-impedance state. The disable or enable action takes only about $40\, nsec$. When disabled, the amplifier’s supply current is reduced to $0\, mA$, thereby eliminating all power consumption by the EL2157C. The EL2157C amplifier’s power down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied CMOS signal is relative to the GND pin. For example, if a single $+5V$ supply is used, the logic voltage levels will be $+0.5V$ and $+2.0V$. If using dual $\pm 5V$ supplies, the logic levels will be $-4.5V$ and $-3.0V$. Letting the ENABLE pin float will disable the EL2157C. If the power-down feature is not desired, connect the ENABLE pin to the $V_{S+}$ pin. The guaranteed logic levels of $+0.5V$ and $+2.0V$ are not standard TTL levels of $+0.8V$ and $+2.0V$, so care must be taken if standard TTL will be used to drive the ENABLE pin.
Applications Information — Contd.

Output Voltage Clamp
The EL2157C amplifier has an output voltage clamp. This clamping action is fast, being activated almost instantaneously, and being deactivated in < 7 ns, and prevents the output voltage from going above the preset clamp voltage. This can be very helpful when the EL2157C is used to drive an A/D converter, as some converters can require long times to recover if overdriven. The output voltage remains at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. If the EL2157C is connected in a gain of 2, for example, and +3V DC is applied to the CLAMP pin, any voltage higher than +1.5V at the inputs will be clamped and +3V will be seen at the output.

Figure 1 below is a unity gain connected EL2157C being driven by a 3Vp-p sinewave, with 2.25V applied to the CLAMP pin. The resulting output waveform, with its output being clamped to 2.25V, is shown in Figure 2.

![Figure 1](image1)

Figure 2 shows the output of the same circuit being driven by a 0.5V to 2.75V square wave, as the clamp voltage is varied from 1.0V to 2.5V, as well as the unclamped output signal. The rising edge of the signal is clamped to the voltage applied to the CLAMP pin almost instantaneously. The output recovers from the clamped mode within 5 - 7 ns, depending on the clamp voltage. Even when the CLAMP pin is taken 0.2V below the minimum 1.2V specified, the output is still clamped and recovers in about 11 ns.

![Figure 3](image2)

The clamp accuracy is affected by 1) the CLAMP pin voltage, 2) the input voltage, and 3) the load resistor. Depending upon the application, the accuracy may be as little as a few tens of millivolts to a few hundred millivolts. Be sure to allow for these inaccuracies when choosing the clamp voltage. Curves of Clamp Accuracy vs. $V_{\text{CLAMP}}$ and $V_{\text{IN}}$ for 3 values of $R_L$ are included in the Typical Performance Curves Section.

Unlike amplifiers that clamp at the input and are therefore limited to non-inverting applications only, the EL2157C output clamp architecture works for both inverting and non-inverting gain applications. There is also no maximum voltage difference limitation between $V_{\text{IN}}$ and $V_{\text{CLAMP}}$ which is common on input clamped architectures.

The voltage clamp operates for any voltage between +1.2V above the GND pin, and the minimum output voltage swing, $V_{\text{OP}}$. Forcing the CLAMP pin much below +1.2V can saturate transistors and should therefore be avoided.
Applications Information — Contd.
Forcing the CLAMP pin above V_{OP} simply deactivates the CLAMP feature. In other words, one cannot expect to clamp any voltage higher than what the EL2157C can drive to in the first place. If the clamp feature is not desired, either let the CLAMP pin float or connect it to the V_{S+} pin.

EL2157C Comparator Application
The EL2157C can be used as a very fast, single supply comparator by utilizing the clamp feature. Most op amps used as comparators allow only slow speed operation because of output saturation issues. However, by applying a DC voltage to the CLAMP pin of the EL2157C, the maximum output voltage can be clamped, thus preventing saturation. Figure 4 below is the EL2157C implemented as a comparator. 2.5V DC is applied to the CLAMP pin, as well as the IN+ pin. A differential signal is then applied between the inputs. Figure 5 shows the output square wave that results when a ±1V, 10 MHz triangular wave is applied, while Figure 6 is a graph of propagation delay vs. overdrive as a square wave is presented at the input.

Video Sync Pulse Remover Application
All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 7 shows a unity gain connected EL2150C/EL2157C. Figure 8 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.
Applications Information — Contd.

Multiplexing with the EL2157C
The ENABLE pin on the EL2157C allows for multiplexing applications. Figure 9 shows two EL2157Cs with their outputs tied together, driving a back terminated 75Ω video load. A 2 Vp-p 10 MHz sinewave is applied at one input, and a 1 Vp-p 5 MHz sinewave to the other. Figure 10 shows the CLOCK signal which is applied, and the resulting output waveform at V_OUT. Switching is complete in about 50 ns. Notice the outputs are tied directly together. Decoupling resistors at each output are not necessary. In fact, adding them approximately doubles the switching time to 100 nsec.

Short Circuit Current Limit
The EL2150C/EL2157C have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100 mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±90 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Power Dissipation
With the high output drive capability of the EL2150C/EL2157C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2150C/EL2157C to remain in the safe operating area.
Applications Information — Contd.
The maximum power dissipation allowed in a package is determined according to [1]:

$$P_{D_{MAX}} = \frac{T_{J_{MAX}} - T_{A_{MAX}}}{\theta_{JA}}$$  \[1\]

where:

- $T_{J_{MAX}}$ = Maximum Junction Temperature
- $T_{A_{MAX}}$ = Maximum Ambient Temperature
- $\theta_{JA}$ = Thermal Resistance of the Package
- $P_{D_{MAX}}$ = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$P_{D_{MAX}} = V_S \cdot I_{S_{MAX}} + (V_S - V_{OUT}) \cdot \frac{V_{OUT}}{R_L}$$  \[2\]

where:

- $V_S$ = Total Supply Voltage
- $I_{S_{MAX}}$ = Maximum Supply Current
- $V_{OUT}$ = Maximum Output Voltage of the Application
- $R_L$ = Load Resistance tied to Ground

If we set the two $P_{D_{MAX}}$ equations, [1] & [2], equal to each other, and solve for $V_S$, we can get a family of curves for various loads and output voltages according to [3]:

$$V_S = \frac{R_L \cdot (T_{J_{MAX}} - T_{A_{MAX}}) + (V_{OUT})^2}{\theta_{JA} \cdot (I_S \cdot R_L) + V_{OUT}}$$  \[3\]

Figures 11 through 13 show total single supply voltage $V_S$ vs. $R_L$ for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of $T_A = +85^\circ C$ and $I_S = 6.5$ mA.
Applications Information — Contd.

EL2157C Macromodel

* Revision A, July 1995

* When not being used, the clamp pin, pin 1,
  should be connected to +Vs supply, pin 7

* Connections: + input
  - input
  + Vs supply
  - Vs supply
  output
  clamp

.subckt EL2157/el 3 2 7 4 6 1

* Output Stage & Clamp

i3 20 4 1.0mA
q3 7 23 20 qn
q4 7 18 19 qn
q5 7 18 21 qn
q6 4 20 22 qp
q7 7 23 18 qn
d1 19 20 da
d2 18 1 da
r8 21 6 2
r9 22 6 2
r10 18 21 10k
d11 7 23 100k
d3 23 24 da
d4 24 4 da
d5 23 18 da

* Power Supply Current

ips 7 4 3.2mA

* Models

.model qn npn(is = 800e-18 bf = 150 tf = 0.02nS)
.model qpa pnp(is = 810e-18 bf = 50 tf = 0.02nS)
.model qp pnp(is = 800e-18 bf = 54 tf = 0.02nS)
.model da d(tt = 0nS)
.ends

* Input Stage

i1 7 10 250uA
i2 7 11 250uA
r1 10 11 4k
q1 12 2 10 qp
q2 13 3 11 qpa
r2 12 4 100
r3 13 4 100

* Second Stage & Compensation

gm 15 4 13 12 4.6m
r4 15 4 15Meg
c1 15 4 0.36pF

* Poles

e1 17 4 15 4 1.0
r6 17 25 400
c3 25 4 1pF
r7 25 18 500
c4 18 4 1pF

*
EL2157C Macromodel — Contd.
Features
- Specified for +3V, +5V, or ±5V Applications
- Large Input Common Mode Range
  \[0V < V_{CM} < V_S - 1.2V\]
- Output Swings to Ground Without Saturating
- \(-3\) dB Bandwidth = 125 MHz
- \(±0.1\) dB Bandwidth = 30 MHz
- Low Supply Current = 5 mA (per amplifier)
- Slew Rate = 275 V/μsec
- Low Offset Voltage = 2 mV max
- Output Current = \(±100\) mA
- High Open Loop Gain = 80 dB
- Differential Gain = 0.05%
- Differential Phase = 0.05°

Applications
- Video Amplifier
- PCMCIA Applications
- A/D Driver
- Line Driver
- Portable Computers
- High Speed Communications
- RGB Printer, FAX, Scanner
- Broadcast Equipment
- Active Filtering

General Description
The EL2250C/EL2450C are part of a family of the electronics industries fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates 1/4 that of the EL2250C/EL2450C. The 125 MHz bandwidth, 275 V/μsec slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, this amplifier can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V below the top rail. Connecting the load resistor to ground and operating from a single supply, the outputs swing completely to ground without saturating. The outputs can also drive to within 1.2V of the top rail. The EL2250C/EL2450C will output \(±100\) mA and will operate with single supply voltages as low as 2.7V, making them ideal for portable, low power applications.

The EL2250C/EL2450C are available in plastic DIP and SOIC packages in industry standard pin outs. Both parts operate over the industrial temperature range of \(-40°C\) to \(+85°C\), and are part of a family of single supply op amps. For single amplifier applications, see the EL2150C/EL2157C. For dual and triple amplifiers with power down and output voltage clamps, see the EL2257C/EL2357C.

Connection Diagrams

**EL2250C SO, P-DIP**

**EL2450C SO, P-DIP**
**Absolute Maximum Ratings** \((T_A = 25^\circ C)\)

<table>
<thead>
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<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
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<th>Typ</th>
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<td>Power Dissipation See Curves</td>
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<td>Differential Input Voltage</td>
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<td>Operating Junction Temperature (150^\circ C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Test Level  
I  
100% production tested and QA sample tested per QA test plan QCX0002.

II  
100% production tested at \(T_A = 25^\circ C\) and QA sample tested at \(T_A = 25^\circ C\), \(T_{MAX}\) and \(T_{MIN}\) per QA test plan QCX0002.

III  
QA sample tested per QA test plan QCX0002.

IV  
Parameter is guaranteed (but not tested) by Design and Characterization Data.

V  
Parameter is typical value at \(T_A = 25^\circ C\) for information purposes only.

**DC Electrical Characteristics**

\(V_S = +5V, GND = 0V, T_A = 25^\circ C, V_{CM} = 1.5V, V_{OUT} = 1.5V\), unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Offset Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(TCV_{OS})</td>
<td>Temperature Coefficient</td>
<td>Measured from (T_{min}) to (T_{max})</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu V/\circ C)</td>
</tr>
<tr>
<td>(I_B)</td>
<td>Input Bias Current (V_{IN} = 0V)</td>
<td></td>
<td>-5.5</td>
<td>-10</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input Offset Current (V_{IN} = 0V)</td>
<td></td>
<td>-750</td>
<td>150</td>
<td>750</td>
<td>I</td>
<td>nA</td>
</tr>
<tr>
<td>(TCI_{OS})</td>
<td>Temperature Coefficient</td>
<td>Measured from (T_{min}) to (T_{max})</td>
<td></td>
<td>50</td>
<td></td>
<td>V</td>
<td>nA/(\circ C)</td>
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<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td>(V_S = +2.7V) to +12V</td>
<td>55</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(CMRR)</td>
<td>Common Mode Rejection Ratio</td>
<td>(V_{CM} = 0V) to +3.8V</td>
<td>55</td>
<td>65</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(CMIR)</td>
<td>Common Mode Input Range</td>
<td>(V_{CM} = 0V) to +3.0V</td>
<td>55</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(R_{IN})</td>
<td>Input Resistance (Common) Mode</td>
<td></td>
<td>1</td>
<td>2</td>
<td></td>
<td>I</td>
<td>(M\Omega)</td>
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<tr>
<td>(C_{IN})</td>
<td>Input Capacitance (SOIC) Package</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>(PDIP) Package</td>
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<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td>(R_{OUT})</td>
<td>Output Resistance (A_v = +1)</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>V</td>
<td>(m\Omega)</td>
</tr>
<tr>
<td>(I_S)</td>
<td>Supply Current (per amplifier) (V_S = +12V)</td>
<td></td>
<td>5</td>
<td>6.5</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(PSOR)</td>
<td>Power Supply Operating Range</td>
<td></td>
<td>2.7</td>
<td>12.0</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Parameter</td>
<td>Description</td>
<td>Test Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Test Level</td>
<td>Units</td>
</tr>
<tr>
<td>-----------</td>
<td>------------------------------------</td>
<td>------------------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------------</td>
<td>-------</td>
</tr>
<tr>
<td>AVOL</td>
<td>Open Loop Gain</td>
<td>$V_S = +12V, V_{OUT} = +2V$ to $+9V$, $R_L = 1k\Omega$ to GND</td>
<td>65</td>
<td>80</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 1k\Omega$ to GND</td>
<td>70</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 150\Omega$ to GND</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>V_{OP}</td>
<td>Positive Output Voltage Swing</td>
<td>$V_S = +12V$, $A_V = +1$, $R_L = 1k\Omega$ to 0V</td>
<td>10.8</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V</td>
<td>9.6</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V$, $A_V = +1$, $R_L = 1k\Omega$ to 0V</td>
<td>4.0</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V</td>
<td>3.4</td>
<td>3.8</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = +3V$, $A_V = +1$, $R_L = 150\Omega$ to 0V</td>
<td>1.8</td>
<td>1.95</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>V_{ON}</td>
<td>Negative Output Voltage Swing</td>
<td>$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V</td>
<td>5.5</td>
<td>8</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V$, $A_V = +1$, $R_L = 1k\Omega$ to 0V</td>
<td>-4.0</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V</td>
<td>-3.7</td>
<td>-3.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>I_{OUT}</td>
<td>Output Current (Note 1)</td>
<td>$V_S = \pm 5V$, $A_V = +1$, $R_L = 10\Omega$ to 0V</td>
<td>±75</td>
<td>±100</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V$, $A_V = +1$, $R_L = 50\Omega$ to 0V</td>
<td>±60</td>
<td></td>
<td></td>
<td>V</td>
<td>mA</td>
</tr>
</tbody>
</table>
# Closed Loop AC Electrical Characteristics

(Nota 2) $V_s = \pm 5V$, $GND = 0V$, $T_A = 25°C$, $V_{CM} = \pm 1.5V$, $V_{OUT} = \pm 1.5V$, $A_V = \pm 1$, $R_F = 0\Omega$, $R_L = 150\Omega$ to GND pin, unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BW$</td>
<td>$-3\text{dB Bandwidth}$ ($V_{OUT} = 400\text{mVp-p}$)</td>
<td>$V_s = +5V$, $A_V = \pm 1$, $R_F = 0\Omega$</td>
<td>125</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +5V$, $A_V = -1$, $R_F = 500\Omega$</td>
<td>60</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +5V$, $A_V = +2$, $R_F = 500\Omega$</td>
<td>60</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +5V$, $A_V = +10$, $R_F = 500\Omega$</td>
<td>6</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +12V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>150</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +3V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>100</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$BW$</td>
<td>$\pm 0.1\text{dB Bandwidth}$ ($V_{OUT} = 400\text{mVp-p}$)</td>
<td>$V_s = +12V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>25</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +5V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>30</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +3V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>20</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$GBWP$</td>
<td>Gain Bandwidth Product</td>
<td>$V_s = +12V$, $A_V = +10$</td>
<td>60</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$PM$</td>
<td>Phase Margin</td>
<td>$R_L = 1\text{k}\Omega$, $C_L = 6\text{pF}$</td>
<td>55</td>
<td>V</td>
<td></td>
<td>°</td>
<td></td>
</tr>
<tr>
<td>$SR$</td>
<td>Slew Rate</td>
<td>$V_s = +10V$, $R_L = 150\Omega$, $V_{OUT} = 0V$ to $+6V$</td>
<td>200</td>
<td>275</td>
<td>I</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = +5V$, $R_L = 150\Omega$, $V_{OUT} = 0V$ to $+3V$</td>
<td>300</td>
<td>V</td>
<td></td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>$t_{R}$, $t_{F}$</td>
<td>Rise Time, Fall Time</td>
<td>$\pm 0.1V$ Step</td>
<td>2.8</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$OS$</td>
<td>Overshoot</td>
<td>$\pm 0.1V$ Step</td>
<td>10</td>
<td>V</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay</td>
<td>$\pm 0.1V$ Step</td>
<td>3.2</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_s$</td>
<td>0.1% Settling Time</td>
<td>$V_s = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$</td>
<td>40</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.01% Settling Time</td>
<td>$V_s = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$</td>
<td>75</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$dG$</td>
<td>Differential Gain (Nota 3)</td>
<td>$A_V = \pm 2$, $R_F = 1\text{k}\Omega$</td>
<td>0.05</td>
<td>V</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$dP$</td>
<td>Differential Phase (Nota 3)</td>
<td>$A_V = \pm 2$, $R_F = 1\text{k}\Omega$</td>
<td>0.05</td>
<td>V</td>
<td></td>
<td>°</td>
<td></td>
</tr>
<tr>
<td>$e_N$</td>
<td>Input Noise Voltage</td>
<td>$f = 10$ kHz</td>
<td>48</td>
<td>V</td>
<td></td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>$i_N$</td>
<td>Input Noise Current</td>
<td>$f = 10$ kHz</td>
<td>1.25</td>
<td>V</td>
<td></td>
<td>pA/√Hz</td>
<td></td>
</tr>
</tbody>
</table>

Nota 1: Internal short circuit protection circuitry has been built into the EL2250C/EL2450C. See the Applications section.

Nota 2: All AC tests are performed on a "warmed up" part, except slew rate, which is pulse tested.

Nota 3: Standard NTSC signal = 286 mVp-p, $f = 3.58$ MHz, as $V_{IN}$ is swept from 0.6V to 1.314V. $R_L$ is DC coupled.
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

3 dB Bandwidth vs Temperature for Non-Inverting Gains

3 dB Bandwidth vs Temperature for Inverting Gains

Frequency Response for Various $R_L$

Frequency Response for Various $C_L$

Non-Inverting Frequency Response vs Common Mode Voltage

Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

3 dB Bandwidth vs Temperature for Non-Inverting Gains

3 dB Bandwidth vs Temperature for Inverting Gains

Frequency Response for Various $R_L$

Frequency Response for Various $C_L$

Non-Inverting Frequency Response vs Common Mode Voltage
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for Non-Inverting Gains

3 dB Bandwidth vs Supply Voltage for Inverting Gains

Frequency Response for Various Supply Voltages, $A_v = 1$

Frequency Response for Various Supply Voltages, $A_v = 2$

PSRR and CMRR vs Frequency

PSRR and CMRR vs Die Temperature

Open Loop Gain and Phase vs Frequency

Open Loop Voltage Gain vs Die Temperature

Closed Loop Output Impedance vs Frequency
Typical Performance Curves — Contd.

**Large Signal Step Response, \( V_S = +3V \)**

- \( V_{IN} = 0.2V \) to 1.45V
- \( V_S = +3V \)
- \( R_L = 150\Omega \)
- \( A_V = +1 \)

**Large Signal Step Response, \( V_S = +5V \)**

- \( V_{IN} = 0.2V \) to 3.0V
- \( V_S = +5V \)
- \( R_L = 150\Omega \)
- \( A_V = +1 \)

**Large Signal Step Response, \( V_S = +12V \)**

- \( V_{IN} = 0.3V \) to 8V
- \( V_S = +12V \)
- \( R_L = 150\Omega \)
- \( A_V = +1 \)

**Small Signal Step Response**

- \( V_{IN} = 0.2V \) to 0.6V
- \( V_S = +5V \)
- \( R_L = 150\Omega \)
- \( A_V = +1 \)

**Slew Rate vs Temperature**

<table>
<thead>
<tr>
<th>Die Temperature (°C)</th>
<th>Slew Rate (V/µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-55</td>
<td>500</td>
</tr>
<tr>
<td>-15</td>
<td>450</td>
</tr>
<tr>
<td>25</td>
<td>400</td>
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<tr>
<td>65</td>
<td>350</td>
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<tr>
<td>105</td>
<td>300</td>
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<tr>
<td>145</td>
<td>250</td>
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<tr>
<td>0</td>
<td>200</td>
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<td>-55</td>
<td>150</td>
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<td>-15</td>
<td>100</td>
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<td>25</td>
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<td>65</td>
<td>0</td>
</tr>
<tr>
<td>105</td>
<td>0</td>
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<tr>
<td>145</td>
<td>0</td>
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**Settling Time vs Settling Accuracy**

<table>
<thead>
<tr>
<th>Settling Time (ns)</th>
<th>Settling Accuracy (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>0.1%</td>
</tr>
<tr>
<td>200</td>
<td>0.5%</td>
</tr>
<tr>
<td>300</td>
<td>1.0%</td>
</tr>
<tr>
<td>400</td>
<td>1.5%</td>
</tr>
<tr>
<td>500</td>
<td>2.0%</td>
</tr>
</tbody>
</table>

**Voltage and Current Noise vs Frequency**

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Voltage Noise (nV/√Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>1k</td>
<td>100</td>
</tr>
<tr>
<td>10k</td>
<td>100</td>
</tr>
<tr>
<td>100k</td>
<td>100</td>
</tr>
<tr>
<td>1M</td>
<td>100</td>
</tr>
</tbody>
</table>

\( V_S = \pm 5V \)

\( \Delta V = \pm 2.5V \)

\( R_L = 500\Omega \)

\( A_V = +1, R_C = 0 \)

\( AV = -1, R_C = 1 \, k\Omega \)

\( \sigma_n = 48nV/\sqrt{Hz} \)

\( \sigma_i = 1.25pA/\sqrt{Hz} \)
Typical Performance Curves — Contd.

Differential Gain for Single Supply Operation

Differential Phase for Single Supply Operation

Differential Gain and Phase for Dual Supply Operation

2nd and 3rd Harmonic Distortion vs Frequency

2nd and 3rd Harmonic Distortion vs Frequency

2nd and 3rd Harmonic Distortion vs Frequency

Output Voltage Swing vs Frequency for THD < 0.1%

Output Voltage Swing vs Frequency for Unlimited Distortion

Output Current vs Die Temperature
Typical Performance Curves — Contd.

**Supply Current vs Supply Voltage (per amplifier)**

- **Supply Current vs Die Temperature (per amplifier)**: \( V_C = +12\,\text{V} \)

**Input Resistance vs Die Temperature**

- **Offset Voltage vs Die Temperature (4 Samples)**

**Input Bias Current vs Input Voltage**: \( V_S = +12\,\text{V} \)

**Input Offset Current and Input Bias Current vs Die Temperature**

- **Positive Output Voltage Swing vs Die Temperature**, \( R_L = 150\,\Omega \) to GND

- **Negative Output Voltage Swing vs Die Temperature**, \( R_L = 150\,\Omega \) to GND

- **Channel to Channel Isolation vs Frequency**
Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

\[ T_{J \text{ MAX}} = 150^\circ C \]
\[ \theta_{JA} = 95^\circ C/W \]
\[ \theta_{JC} = 50^\circ C/W \]

14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

\[ T_{J \text{ MAX}} = 150^\circ C \]
\[ \theta_{JA} = 77^\circ C/W \]
\[ \theta_{JC} = 40^\circ C/W \]

8-Lead Plastic SOIC
Maximum Power Dissipation
vs Ambient Temperature

\[ T_{J \text{ MAX}} = 150^\circ C \]
\[ \theta_{JA} = 165^\circ C/W \]
\[ \theta_{JC} = 45^\circ C/W \]

14-Lead Plastic SOIC
Maximum Power Dissipation
vs Ambient Temperature

\[ T_{J \text{ MAX}} = 150^\circ C \]
\[ \theta_{JA} = 116^\circ C/W \]
\[ \theta_{JC} = 40^\circ C/W \]

Simplified Schematic

[Diagram of simplified schematic]
Applications Information

Product Description
The EL2250C/EL2450C are part of a family of the industries fastest single supply operational amplifiers. Connected in voltage follower mode, their -3dB bandwidth is 125 MHz while maintaining a 275 V/µs slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2250C/EL2450C allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where the GND pin is connected to the ground plane, a single 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor across the VS+ and GND pins will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation
The EL2250C/EL2450C have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2250C/EL2450C will operate on dual supplies ranging from ±1.35V to ±6V. With a single-supply, the EL2250C/EL2450C will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 8 and 4 are the power supply pins on the EL2250C. The positive power supply is connected to pin 8. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

Pins 4 and 11 are the power supply pins on the EL2450C. The positive power supply is connected to pin 4. When used in single supply mode, pin 11 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 11.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2250C/EL2450C have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2250C/EL2450C have an input range which spans from 0V to 3.8V.

The output range of the EL2250C/EL2450C is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail with a 1 kΩ load. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ±4V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.
Applications Information — Contd.

Choice Of Feedback Resistor, RF

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, RF has some maximum value which should not be exceeded for optimum performance. If a large value of RF must be used, a small capacitor in the few picofarad range in parallel with RF can help to reduce this ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, RF + RG appear in parallel with RL for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, RF has a minimum value that should not be exceeded for optimum performance.

For AV = +1, RF = 0 Ω is optimum. For AV = -1 or +2 (noise gain of 2), optimum response is obtained with RF between 500 Ω and 1 kΩ. For AV = -4 or +5 (noise gain of 5), keep RF between 2 kΩ and 10 kΩ.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150 Ω, because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2250C/EL2450C are specified with the black level of the output video signal set to +1.2V. This allows ample room for the sync pulse even in a gain of +2 configuration. This results in dG and dP specifications of 0.05% and 0.05° while driving 150 Ω at a gain of +2. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply dG and dP curves for RL = 150 Ω, if the output black level clamp is reduced from 1.2V to 0.6V dG/dP will increase from 0.05%/0.05° to 0.08%/0.25°. Note that in a gain of +2 configuration, this is the lowest black level allowed such that the sync tip doesn’t go below 0V.

If your application requires that the output goes to ground, then the output stage of the EL2250C/EL2450C, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and dG and dP will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as 1 kΩ, if the input black level is kept above 1.25V, dG and dP are a respectable 0.03% and 0.03°.

For other biasing conditions see the Differential Gain and Differential Phase vs. Input Voltage curves.

Output Drive Capability

In spite of their moderately low 5 mA of supply current, the EL2250C/EL2450C are capable of providing ±100 mA of output current into a 10 Ω load, or ±60 mA into 50 Ω. With this large output current capability, a 50 Ω load can be driven to ±3V with VS = ±5V, making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2250C/EL2450C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5 kΩ and 50 kΩ) can be placed in series with the output to eliminate most peaking. The gain resistor (RG) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.

Video Sync Pulse Remover Application

All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off.
Application Information — Contd.

Figure 1 shows a unity gain connected amplifier A of an EL2250C. Figure 2 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

![Figure 1](image1)

![Figure 2](image2)

Short Circuit Current Limit

The EL2250C/EL2450C have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100 mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ± 90 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Power Dissipation

With the high output drive capability of the EL2250C/EL2450C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2250C/EL2450C to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to [1]:

$$ PD_{\text{MAX}} = \frac{T_{\text{JMAX}} - T_{\text{AMAX}}}{\theta_{JA}} $$

where:

\( T_{\text{JMAX}} \) = Maximum Junction Temperature
\( T_{\text{AMAX}} \) = Maximum Ambient Temperature
\( \theta_{JA} \) = Thermal Resistance of the Package
\( PD_{\text{MAX}} \) = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$ PD_{\text{MAX}} = N(V_s' IS_{\text{MAX}} + (V_s - V_{\text{OUT}}) V_{\text{OUT}}) R_L $$

where:

\( N \) = Number of amplifiers
\( V_s \) = Total Supply Voltage
\( IS_{\text{MAX}} \) = Maximum Supply Current per amplifier
\( V_{\text{OUT}} \) = Maximum Output Voltage of the Application
\( R_L \) = Load Resistance tied to Ground

If we set the two \( PD_{\text{MAX}} \) equations, [1] & [2], equal to each other, and solve for \( V_s \), we can get a family of curves for various loads and output voltages according to [3]:

$$ R_L \left( T_{\text{JMAX}} - T_{\text{AMAX}} \right) + (V_{\text{OUT}})^2 \frac{N^2 \theta_{JA}}{(IS R_L) + V_{\text{OUT}}} $$

Figures 3 through 6 below show total single supply voltage \( V_s \) vs. \( R_L \) for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of \( T_A = 85^\circ C \) and \( IS = 6.5 \text{ mA per amplifier.} \)
Application Information — Contd.

EL2250C Single Supply Voltage vs R_LOAD for Various V_OUT (PDIP Package)

Figure 3

EL2450C Single Supply Voltage vs R_LOAD for Various V_OUT (PDIP Package)

Figure 5

EL2250C Single Supply Voltage vs R_LOAD for Various V_OUT (SO Package)

Figure 4

EL2450C Single Supply Voltage vs R_LOAD for Various V_OUT (SO Package)

Figure 6
EL2250C/EL2450C Macromodel (one amplifier)

* Revision A, April 1996
* Pin numbers reflect a standard single op amp.
* Connections:
  * + input
  * − input
  * + Vsupply
  * − Vsupply
  * output

.subckt EL2250/el 3 2 7 4 6

* Input Stage

i1 7 10 250μA
i2 7 11 250μA
r1 10 11 4k
q1 12 2 10 qp
q2 13 3 11 qpa
r2 12 4 100
r3 13 4 100

* Second Stage & Compensation

gm 15 4 13 12 4.6m
r4 15 4 15Meg
c1 15 4 0.36pF

* Poles

c1 17 4 15 4 1.0
r6 17 25 400
c3 25 4 1pF
r7 25 18 500
c4 18 4 1pF

* Output Stage

i3 20 4 1.0mA
q3 7 23 20 qn
q4 7 18 19 qn
q5 7 18 21 qn
q6 4 20 22 qp
q7 7 23 18 qn

.dlct EL2250/e1 3 2 7 4

*d Power Supply Current

ips 7 4 3.2mA

* Models

.model qn npn(is = 800e-18 bf = 150 tf = 0.02nS)
.model qpa npn(is = 810e-18 bf = 50 tf = 0.02nS)
.model qp npn(is = 800e-18 bf = 54 tf = 0.02nS)
.model da d(tt = 0nS)
.ends
EL2250C/EL2450C Macromodel (one amplifier) — Contd.
Features
- Specified for +3V, +5V, or ±5V Applications
- Power Down to 0 µA
- Output Voltage Clamp
- Large Input Common Mode Range
  0V < V_CM < V_S - 1.2V
- Output Swings to Ground Without Saturating
- -3 dB Bandwidth = 125 MHz
- ±0.1 dB Bandwidth = 30 MHz
- Low Supply Current = 5 mA
- Slew Rate = 275 V/µs
- Low Offset Voltage = 3 mV max
- Output Current = ±100 mA
- High Open Loop Gain = 80 dB
- Differential Gain = 0.05%
- Differential Phase = 0.05°

Applications
- Video Amplifier
- PCMCIA Applications
- A/D Driver
- Line Driver
- Portable Computers
- High Speed Communications
- RGB Printer, FAX, Scanner Applications
- Broadcast Equipment
- Active Filtering
- Multiplexing

General Description
The EL2257C/EL2357C are the electronics industry's fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates ¼ that of the EL2257C/EL2357C. The 125 MHz bandwidth, 275 V/µs slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, this amplifier can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V below the top rail. Connecting the load resistor to ground and operating from a single supply, the outputs swing completely to ground without saturating. The outputs can also drive to within 1.2V of the top rail. The EL2257C/EL2357C will output ±100 mA and will operate with single supply voltages as low as 2.7V, making them ideal for portable, low power applications.

The EL2257C/EL2357C have a high speed disable feature. Applying a low logic level to all ENABLE pins reduces the supply current to 0 µA within 50 ns. Each amplifier has its own ENABLE pin. This is useful for both multiplexing and reducing power consumption.

The EL2257C/EL2357C also have an output voltage clamp feature. This clamp is a fast recovery (<7 ns) output clamp that prevents the output voltage from going above the preset clamp voltage. This feature is desirable for A/D applications, as A/D converters can require long times to recover if overdriven.

The EL2257C/EL2357C are available in plastic DIP and SOIC packages. Both parts operate over the industrial temperature range of -40°C to +85°C. For single amplifier applications, see the EL2150C/EL2157C. For space saving, industry standard pin out dual and quad applications, see the EL2250C/EL2450C.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2257CN</td>
<td>-40°C to +85°C</td>
<td>14 Pin DIP</td>
<td>MDPO031</td>
</tr>
<tr>
<td>EL2257CS</td>
<td>-40°C to +85°C</td>
<td>14 Pin SOIC</td>
<td>MDPO027</td>
</tr>
<tr>
<td>EL2357CN</td>
<td>-40°C to +85°C</td>
<td>16 Pin DIP</td>
<td>MDPO031</td>
</tr>
<tr>
<td>EL2357CS</td>
<td>-40°C to +85°C</td>
<td>16 Pin SOIC</td>
<td>MDPO027</td>
</tr>
</tbody>
</table>

Connection Diagrams
Absolute Maximum Ratings \((T_A = 25^\circ C)\)

- Supply Voltage between \(V_S\) and GND: 12.6V
- Input Voltage (IN+, IN-, GND–0.3V, \(V_S+0.3V\), ENABLE, CLAMP): Storage Temperature Range: –65°C to +150°C
- Differential Input Voltage: ±6V
- Maximum Output Current: 90 mA
- Output Short Circuit Duration: (Note 1)

Power Dissipation: See Curves

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J=T_C=T_A\).

Test Level       Test Procedure
I                100% production tested and QA sample tested per QA test plan QCX0002.
II               100% production tested at \(T_A = 25^\circ C\) and QA sample tested at \(T_A = 25^\circ C\).
III              \(T_{MAX}\) and \(T_{MIN}\) per QA test plan QCX0002.
IV               QA sample tested per QA test plan QCX0002.
V                Parameter is guaranteed (but not tested) by Design and Characterization Data.

DC Electrical Characteristics

\(V_S = +5V, GND = 0V, T_A = 25^\circ C, V_{CM} = 1.5V, V_{OUT} = 1.5V, V_{CLAMP} = +5V, V_{ENABLE} = +5V\), unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS}) Offset Voltage</td>
<td>EL2257C</td>
<td>–2</td>
<td>2</td>
<td>I</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>EL2357C</td>
<td>–6</td>
<td>6</td>
<td>I</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>(TC_{VOS}) Offset Voltage</td>
<td>Temperature Coefficient</td>
<td>Measured from (T_{MIN}) to (T_{MAX})</td>
<td>10</td>
<td></td>
<td>V</td>
<td></td>
<td>(\mu V^/^\circ C)</td>
</tr>
<tr>
<td>(I_B) Input Bias Current</td>
<td>(V_{IN} = 0V)</td>
<td>–5.5</td>
<td>–10</td>
<td>I</td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OS}) Input Offset Current</td>
<td>(V_{IN} = 0V)</td>
<td>–750</td>
<td>150</td>
<td>750</td>
<td>I</td>
<td></td>
<td>nA/(^\circ C)</td>
</tr>
<tr>
<td>(TC_{I_B}) Input Bias Current</td>
<td>Temperature Coefficient</td>
<td>Measured from (T_{MIN}) to (T_{MAX})</td>
<td>50</td>
<td></td>
<td>V</td>
<td></td>
<td>nA/(^\circ C)</td>
</tr>
<tr>
<td>(PSRR) Power Supply Rejection Ratio</td>
<td>(V_S = V_{ENABLE} = +2.7V) to +12V, (V_{CLAMP} = OPEN)</td>
<td>55</td>
<td>70</td>
<td>I</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(CMRR) Common Mode Rejection Ratio</td>
<td>(V_{CM} = 0V) to +3.8V</td>
<td>55</td>
<td>65</td>
<td>I</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{CM} = 0V) to +3.0V</td>
<td>55</td>
<td>70</td>
<td>I</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>(CMIR) Common Mode Input Range</td>
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<td>(V_S - 1.2)</td>
<td>I</td>
<td>V</td>
<td></td>
<td></td>
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<td>(R_{IN}) Input Resistance</td>
<td>Common Mode</td>
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<td>2</td>
<td>I</td>
<td></td>
<td>M(\Omega)</td>
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<td>(C_{IN}) Input Capacitance</td>
<td>SOIC Package</td>
<td>1</td>
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<td>V</td>
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<td>pF</td>
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<td></td>
<td>PDIP Package</td>
<td>1.5</td>
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<td>V</td>
<td></td>
<td>pF</td>
<td></td>
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<tr>
<td>(R_{OUT}) Output Resistance</td>
<td>(A_V = +1)</td>
<td>40</td>
<td></td>
<td>V</td>
<td></td>
<td>m(\Omega)</td>
<td></td>
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<tr>
<td>(I_{S,ON}) Supply Current - Enabled (per amplifier)</td>
<td>(V_S = V_{CLAMP} = +12V, V_{ENABLE} = +12V)</td>
<td>5</td>
<td>6.5</td>
<td>I</td>
<td>m(A)</td>
<td></td>
<td></td>
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<tr>
<td>(I_{S,OFF}) Supply Current - Shut Down (per amplifier)</td>
<td>(V_S = V_{CLAMP} = +10V, V_{ENABLE} = +0.5V)</td>
<td>0</td>
<td>50</td>
<td>I</td>
<td>(\mu A)</td>
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<tr>
<td></td>
<td>(V_S = V_{CLAMP} = +12V, V_{ENABLE} = +0.5V)</td>
<td>5</td>
<td></td>
<td>V</td>
<td>(\mu A)</td>
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<tr>
<td>(PSOR) Power Supply Operating Range</td>
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<td>I</td>
<td>V</td>
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</table>
### DC Electrical Characteristics — Contd.

$V_S = +5\, V$, $GND = 0\, V$, $T_A = 25^\circ C$, $V_{CM} = +1.5\, V$, $V_{OUT} = +1.5\, V$, $V_{CLAMP} = +5\, V$, $V_{ENABLE} = +5\, V$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>$AVOL$</td>
<td>Open Loop Gain</td>
<td>$V_S = V_{CLAMP} = +12, V$, $V_{OUT} = +2, V$ to $+9, V$, $R_L = 1, k\Omega$ to $0, V$</td>
<td>65</td>
<td>80</td>
<td></td>
<td>I</td>
<td>dB</td>
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<td></td>
<td></td>
<td>$V_{OUT} = +1.5, V$ to $+3.5, V$, $R_L = 1, k\Omega$ to $GND$</td>
<td>70</td>
<td></td>
<td>V</td>
<td>dB</td>
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<td></td>
<td></td>
<td>$V_{OUT} = +1.5, V$ to $+3.5, V$, $R_L = 150, \Omega$ to $GND$</td>
<td>60</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
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<tr>
<td>$V_{OP}$</td>
<td>Positive Output Voltage Swing</td>
<td>$V_S = +12, V$, $A_V = +1$, $R_L = 1, k\Omega$ to $0, V$</td>
<td>10.8</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
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<td></td>
<td></td>
<td>$V_S = +12, V$, $A_V = +1$, $R_L = 150, \Omega$ to $0, V$</td>
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<td>10.0</td>
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<td>I</td>
<td>V</td>
</tr>
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<td></td>
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<td>$V_S = \pm 5, V$, $A_V = +1$, $R_L = 1, k\Omega$ to $0, V$</td>
<td>4.0</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
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<td></td>
<td></td>
<td>$V_S = \pm 5, V$, $A_V = +1$, $R_L = 150, \Omega$ to $0, V$</td>
<td>3.4</td>
<td>3.8</td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
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<td></td>
<td>$V_S = +3, V$, $A_V = +1$, $R_L = 150, \Omega$ to $0, V$</td>
<td>1.8</td>
<td>1.95</td>
<td></td>
<td>V</td>
<td>V</td>
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<tr>
<td>$V_{ON}$</td>
<td>Negative Output Voltage Swing</td>
<td>$V_S = +12, V$, $A_V = +1$, $R_L = 150, \Omega$ to $0, V$</td>
<td>5.5</td>
<td>8</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5, V$, $A_V = +1$, $R_L = 1, k\Omega$ to $0, V$</td>
<td>-4.0</td>
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<td>$V_S = \pm 5, V$, $A_V = +1$, $R_L = 150, \Omega$ to $0, V$</td>
<td>-3.7</td>
<td>-3.4</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current (Note 1)</td>
<td>$V_S = \pm 5, V$, $A_V = +1$, $R_L = 10, \Omega$ to $0, V$</td>
<td>$\pm 75$</td>
<td>$\pm 100$</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5, V$, $A_V = +1$, $R_L = 50, \Omega$ to $0, V$</td>
<td>$\pm 60$</td>
<td></td>
<td>V</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT,OFF}$</td>
<td>Output Current, Disabled</td>
<td>$V_{ENABLE} = +0.5, V$</td>
<td>0</td>
<td>20</td>
<td></td>
<td>I</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{IH-EN}$</td>
<td>ENABLE pin Voltage for Power Up</td>
<td>Relative to GND Pin</td>
<td>2.0</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL-EN}$</td>
<td>ENABLE pin Voltage for Shut Down</td>
<td>Relative to GND Pin</td>
<td>0.5</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH-EN}$</td>
<td>ENABLE pin Input Current-High (Note 2)</td>
<td>$V_S = V_{CLAMP} = +12, V$, $V_{ENABLE} = +12, V$</td>
<td>340</td>
<td>410</td>
<td>I</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$I_{IL-EN}$</td>
<td>ENABLE pin Input Current-Low (Note 2)</td>
<td>$V_S = V_{CLAMP} = +12, V$, $V_{ENABLE} = +0.5, V$</td>
<td>0</td>
<td>1</td>
<td>I</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$V_{OR-CL}$</td>
<td>Voltage Clamp Operating Range (Note 3)</td>
<td>Relative to GND Pin</td>
<td>1.2</td>
<td></td>
<td></td>
<td>$V_{OP}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{ACC-CL}$</td>
<td>CLAMP Accuracy (Note 4)</td>
<td>$V_{IN} = +4, V$, $R_L = 1, k\Omega$ to $GND$</td>
<td>$-250$</td>
<td>100</td>
<td>250</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{IH-CL}$</td>
<td>CLAMP pin Input Current - High</td>
<td>$V_S = V_{CLAMP} = +12, V$</td>
<td>12</td>
<td>25</td>
<td></td>
<td>$\mu$A</td>
<td></td>
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<tr>
<td>$I_{IL-CL}$</td>
<td>CLAMP pin Input Current - Low</td>
<td>$V_S = +12, V$, $V_{CLAMP} = +1.2, V$</td>
<td>$-20$</td>
<td>$-15$</td>
<td>I</td>
<td>$\mu$A</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Internal short circuit protection circuitry has been built into the EL2257C/EL2357C. See the Applications section.

Note 2: If the disable feature is not desired, tie the ENABLE pins to the $V_S$ pin, or apply a logic high level to the ENABLE pins.

Note 3: The maximum output voltage that can be clamped is limited to the maximum positive output Voltage, or $V_{OP}$. Applying a Voltage higher than $V_{OP}$ inactivates the clamp. If the clamp feature is not desired, either tie the CLAMP pin to the $V_S$ pin, or simply let the CLAMP pin float.

Note 4: The clamp accuracy is affected by $V_{IN}$ and $R_L$. See the Typical Curves Section and the Clamp Accuracy vs. $V_{IN}$ and $R_L$ curve.
Closed Loop AC Electrical Characteristics
(Note 5) $V_S = +5V$, $GND = 0V$, $T_A = 25^\circ C$, $V_{CM} = +1.5V$, $V_{OUT} = +1.5V$, $V_{CLAMP} = +5V$, $V_{ENABLE} = +5V$, $A_V = +1$, $R_F = 0\Omega$, $RL = 150\Omega$ to GND pin, unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>$-3,\text{dB Bandwidth}$</td>
<td>$V_S = +5V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>125</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>$V_S = +5V$, $A_V = -1$, $R_F = 500\Omega$</td>
<td>60</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>$V_S = +5V$, $A_V = +2$, $R_F = 500\Omega$</td>
<td>60</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_S = +12V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>150</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_S = +3V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>100</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>BW</td>
<td>$\pm 0.1,\text{dB Bandwidth}$</td>
<td>$V_S = +12V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>25</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_S = +5V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>30</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_S = +3V$, $A_V = +1$, $R_F = 0\Omega$</td>
<td>20</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain Bandwidth Product</td>
<td>$V_S = +12V$, @ $A_V = +10$</td>
<td>60</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
<td>$R_L = 1,k\Omega$, $CL = 6,pF$</td>
<td>55</td>
<td>V</td>
<td>*</td>
<td></td>
<td></td>
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<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>$V_S = +10V$, $R_L = 150\Omega$, $V_{out} = 0V$ to $+6V$</td>
<td>200</td>
<td>I</td>
<td>V/µs</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>$V_S = +5V$, $R_L = 150\Omega$, $V_{out} = 0V$ to $+3V$</td>
<td>275</td>
<td>I</td>
<td>V/µs</td>
<td></td>
<td></td>
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<td></td>
<td>$V_S = +5V$, $R_L = 150\Omega$, $V_{out} = +3V$</td>
<td>300</td>
<td>V</td>
<td>V/µs</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>t_{R,F}</td>
<td>Rise Time, Fall Time</td>
<td>$\pm 0.1V$ Step</td>
<td>2.8</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>$\pm 0.1V$ Step</td>
<td>10</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{PD}</td>
<td>Propagation Delay</td>
<td>$\pm 0.1V$ Step</td>
<td>3.2</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_S</td>
<td>$0.1%$ Settling Time</td>
<td>$V_S = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$</td>
<td>40</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$0.01%$ Settling Time</td>
<td>$V_S = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$</td>
<td>75</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>dG</td>
<td>Differential Gain (Note 6)</td>
<td>$A_V = +2$, $R_F = 1,k\Omega$</td>
<td>0.05</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase (Note 6)</td>
<td>$A_V = +2$, $R_F = 1,k\Omega$</td>
<td>0.05</td>
<td>V</td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e_N</td>
<td>Input Noise Voltage</td>
<td>$f = 10,kHz$</td>
<td>48</td>
<td>V</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>i_N</td>
<td>Input Noise Current</td>
<td>$f = 10,kHz$</td>
<td>1.25</td>
<td>V</td>
<td>pA/√Hz</td>
<td></td>
<td></td>
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<tr>
<td>t_{DIS}</td>
<td>Disable Time (Note 7)</td>
<td></td>
<td>50</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{EN}</td>
<td>Enable Time (Note 7)</td>
<td></td>
<td>25</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{CL}</td>
<td>Clamp Overload Recovery</td>
<td></td>
<td>7</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 5: All AC tests are performed on a "warmed up" part, except slew rate, which is pulse tested.

Note 6: Standard NTSC signal = 286 mVp-p, f = 3.58 MHz, as $V_{IN}$ is swept from 0.6V to 1.314V. $R_L$ is DC coupled.

Note 7: Disable/Enable time is defined as the time from when the logic signal is applied to the ENABLE pin to when the supply current has reached half its final value.
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

3 dB Bandwidth vs Temperature for Non-Inverting Gains

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

3 dB Bandwidth vs Temperature for Inverting Gains

Frequency Response for Various $R_L$

Frequency Response for Various $C_L$

Non-Inverting Frequency Response vs Common Mode Voltage
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for Non-Inverting Gains

Frequency Response for Various Supply Voltages, \( A_V = 1 \)

PSRR and CMRR vs Frequency

3 dB Bandwidth vs Supply Voltage for Inverting Gains

Frequency Response for Various Supply Voltages, \( A_V = 2 \)

PSRR and CMRR vs Die Temperature

Open Loop Gain and Phase vs Frequency

Open Loop Voltage Gain vs Die Temperature

Closed Loop Output Impedance vs Frequency
Typical Performance Curves — Contd.

**Large Signal Step Response,\nV_S = \pm 3V**

- \( V_{IN} = 0.2V \text{ to } 1.45V \)
- \( V_S = \pm 3V \)
- \( R_L = 150\Omega \)
- \( A_V = \pm 1 \)

**Large Signal Step Response,\nV_S = \pm 5V**

- \( V_{IN} = 0.2V \text{ to } 3.0V \)
- \( V_S = \pm 5V \)
- \( R_L = 150\Omega \)
- \( A_V = \pm 1 \)

**Large Signal Step Response,\nV_S = \pm 12V**

- \( V_{IN} = 0.3V \text{ to } 8V \)
- \( V_S = \pm 12V \)
- \( R_L = 150\Omega \)
- \( A_V = \pm 1 \)

**Small Signal Step Response**

- \( V_{IN} = 0.2V \text{ to } 0.6V \)
- \( V_S = \pm 5V \)
- \( R_L = 150\Omega \)
- \( A_V = \pm 1 \)

**Slew Rate vs Temperature**

- \( V_S = \pm 5V \)
- \( R_L = 150\Omega \text{ to GND} \)
- \( A_V = \pm 1 \)
- \( R_F = 0 \)

**Settling Time vs Settling Accuracy**

- \( V_S = \pm 5V \)
- \( \Delta V = \pm 2.5V \)
- \( R_L = 500\Omega \)
- \( A_V = \pm 1, R_F = 0 \)

**Voltage and Current Noise vs Frequency**

- \( e_n = 48\mu V/\sqrt{Hz} \)
- \( b = 1.25pA/\sqrt{Hz} \)
Typical Performance Curves — Contd.

**Differential Gain for Single Supply Operation**

- \( V_S = +5V, +12V \)
- \( R_L = 150\Omega \)
- \( A_v = +2 \)
- \( R_T = 1k\Omega \)

**Differential Phase for Single Supply Operation**

- \( V_S = +5V \)
- \( V_S = +12V \)
- \( R_L = 150\Omega \)
- \( A_v = +2 \)
- \( R_T = 1k\Omega \)

**Differential Gain and Phase for Dual Supply Operation**

- \( V_S = \pm 5V \)
- \( V_S = +12V \)
- \( R_L = 150\Omega \)
- \( A_v = +2 \)
- \( R_T = 1k\Omega \)

**2nd and 3rd Harmonic Distortion vs Frequency**

- \( V_{OUT} = 0V \) to +2V
- \( V_S = +5V \)
- \( R_L = 100\Omega \)

**2nd and 3rd Harmonic Distortion vs Frequency**

- \( V_{OUT} = 0.1V \) to 2.1V
- \( V_S = +5V \)
- \( R_L = 100\Omega \)

**2nd and 3rd Harmonic Distortion vs Frequency**

- \( V_{OUT} = -1V \) to +1V
- \( V_S = \pm 5V \)
- \( R_L = 100\Omega \)

**Output Voltage Swing vs Frequency for THD < 0.1%**

- \( V_S = +12V \)
- \( A_v = +1 \)
- \( R_L = 500\Omega \)

**Output Voltage Swing vs Frequency for Unlimited Distortion**

- \( V_S = +12V \)
- \( A_v = +1 \)
- \( R_L = 150\Omega \)

**Output Current vs Die Temperature**

- \( V_S = \pm 5V \)
- \( R_L = 10\Omega \)

- \( 75 \) to 145°C

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Typical Performance Curves — Contd.

Supply Current vs Supply Voltage (per amplifier)

![Supply Current vs Supply Voltage](image1)

Supply Current vs Die Temperature (per amplifier)

![Supply Current vs Die Temperature](image2)

Input Resistance vs Die Temperature

![Input Resistance vs Die Temperature](image3)

Offset Voltage vs Die Temperature (4 Samples)

![Offset Voltage vs Die Temperature](image4)

Input Bias Current vs Input Voltage

![Input Bias Current vs Input Voltage](image5)

Input Offset Current and Input Bias Current vs Die Temperature

![Input Offset Current and Input Bias Current vs Die Temperature](image6)

Positive Output Voltage Swing vs Die Temperature, \(R_L = 1500 \Omega\) to GND

![Positive Output Voltage Swing vs Die Temperature](image7)

Negative Output Voltage Swing vs Die Temperature, \(R_L = 1500 \Omega\) to GND

![Negative Output Voltage Swing vs Die Temperature](image8)

Clamp Accuracy vs Die Temperature

![Clamp Accuracy vs Die Temperature](image9)
Typical Performance Curves — Contd.

Clamp Accuracy

RL = 150Ω

\[ V_{\text{CLAMP}} = 1.2V \]
\[ V_{\text{CLAMP}} = 1.9V \]
\[ V_{\text{CLAMP}} = 2.7V \]
\[ V_{\text{CLAMP}} = 3.4V \]

\[ V_{\text{IN}} (V) \]

\[ V_{\text{OUT}} - V_{\text{CLAMP}} (mV) \]

Enable Response for a Family of DC Inputs

\[ V_{\text{ENABLE}} = +1, \; R_L = 150Ω, \; V_S = +5V \]

Disable/Enable Response for a Family of Sine Waves

\[ V_{\text{IN}} (V) \]

\[ V_{\text{OUT}} (V) \]

\[ V_{\text{ENABLE}} \]

\[ 50 \text{ ns/div} \]
Typical Performance Curves — Contd.

**EL2257**
- Channel to Channel
- Isolation vs Frequency

**EL2357**
- Channel to Channel
- Isolation vs Frequency

**14-Lead Plastic SO**
- Maximum Power Dissipation
  - vs Ambient Temperature

**16-Lead Plastic DIP**
- Maximum Power Dissipation
  - vs Ambient Temperature
Simplified Schematic (one channel)
Applications Information

Product Description
The EL2257C/EL2357C are the industries fastest single supply operational amplifiers. Connected in voltage follower mode, their -3 dB bandwidth is 125 MHz while maintaining a 275 V/µs slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2257C/EL2357C allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where the GND pin is connected to the ground plane, a single 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor from the VS+ pin to the GND pin will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation
The EL2257C/EL2357C have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2257C/EL2357C will operate on dual supplies ranging from ±1.35V to ±6V. With a single-supply, the EL2257C/EL2357C will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 11 and 4 (14 and 3) are the power supply pins on the EL2257C (EL2357C). The positive power supply is connected to pin 11 (14). When used in single supply mode, pin 4 (3) is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4 (3).

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2257C/EL2357C have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2257C/EL2357C have an input range which spans from 0V to 3.8V.

The output range of the EL2257C/EL2357C is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail with a 1 kΩ load. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ±4V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.

Choice Of Feedback Resistor, RF
The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the
Applications Information — Contd.

time domain and peaking in the frequency domain. Therefore, \( R_F \) has some maximum value which should not be exceeded for optimum performance. If a large value of \( R_F \) must be used, a small capacitor in the few picofarad range in parallel with \( R_F \) can help to reduce this ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, \( R_F + R_G \) appear in parallel with \( R_L \) for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, \( R_F \) has a minimum value that should not be exceeded for optimum performance.

For \( A_V = +1 \), \( R_F = 0 \Omega \) is optimum. For \( A_V = -1 \) or +2 (noise gain of 2), optimum response is obtained with \( R_F \) between 500\( \Omega \) and 1 k\( \Omega \). For \( A_V = -4 \) or +5 (noise gain of 5), keep \( R_F \) between 2 k\( \Omega \) and 10 k\( \Omega \).

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150\( \Omega \), because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2257C/EL2357C are specified with the black level of the output video signal set to +1.2V. This allows ample room for the sync pulse even in a gain of +2 configuration. This results in dG and dP specifications of 0.05% and 0.05° while driving 150\( \Omega \) at a gain of +2. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply dG and dP curves for \( R_L = 150 \Omega \), if the output black level clamp is reduced from 1.2V to 0.6V dG/dP will increase from 0.05%/0.05° to 0.08%/0.25°. Note that in a gain of +2 configuration, this is the lowest black level allowed such that the sync tip doesn't go below 0V.

If your application requires that the output goes to ground, then the output stage of the EL2257C/EL2357C, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and dG and dP will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as 1 k\( \Omega \), if the input black level is kept above 1.25V, dG and dP are a respectable 0.03% and 0.03°.

For other biasing conditions see the Differential Gain and Differential Phase vs. Input Voltage curves.

Output Drive Capability

In spite of their moderately low 5 mA of supply current, the EL2257C/EL2357C are capable of providing ±100 mA of output current into a 10\( \Omega \) load, or ±60 mA into 50\( \Omega \). With this large output current capability, a 50\( \Omega \) load can be driven to ±3V with \( V_S = \pm 5V \), making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2257C/EL2357C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5\( \Omega \) and 50\( \Omega \)) can be placed in series with the output to eliminate most peaking. The gain resistor \( R_G \) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.
Applications Information — Contd.

Disable/Power-Down

Each amplifier in the EL2257C/EL2357C can be individually disabled, placing each output in a high-impedance state. The disable or enable action takes only about 40 ns. When all amplifiers are disabled, the total supply current is reduced to 0 mA, thereby eliminating all power consumption by the EL2257C/EL2357C. The EL2257C/EL2357C amplifier’s power down can be controlled by standard CMOS signal levels at each ENABLE pin. The applied CMOS signal is relative to the GND pin. For example, if a single +5V supply is used, the logic voltage levels will be +0.5V and +2.0V. If using dual ±5V supplies, the logic levels will be -4.5V and -3.0V. Letting all ENABLE pins float will disable the EL2257C/EL2357C. If the power-down feature is not desired, connect all ENABLE pins to the Vgs+ pin. The guaranteed logic levels of +0.5V and +2.0V are not standard TTL levels of +0.8V and +2.0V, so care must be taken if standard TTL will be used to drive the ENABLE pins.

Output Voltage Clamp

The EL2257C/EL2357C amplifiers have an output voltage clamp. This clamping action is fast, being activated almost instantaneously, and being deactivated in < 7 ns, and prevents the output voltage from going above the preset clamp voltage. This can be very helpful when the EL2257C/EL2357C are used to drive an A/D converter, as some converters can require long times to recover if overdriven. The output voltage remains at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. For example, if the EL2257C/EL2357C is connected in a gain of 2, and +3V DC is applied to the CLAMP pin, any voltage higher than +1.5V at the inputs will be clamped and +3V will be seen at the output. Each amplifier of the EL2257C have their own CLAMP pin, so individual clamp levels may be set, whereas a single CLAMP pin controls the clamp level of the EL2357C.
Applications Information — Contd.

Figure 3 shows the output of amplifier A of the same circuit being driven by a 0.5V to 2.75V square wave as the clamp voltage is varied from 1.0V to 2.5V, as well as the unclamped output signal. The rising edge of the signal is clamped to the voltage applied to the CLAMP pin almost instantaneously. The output recovers from the clamped mode within 5–7 ns, depending on the clamp voltage. Even when the CLAMP pin is taken 0.2V below the minimum 1.2V specified, the output is still clamped and recovers in about 11 ns.

The clamp accuracy is affected by 1) the CLAMP pin voltage, 2) the input voltage, and 3) the load resistor. Depending upon the application, the accuracy may be as little as a few tens of millivolts up to a few hundred millivolts. Be sure to allow for these inaccuracies when choosing the clamp voltage. Curves of Clamp Accuracy vs. $V_{CLAMP}$ and $V_{IN}$ for 3 values of $R_L$ are included in the Typical Performance Curves Section.

Unlike amplifiers that clamp at the input and are therefore limited to non-inverting applications only, the EL2257C/EL2357C output clamp architecture works for both inverting and non-inverting gain applications. There is also no maximum voltage difference limitation between $V_{IN}$ and $V_{CLAMP}$ which is common on input clamped architectures.

The voltage clamp operates for any voltage between $+1.2V$ above the GND pin, and the minimum output voltage swing, $V_{OP}$. Forcing the CLAMP pin much below $+1.2V$ can saturate transistors and should therefore be avoided. Forcing the CLAMP pin above $V_{OP}$ simply deactivates the CLAMP feature. In other words, one cannot expect to clamp any voltage higher than what the EL2257C/EL2357C can drive to in the first place. If the clamp feature is not desired, either let the CLAMP pin float or connect it to the $V_{S+}$ pin.

**EL2257C/EL2357C Comparator Application**

The EL2257C/EL2357C can be used as a very fast, single supply comparator by utilizing the clamp feature. Most op amps used as comparators allow only slow speed operation because of output saturation issues. However, by applying a DC voltage to the CLAMP pin of the EL2257C/EL2357C, the maximum output voltage can be clamped, thus preventing saturation. Figure 4 below is amplifier A of an EL2257C implemented as a comparator. 2.25V DC is applied to the CLAMP pin, as well as the IN- pin. A differential signal is then applied between the inputs. Figure 5 shows the output square wave that results when a $\pm 1V$, 10 MHz triangular wave is applied, while Figure 6 is a graph of propagation delay vs. overdrive as a square wave is presented at the input.
Applications Information — Contd.

Figure 5

Figure 6

Figure 7

Figure 8

Video Sync Pulse Remover Application
All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 7 shows a unity gain connected amplifier A of an EL2257C. Figure 8 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

Multiplexing with the EL2257C/EL2357C
The ENABLE pins on the EL2257C/EL2357C allow for multiplexing applications. Figure 9 shows an EL2357C with all 3 outputs tied together, driving a back terminated 75Ω video load. Three sinewaves of varying amplitudes and frequencies are applied to the three inputs. Logic signals are applied to each of the ENABLE pins to cycle through turning each of the amplifiers on, one at a time. Figure 10 shows the resulting output waveform at VOUT. Switching is complete
Applications Information — Contd.
in about 50 ns. Notice the outputs are tied directly together. Decoupling resistors at each output are not necessary. In fact, adding them approximately doubles the switching time to 100 ns.

Power Dissipation
With the high output drive capability of the EL2257C/EL2357C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2257C/EL2357C to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to [1]:

\[ PD_{\text{MAX}} = \frac{T_{\text{JMAX}} - T_{\text{AMAX}}}{\theta_{JA}} \]  

where:
- \( T_{\text{JMAX}} \) = Maximum Junction Temperature
- \( T_{\text{AMAX}} \) = Maximum Ambient Temperature
- \( \theta_{JA} \) = Thermal Resistance of the Package
- \( PD_{\text{MAX}} \) = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

\[ PD_{\text{MAX}} = N \times (V_S + IS_{\text{MAX}} + (V_S - V_{\text{OUT}}) \times \frac{V_{\text{OUT}}}{R_L}) \]  

where:
- \( N \) = Number of amplifiers
- \( V_S \) = Total Supply Voltage
- \( IS_{\text{MAX}} \) = Maximum Supply Current per amplifier
- \( V_{\text{OUT}} \) = Maximum Output Voltage of the Application
- \( R_L \) = Load Resistance tied to Ground

If we set the two \( PD_{\text{MAX}} \) equations, [1] and [2], equal to each other, and solve for \( V_S \), we can get a family of curves for various loads and output voltages according to [3]:

\[ V_S = \frac{R_L \times (T_{\text{JMAX}} - T_{\text{AMAX}})}{N \times \theta_{JA}} + (V_{\text{OUT}})^2 \]

\[ \frac{N \times \theta_{JA}}{(IS \times R_L) + V_{\text{OUT}}} \]

Short Circuit Current Limit
The EL2257C/EL2357C have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100 mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds \( \pm 90 \) mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.
Applications Information — Contd.

Figures 11 and 12 below show total single supply voltage $V_S$ vs. $R_L$ for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of $T_A = +85^\circ C$ and $I_S = 6.5$ mA per amplifier.

**Figure 11**

**Figure 12**
EL2257C/EL2357C Macromodel -
(one channel)

* Revision A, October 1995
* Pin numbers reflect a standard single opamp.
* When not being used, the clamp pin, pin 1,
* should be connected to +Vsupply, pin 7
* Connections: + input
  * | | - input
  * | | + Vsupply
  * | | -Vsupply
  * | | output
  * | | clamp

subckt EL2257/el 3 2 7 4 6 1

* Input Stage
  i1 7 10 250mA
  i2 7 11 250mA
  r1 10 11 4K
  q1 12 2 10 qpa
  q2 13 3 11 qpa
  r2 12 4 100
  r3 13 4 100

* Second Stage & Compensation
  gm 15 4 13 12 4.6m
  r4 15 4 15Meg
  c1 15 4 0.36pF

* Poles
  c1 17 4 15 4 1.0
  r6 17 25 400
  c3 25 4 1pF
  r7 25 18 500
  c4 18 4 1pF

* Output Stage & Clamp
  i3 20 4 1.0mA
  q3 7 23 20 qn
  q4 7 18 19 qn
  q5 7 18 21 qn
  q6 4 20 22 qp
  q7 7 23 18 qn
  d1 19 20 da
  d2 18 1 da
  r8 21 6 2
  r9 22 6 2
  r10 18 21 10k
  r11 7 23 100k
  d3 23 24 da
  d4 24 4 da
  d5 23 18 da

* Power Supply Current
  ips 7 4 3.2mA

* Models
  .model qn npn(is=800e-18 bf=150 tf=0.02nS)
  .model qpa pnp(is=810e-18 bf=50 tf=0.02nS)
  .model qp pnp(is=800e-18 bf=54 tf=0.02nS)
  .model da d(tt=0nS)
.ends
EL2257C/EL2357C Macromodel - (one channel) — Contd.
EL2160C
130 MHz Current Feedback Amplifier

Features
• 130 MHz 3 dB bandwidth  
  \((AV = +2)\)
• 180 MHz 3 dB bandwidth  
  \((AV = +1)\)
• 0.01% differential gain,  
  \(RL = 500\Omega\)
• 0.01° differential phase,  
  \(RL = 500\Omega\)
• Low supply current, 8.5 mA
• Wide supply range, ±2V to ±15V
• 80 mA output current (peak)
• Low cost
• 1500 V/μs slew rate
• Input common mode range to within 1.5V of supplies
• 35 ns settling time to 0.1%

Applications
• Video amplifiers
• Cable drivers
• RGB amplifiers
• Test equipment amplifiers
• Current to voltage converter

General Description
The EL2160C is a current feedback operational amplifier with 
-3 dB bandwidth of 130 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

The EL2160C is designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.1°).

The amplifier can operate on any supply voltage from 4V (±2V) to 33V (±16.5V), yet consume only 8.5 mA at any supply voltage. Using industry standard pinouts, the EL2160C is available in 8-pin P-DIP and 8-pin SO packages. For dual and quad applications, please see the EL2260C/EL2460C datasheet.


Connection Diagram

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2160CN</td>
<td>−40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0631</td>
</tr>
<tr>
<td>EL2160CS</td>
<td>−40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0627</td>
</tr>
</tbody>
</table>

Top View
Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>25°C</td>
<td>2</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>TC (V_{OS})</td>
<td>Average Offset Voltage Drift (Note 1)</td>
<td>Full</td>
<td>10</td>
<td>V</td>
<td>(\mu V/^\circ C)</td>
<td></td>
</tr>
<tr>
<td>(+I_{IN})</td>
<td>(+) Input Current</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>25°C</td>
<td>0.5</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(-I_{IN})</td>
<td>(-) Input Current</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>25°C</td>
<td>5</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio (Note 2)</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>25°C</td>
<td>50</td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>(-ICMR)</td>
<td>(-) Input Current Common Mode Rejection (Note 2)</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>25°C</td>
<td>0.2</td>
<td>I</td>
<td>(\mu A/V)</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Note 3)</td>
<td></td>
<td></td>
<td>25°C</td>
<td>75</td>
<td>II</td>
</tr>
<tr>
<td>(-IPSR)</td>
<td>(-) Input Current Power Supply Rejection (Note 3)</td>
<td>25°C</td>
<td>0.2</td>
<td>I</td>
<td>(\mu A/V)</td>
<td></td>
</tr>
</tbody>
</table>

Open Loop DC Electrical Characteristics
\(V_S = \pm 15V, R_L = 150\Omega, T_A = 25^\circ C\) unless otherwise specified.
### Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15\text{V}, R_L = 150\Omega, T_A = 25^\circ\text{C}$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{OL}$</td>
<td>Transimpedance (Note 4)</td>
<td>$V_S = \pm 15\text{V}$, $R_L = 400\Omega$</td>
<td>25°C</td>
<td>500</td>
<td>2000</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5\text{V}$, $R_L = 150\Omega$</td>
<td>25°C</td>
<td>500</td>
<td>1800</td>
<td>I</td>
</tr>
<tr>
<td>$+R_{IN}$</td>
<td>+ Input Resistance</td>
<td></td>
<td>25°C</td>
<td>1.5</td>
<td>3.0</td>
<td>II</td>
</tr>
<tr>
<td>$+C_{IN}$</td>
<td>+ Input Capacitance</td>
<td></td>
<td>25°C</td>
<td>2.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CMIR</td>
<td>Common Mode Input Range</td>
<td>$V_S = \pm 15\text{V}$</td>
<td>25°C</td>
<td>±13.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CMIR</td>
<td>Common Mode Input Range</td>
<td>$V_S = \pm 5\text{V}$</td>
<td>25°C</td>
<td>±3.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing</td>
<td>$R_L = 400\Omega$, $V_S = \pm 15\text{V}$</td>
<td>25°C</td>
<td>±12</td>
<td>±13.5</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 150\Omega$, $V_S = \pm 15\text{V}$</td>
<td>25°C</td>
<td>±12</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 150\Omega$, $V_S = \pm 5\text{V}$</td>
<td>25°C</td>
<td>±3.0</td>
<td>±3.7</td>
<td>I</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Output Short Circuit Current (Note 5)</td>
<td>$V_S = \pm 5\text{V}$, $V_S = \pm 15\text{V}$</td>
<td>25°C</td>
<td>60</td>
<td>100</td>
<td>150</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$V_S = \pm 15\text{V}$</td>
<td>25°C</td>
<td>8.5</td>
<td>12.0</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5\text{V}$</td>
<td>25°C</td>
<td>6.4</td>
<td>9.5</td>
<td>I</td>
</tr>
</tbody>
</table>
## Closed Loop AC Electrical Characteristics

$V_S = \pm 15\, \text{V}, \, A_V = +2, \, R_P = 560\, \Omega, \, R_L = 150\, \Omega, \, T_A = 25^\circ\, \text{C}$ unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>BW</td>
<td>$-3, \text{dB Bandwidth}$ (Note 8)</td>
<td>$V_S = \pm 15, \text{V}, , A_V = +2$</td>
<td>130</td>
<td>$V$</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15, \text{V}, , A_V = +1$</td>
<td>180</td>
<td>$V$</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5, \text{V}, , A_V = +2$</td>
<td>100</td>
<td>$V$</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5, \text{V}, , A_V = +1$</td>
<td>110</td>
<td>$V$</td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (Notes 6, 8)</td>
<td>$R_L = 400, \Omega$</td>
<td>1000</td>
<td>1500</td>
<td>IV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_P = 1, \text{k}, \Omega, , R_G = 110, \Omega$</td>
<td>$R_L = 400, \Omega$</td>
<td>1500</td>
<td>$V$</td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Rise Time, Fall Time, (Note 8)</td>
<td>$V_{OUT} = \pm 500, \text{mV}$</td>
<td>2.7</td>
<td>$V$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>Propagation Delay (Note 8)</td>
<td></td>
<td>3.2</td>
<td>$V$</td>
<td>ns</td>
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<tr>
<td>OS</td>
<td>Overshoot (Note 8)</td>
<td>$V_{OUT} = \pm 500, \text{mV}$</td>
<td>0</td>
<td>$V$</td>
<td>%</td>
</tr>
<tr>
<td>$t_s$</td>
<td>0.1% Settling Time (Note 8)</td>
<td>$V_{OUT} = \pm 10, \text{V}$</td>
<td>35</td>
<td>$V$</td>
<td>ns</td>
</tr>
<tr>
<td>$dG$</td>
<td>Differential Gain (Notes 7, 8)</td>
<td>$R_L = 150, \Omega$</td>
<td>0.025</td>
<td>$V$</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 500, \Omega$</td>
<td>0.005</td>
<td>$V$</td>
<td>%</td>
</tr>
<tr>
<td>$dP$</td>
<td>Differential Phase (Notes 7, 8)</td>
<td>$R_L = 150, \Omega$</td>
<td>0.1</td>
<td>$V$</td>
<td>deg ($^\circ$)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 500, \Omega$</td>
<td>0.005</td>
<td>$V$</td>
<td>deg ($^\circ$)</td>
</tr>
</tbody>
</table>

**Note 1:** Measured from $T_{MIN}$ to $T_{MAX}$.

**Note 2:** $V_{CM} = \pm 10\, \text{V}$ for $V_S = \pm 15\, \text{V}$ and $T_A = 25^\circ\, \text{C}$

$V_{CM} = \pm 3\, \text{V}$ for $V_S = \pm 5\, \text{V}$ and $T_A = 25^\circ\, \text{C}$

**Note 3:** The supplies are moved from $\pm 2.5\, \text{V}$ to $\pm 15\, \text{V}$.

**Note 4:** $V_{OUT} = \pm 7\, \text{V}$ for $V_S = \pm 15\, \text{V}$, and $V_{OUT} = \pm 2\, \text{V}$ for $V_S = \pm 5\, \text{V}$.

**Note 5:** A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

**Note 6:** Slew Rate is with $V_{OUT}$ from $+10\, \text{V}$ to $-10\, \text{V}$ and measured at the 25% and 75% points.

**Note 7:** DC offset from $-0.714\, \text{V}$ through $+0.714\, \text{V}$, AC amplitude 286 mV$_{\text{p-p}}$, $f = 3.58\, \text{MHz}$.

**Note 8:** All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Frequency Response for Various $R_L$

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

Frequency Response for Various $R_F$ and $R_C$

3 dB Bandwidth vs Supply Voltage for $A_Y = -1$

Peaking vs Supply Voltage for $A_Y = -1$

3 dB Bandwidth vs Temperature for $A_Y = -1$
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_V = +1$

Peaking vs Supply Voltage for $A_V = +1$

3 dB Bandwidth vs Temperature for $A_V = +1$

3 dB Bandwidth vs Supply Voltage for $A_V = +2$

Peaking vs Supply Voltage for $A_V = +2$

3 dB Bandwidth vs Temperature for $A_V = +2$

3 dB Bandwidth vs Supply Voltage for $A_V = +10$

Peaking vs Supply Voltage for $A_V = +10$

3 dB Bandwidth vs Temperature for $A_V = +10$

Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_V = +1$

Peaking vs Supply Voltage for $A_V = +1$

3 dB Bandwidth vs Temperature for $A_V = +1$

3 dB Bandwidth vs Supply Voltage for $A_V = +2$

Peaking vs Supply Voltage for $A_V = +2$

3 dB Bandwidth vs Temperature for $A_V = +2$

3 dB Bandwidth vs Supply Voltage for $A_V = +10$

Peaking vs Supply Voltage for $A_V = +10$

3 dB Bandwidth vs Temperature for $A_V = +10$
Typical Performance Curves — Contd.

Frequency Response for Various $C_L$

Frequency Response for Various $C_{IN}$

PSRR and CMRR vs Frequency

2nd and 3rd Harmonic Distortion vs Frequency

Transimpedance ($R_{OL}$) vs Frequency

Voltage and Current Noise vs Frequency

Closed-Loop Output Impedance vs Frequency

Transimpedance ($R_{OL}$) vs Die Temperature

Typical Performance Curves — Contd.
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)

Supply Current vs Die Temperature

Supply Current vs Supply Voltage

Input Resistance vs Die Temperature

Input Current vs Die Temperature

Input Bias Current vs Input Voltage

Output Voltage Swing vs Die Temperature

Short Circuit Current vs Die Temperature

PSRR & CMRR vs Die Temperature
Typical Performance Curves — Contd.

Differential Gain vs DC Input Voltage, \( R_L = 150 \)

Differential Phase vs DC Input Voltage, \( R_L = 150 \)

Small Signal Pulse Response

Differential Gain vs DC Input Voltage, \( R_L = 500 \)

Differential Phase vs DC Input Voltage, \( R_L = 500 \)

Large Signal Pulse Response

Slew Rate vs Supply Voltage

Slew Rate vs Temperature

Setting Time vs Settling Accuracy

Settling Time Accuracy %
Typical Performance Curves — Contd.

Long Term Settling Error

<table>
<thead>
<tr>
<th>Residual Settling Error (V)</th>
<th>Time (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.04</td>
<td>0</td>
</tr>
<tr>
<td>0.03</td>
<td>20</td>
</tr>
<tr>
<td>0.02</td>
<td>40</td>
</tr>
<tr>
<td>0.01</td>
<td>60</td>
</tr>
<tr>
<td>0.005</td>
<td>80</td>
</tr>
<tr>
<td>0.002</td>
<td>100</td>
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</table>

ΔV = ±10 V
Rc = 560
Rs = 1k
Vs = ±15 V

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

<table>
<thead>
<tr>
<th>Power Dissipation (W)</th>
<th>Ambient Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>-40</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>25</td>
</tr>
<tr>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>1</td>
<td>75</td>
</tr>
<tr>
<td>0.5</td>
<td>100</td>
</tr>
</tbody>
</table>

TJmax = 150°C
θJA = 95°C/W
θJC = 50°C/W

INFINITE HEAT SINK
FREE AIR NO HEAT SINK

8-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature

<table>
<thead>
<tr>
<th>Power Dissipation (W)</th>
<th>Ambient Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>-40</td>
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<tr>
<td>4</td>
<td>0</td>
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<tr>
<td>3</td>
<td>25</td>
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<tr>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>1</td>
<td>75</td>
</tr>
<tr>
<td>0.5</td>
<td>100</td>
</tr>
</tbody>
</table>

TJmax = 150°C
θJA = 165°C/W
θJC = 45°C/W

INFINITE HEAT SINK
FREE AIR NO HEAT SINK

Burn-In Circuit

EL2160C

1k

1
2
3
4
5
6
7
8

V+ +15V

V- -15V

2060-7

2060-8
Differential Gain and Phase Test Circuit

Simplified Schematic (One Amplifier)
Applications Information

Product Description
The EL2160C is a current mode feedback amplifier that offers wide bandwidth and good video specifications at a moderately low supply current. It is built using Elantec's proprietary complementary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL2160C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, \( R_F \), and then the gain is set by picking the gain resistor, \( R_G \). The curves at the beginning of the Typical Performance Curves section show the effect of varying both \( R_F \) and \( R_G \). The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below \( \frac{1}{4} \)". The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 \( \mu \)F tantalum capacitor in parallel with a 0.01 \( \mu \)F ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input
Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2160C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of \( C_{IN} \) emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2 pF of capacitance at the \( V_{IN} \) pin for the case of \( A_V = +2 \). Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values
The EL2160C has been designed and specified with \( R_F = 560 \Omega \) for \( A_V = +2 \). This value of feedback resistor yields extremely flat frequency response with little to no peaking out to 130 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing \( R_F \) to 430\( \Omega \), bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of \( R_F \) to 360\( \Omega \) increases the bandwidth to 195 MHz with about 2.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature
 Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2160C was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With \( V_S = \pm 15 \)V and \( A_V = +2 \), the bandwidth only varies from 150 MHz to 110 MHz over the entire die junction temperature range of \( 0^\circ C < T < 150^\circ C \).
Applications Information — Contd.

Supply Voltage Range
The EL2160C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the 3 dB bandwidth at $A_V = +2$ is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2160C at ±2V supplies, $A_V = +2$, $R_F = R_G = 560\Omega$, driving a load of 150Ω, showing a clean ±600 mV signal at the output.

If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2160C.

Settling Characteristics
The EL2160C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2160C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation
The EL2160C amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2160C remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{J\text{MAX}} - T_{A\text{MAX}}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = 2 \cdot V_S \cdot I_S + (V_S - V_{OUT}) \cdot \frac{V_{OUT}}{R_L}$$

where $I_S$ is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL2160C maintains almost constant supply...
Applications Information — Contd.
current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn’t come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

The EL2160C consumes typically 8.5 mA and maximum 11.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum values if it cannot reach half supply. If we set the two $P_{\text{DMAX}}$ equations equal to each other, and solve for $V_S$, we can get a family of curves for various loads and output voltages according to:

$$V_S = \frac{R_L \cdot (T_{JMAX} - T_{A\text{MAX}})}{\theta_{JA}} + \frac{(V_{OUT})^2}{(2 \cdot I_S \cdot R_L) + V_{OUT}}$$

The following curves show supply voltage ($\pm V_S$) vs $R_{LOAD}$ for various output voltage swings for the 2 different packages. The curves assume worst case conditions of $T_A = +85^\circ$C and $I_S = 11$ mA.

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit
The EL2160C has an internal current limit that protects the circuit in the event of the output being shorted to ground. This limit is set at 100 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 65 mA. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2160C to survive an indefinite short.

Driving Cables and Capacitive Loads
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2160C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, $R_G$, can be chosen to make up for the gain loss created by this additional series resistor at the output.
EL2160C Macromodel

* Revision A, November 1993
* AC Characteristics used C_{IN} = 1 \text{ pF}; R_F = 560 \text{ Ohm}
* Connections:
  + input
  - input + V_{supply}
  - V_{supply}
  output

.subckt EL2160C/EL 3 2 7 4 6

* Input Stage
  e1 10 0 3 0 1.0
  vis 10 9 0V
  h2 9 12 vxx 1.0
  r1 2 11 130
  l1 11 12 25nH
  iinp 3 0 0.5 \mu \text{A}
  iinn 2 0 5 \mu \text{A}
  r12 3 0 2 \text{M} \text{eg}

* Slew Rate Limiting
  h1 13 0 vis 600
  r2 13 14 1K
  d1 14 0 dclamp
  d2 0 14 dclamp

* High Frequency Pole
  *e2 30 0 14 0 0.0016666666666
  l3 30 17 0.43 \mu \text{H}
  c5 17 0 0.27 \mu \text{F}
  r5 17 0 500

* Transimpedance Stage
  g1 0 18 17 0 1.0
  ro1 18 0 2 \text{M} \text{eg}
  cdp 18 0 2.285 \text{pF}

* Output Stage
  q1 4 18 19 qp
  q2 7 18 20 qn
  q3 7 19 21 qn
  q4 4 20 22 qp
  r7 21 6 4
  r8 22 6 4
  ios1 7 19 2mA
  ios2 20 4 2mA

* Supply Current
  *ips 7.4 3mA

* Error Terms
  *ivos 0 23 2mA
  vxx 23 0 0V
  e4 24 0 3 0 1.0
  e5 25 0 7 0 1.0
  e6 26 0 4 0 1.0
  r9 24 23 562
  r10 25 23 1K
  r11 26 23 1K

* Models
  .model qn npn (is = 5e-15 bf = 100 tf = 0.1 \text{ns})
  .model qp pnp (is = 5e-15 bf = 100 tf = 0.1 \text{ns})
  .model dclamp d (is = 1e-30 ibv = 0.266 bv = 2.24 n = 4)
.ends
**Features**

- 130 MHz 3 dB bandwidth \((A_v = +2)\)
- 180 MHz 3 dB bandwidth \((A_v = +1)\)
- 0.01% differential gain, \(R_L = 500\Omega\)
- 0.01° differential phase, \(R_L = 500\Omega\)
- Low supply current, 7.5 mA per amplifier
- Wide supply range, ±2V to ±15V
- 80 mA output current (peak)
- Low cost
- 1500 V/\(\mu\)s slew rate
- Input common mode range to within 1.5V of supplies
- 35 ns settling time to 0.1%

**Applications**

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converter

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2260CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2260CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDPO027</td>
</tr>
<tr>
<td>EL2460CN</td>
<td>-40°C to +85°C</td>
<td>14-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2460CS</td>
<td>-40°C to +85°C</td>
<td>14-Pin SOIC</td>
<td>MDPO027</td>
</tr>
</tbody>
</table>

**General Description**

The EL2260C/EL2460C are dual/quad current feedback operational amplifiers with -3 dB bandwidth of 130 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, these amplifiers use current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

The EL2260C/EL2460C are designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (0.01%/0.01°) and double terminated 75Ω cables (0.025%/0.1°).

The amplifiers can operate on any supply voltage from 4V (±2V) to 33V (±16.5V), yet consume only 7.5 mA per amplifier at any supply voltage. Using industry standard pinouts, the EL2260C is available in 8-pin P-DIP and 8-pin SO packages, while the EL2460C is available in 14-pin P-DIP and 14-pin SO packages.

Elantec's facilities comply with MIL-I-45208A and offer applicable quality specifications. For information on Elantec’s processing, see the Elantec document, QRA-1: Elantec’s Processing—Monolithic Products.
EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Absolute Maximum Ratings ($T_A = 25^\circ C$)

- Voltage between $V_{S}^+$ and $V_{S}^-$: $+33V$
- Voltage between $+IN$ and $-IN$: $\pm 6V$
- Current into $+IN$ or $-IN$: 10 mA
- Internal Power Dissipation: See Curves

Operating Ambient Temperature Range: $-40^\circ C$ to $+85^\circ C$
Operating Junction Temperature: $150^\circ C$
Storage Temperature Range: $-65^\circ C$ to $+150^\circ C$
Output Current: $\pm 50 mA$

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LT877 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level | Test Procedure
--- | ---
I | 100% production tested and QA sample tested per QA test plan QCX0021.
II | 100% production tested at $T_A = 25^\circ C$ and QA sample tested at $T_A = 25^\circ C$.
III | $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0022.
IV | QA sample tested per QA test plan QCX0022.
V | Parameter is guaranteed (but not tested) by Design and Characterization Data.

Open Loop DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 150\Omega$, $T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>Min Typ Max</td>
<td>EL2260C EL2460C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>TC $V_{OS}$</td>
<td>Average Offset Voltage Drift (Note 1)</td>
<td></td>
<td>Full</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>$+I_{IN}$</td>
<td>$+ Input Current$</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>$-I_{IN}$</td>
<td>$- Input Current$</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>5</td>
<td>25</td>
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<td></td>
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<td>$T_{MIN}, T_{MAX}$</td>
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<td>35</td>
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<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio (Note 2)</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>Full</td>
<td>50</td>
<td>55</td>
</tr>
<tr>
<td>$-ICMR$</td>
<td>$- Input Current Common Mode Rejection (Note 2)$</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>0.2</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Note 3)</td>
<td></td>
<td>Full</td>
<td>75</td>
<td>95</td>
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<tr>
<td>$-IPSR$</td>
<td>$- Input Current Power Supply Rejection (Note 3)$</td>
<td></td>
<td>$25^\circ C$</td>
<td>0.2</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_{MIN}, T_{MAX}$</td>
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<td>5</td>
</tr>
</tbody>
</table>
Open Loop DC Electrical Characteristics — Contd.

Vs = ±15V, RL = 150Ω, TA = 25°C unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
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<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>ROL</td>
<td>Trans impedance</td>
<td>Vs = ±15V, RL = 400Ω</td>
<td>25°C, TMIN, TMAX</td>
<td>500</td>
<td>250</td>
<td>2000</td>
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<tr>
<td></td>
<td></td>
<td>Vs = ±5V, RL = 150Ω</td>
<td>25°C, TMIN, TMAX</td>
<td>500</td>
<td>250</td>
<td>1800</td>
</tr>
<tr>
<td>+RIN</td>
<td>+Input Resistance</td>
<td>Full</td>
<td></td>
<td>1.5</td>
<td>3.0</td>
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<tr>
<td>+CIN</td>
<td>+Input Capacitance</td>
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<td>2.5</td>
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<tr>
<td>CMIR</td>
<td>Common Mode Input Range</td>
<td>Vs = ±15V</td>
<td>25°C</td>
<td>±13.5</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vs = ±5V</td>
<td>25°C</td>
<td>±3.5</td>
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<td></td>
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<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td>RL = 400Ω, Vs = ±15V</td>
<td>25°C, TMIN, TMAX</td>
<td>±12</td>
<td>±11</td>
<td>±13.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RL = 150Ω, Vs = ±5V</td>
<td>25°C, TMIN, TMAX</td>
<td>±3.0</td>
<td>±2.5</td>
<td>±3.7</td>
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<tr>
<td>ISC</td>
<td>Output Short Circuit Current</td>
<td>Vs = ±5V, Vs = ±15V</td>
<td>25°C</td>
<td>60</td>
<td>100</td>
<td>150</td>
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<tr>
<td>IS</td>
<td>Supply Current (Per Amplifier)</td>
<td>Vs = ±15V</td>
<td>25°C, TMIN, TMAX</td>
<td>7.5</td>
<td></td>
<td>11.0</td>
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<td></td>
<td></td>
<td>Vs = ±5V</td>
<td>25°C, TMIN, TMAX</td>
<td>5.4</td>
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<td>8.5</td>
</tr>
</tbody>
</table>
## Closed Loop AC Electrical Characteristics

$V_S = \pm 15V, A_V = +2, R_F = 560\Omega, R_L = 150\Omega, T_A = 25^\circ C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Test Level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V, A_V = +2$</td>
<td>130</td>
<td>V MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V, A_V = +1$</td>
<td>180</td>
<td>V MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V, A_V = +2$</td>
<td>100</td>
<td>V MHz</td>
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<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V, A_V = +1$</td>
<td>110</td>
<td>V MHz</td>
</tr>
<tr>
<td>BW</td>
<td>$-3$ dB Bandwidth (Note 8)</td>
<td>$R_L = 400\Omega$</td>
<td>1000</td>
<td>1500 IV V/μs</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (Notes 6, 8)</td>
<td>$R_F = 1K\Omega, R_Q = 110\Omega$</td>
<td>1500 V</td>
<td>V/μs</td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Rise Time, Fall Time, (Note 8)</td>
<td>$V_{OUT} = \pm 500mV$</td>
<td>2.7</td>
<td>V ns</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>Propagation Delay (Note 8)</td>
<td>$V_{OUT} = \pm 500mV$</td>
<td>3.2</td>
<td>V ns</td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot (Note 8)</td>
<td>$V_{OUT} = \pm 500mV$</td>
<td>0</td>
<td>V %</td>
</tr>
<tr>
<td>$t_s$</td>
<td>0.1% Settling Time (Note 8)</td>
<td>$V_{OUT} = \pm 10V$</td>
<td>35</td>
<td>V ns</td>
</tr>
<tr>
<td>$dG$</td>
<td>Differential Gain (Notes 7, 8)</td>
<td>$R_L = 150\Omega$</td>
<td>0.025</td>
<td>V %</td>
</tr>
<tr>
<td>$dP$</td>
<td>Differential Phase (Notes 7, 8)</td>
<td>$R_L = 150\Omega$</td>
<td>0.1 deg (°)</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Measured from $T_{MIN}$ to $T_{MAX}$.

**Note 2:** $V_{CM} = \pm 10V$ for $V_S = \pm 15V$ and $T_A$ = Full

$V_{CM} = \pm 3V$ for $V_S = \pm 5V$ and $T_A = 25^\circ C$

$V_{CM} = \pm 2V$ for $V_S = \pm 5V$ and $T_A = T_{MIN}, T_{MAX}$

**Note 3:** The supplies are moved from $\pm 2.5V$ to $\pm 15V$.

**Note 4:** $V_{OUT} = \pm 7V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.

**Note 5:** A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

**Note 6:** Slew Rate is with $V_{OUT}$ from $+10V$ to $-10V$ and measured at the 25% and 75% points.

**Note 7:** DC offset from $-0.714V$ through $+0.714V$, AC amplitude 286 mV<sub>pp</sub>, $f = 3.58$ MHz.

**Note 8:** All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Frequency Response for Various $R_L$

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

Frequency Response for Various $R_F$ and $R_G$

3 dB Bandwidth vs Supply Voltage for $A_V = -1$

Peaking vs Supply Voltage for $A_V = -1$

3 dB Bandwidth vs Temperature for $A_V = -1$
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_V = +1$

- $R_F = 360$
- $R_F = 430$
- $R_F = 560$
- $R_F = 750$
- $V_{IN} = 150$

Peaking vs Supply Voltage for $A_V = +1$

- $R_F = 360$
- $R_F = 430$
- $R_F = 560$
- $R_F = 750$

3 dB Bandwidth vs Temperature for $A_V = +1$

- $V_S = \pm 15V$
- $V_S = \pm 10V$
- $V_S = \pm 5V$
- $V_S = \pm 2V$

3 dB Bandwidth vs Supply Voltage for $A_V = +2$

- $R_F = 360$
- $R_F = 430$
- $R_F = 560$
- $R_F = 750$
- $V_{IN} = 150$

Peaking vs Supply Voltage for $A_V = +2$

- $R_F = 360$
- $R_F = 430$
- $R_F = 560$
- $R_F = 750$

3 dB Bandwidth vs Temperature for $A_V = +2$

- $V_S = \pm 15V$
- $V_S = \pm 10V$
- $V_S = \pm 5V$
- $V_S = \pm 2V$

3 dB Bandwidth vs Supply Voltage for $A_V = +10$

- $R_F = 150$
- $R_F = 360$
- $R_F = 430$
- $R_F = 560$
- $R_F = 750$

Peaking vs Supply Voltage for $A_V = +10$

- $R_F = 150$
- $R_F = 360$
- $R_F = 430$
- $R_F = 560$
- $R_F = 750$

3 dB Bandwidth vs Temperature for $A_V = +10$

- $V_S = \pm 15V$
- $V_S = \pm 10V$
- $V_S = \pm 5V$
- $V_S = \pm 2V$
Typical Performance Curves — Contd.

- **Frequency Response for Various \( C_L \)**
  - \( C_L = 90\,\text{pF} \)
  - \( C_L = 47\,\text{pF} \)
  - \( C_L = 20\,\text{pF} \)
  - \( C_L = 0\,\text{pF} \)

- **Frequency Response for Various \( C_{IN}^- \)**
  - \( C_{IN}^- = 3\,\text{pF} \)
  - \( C_{IN}^- = 2\,\text{pF} \)
  - \( C_{IN}^- = 1\,\text{pF} \)
  - \( C_{IN}^- = 0\,\text{pF} \)

- **Channel to Channel Isolation vs Frequency**

- **PSRR and CMRR vs Frequency**

- **2nd and 3rd Harmonic Distortion vs Frequency**

- **Transimpeance \( (R_{OL}) \) vs Frequency**

- **Voltage and Current Noise vs Frequency**

- **Closed-Loop Output Impedance vs Frequency**

- **Transimpeance \( (V_{OL}) \) vs Die Temperature**

- **Voltage and Current Noise vs Frequency**
  - \( b = 10 \,\text{pA/\sqrt{Hz}} \)
  - \( b = 5.1 \,\text{nV/\sqrt{Hz}} \)
  - \( b = 2.6 \,\text{pA/\sqrt{Hz}} \)

- **Voltage and Current Noise vs Frequency**
  - \( a = 3 \,\text{mV/\sqrt{Hz}} \)
  - \( a = 5 \,\text{mV/\sqrt{Hz}} \)

- **Voltage and Current Noise vs Frequency**
  - \( a = 7 \,\text{mV/\sqrt{Hz}} \)
Typical Performance Curves — Contd.

offset Voltage vs Die Temperature (4 Samples)

Supply Current vs Die Temperature (Per Amplifier)

Supply Current vs Supply Voltage (Per Amplifier)

+ Input Resistance vs Die Temperature

Input Current vs Die Temperature

+ Input Bias Current vs Input Voltage

Output Voltage Swing vs Die Temperature

Short Circuit Current vs Die Temperature

PSRR & CMRR vs Die Temperature

Input Voltage (V)

Supply Voltage (V)

Input Voltage (V)

PSRR (dB)

CMRR (dB)
Typical Performance Curves — Contd.

**Differential Gain vs DC Input Voltage, \( R_L = 150 \)**

- \( A_V = +2 \)
- \( R_F = 560 \)
- \( V_S = \pm 5V \)
- \( V_S = \pm 10V \)
- \( V_S = \pm 15V \)

**Differential Phase vs DC Input Voltage, \( R_L = 150 \)**

- \( A_V = +2 \)
- \( R_F = 560 \)
- \( V_S = \pm 5V \)
- \( V_S = \pm 10V \)
- \( V_S = \pm 15V \)

**Slew Rate vs Supply Voltage**

- \( V_S = \pm 5V \)
- \( V_S = \pm 10V \)
- \( V_S = \pm 15V \)

**Slew Rate vs Temperature**

- \( V_S = \pm 5V \)
- \( V_S = \pm 10V \)
- \( V_S = \pm 15V \)
Typical Performance Curves — Contd.

**Settling Time vs Settling Accuracy**

- **14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature**
- **14-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature**

**Long Term Settling Error**

- **8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature**
- **8-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature**

**Burn-In Circuits**

- **EL2260C**
- **EL2460C**
Differential Gain and Phase Test Circuit

Simplified Schematic (One Amplifier)
EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Applications Information

Product Description
The EL2260C/EL2460C are dual and quad current mode feedback amplifiers that offer wide bandwidths and good video specifications at moderately low supply currents. They are built using Elantec's proprietary complimentary bipolar process and are offered in industry standard pin-outs. Due to the current feedback architecture, the EL2260C/EL2460C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, $R_F$, and then the gain is set by picking the gain resistor, $R_G$. The curves at the beginning of the Typical Performance Curves section show the effect of varying both $R_F$ and $R_G$. The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below $\frac{1}{4''}$. The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO packages, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input
Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2260C/EL2460C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}$ emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2 pF of capacitance at the $V_{IN}$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values
The EL2260C and EL2460C have been designed and specified with $R_F = 560\,\Omega$ for $A_V = +2$. This value of feedback resistor yields extremely flat frequency response with little to no peaking out to 130 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing $R_F$ to 430Ω, bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of $R_F$ to 360Ω increases the bandwidth to 195 MHz with about 2.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature
Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2260C/EL2460C were designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 150 MHz to 110 MHz over the entire die junction temperature range of 0°C < $T$ < 150°C.
Applications Information — Contd.

Supply Voltage Range
The EL2260C/EL2460C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the 3 dB bandwidth at $A_V = +2$ is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2260C at ±2V supplies, $A_V = +2$, $R_F = R_G = 560\Omega$, driving a load of 150Ω, showing a clean ±600 mV signal at the output.

![Oscilloscope Plot](image)

If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2260C/EL2460C.

Settling Characteristics
The EL2260C/EL2460C offer superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2260/EL2460 are not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation
The EL2260C/EL2460C amplifiers combine both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2260C/EL2460C remain within their absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = N \cdot \left(2 \cdot V_S \cdot I_S + (V_S - V_{OUT}) \cdot \frac{V_{OUT}}{R_L}\right)$$

where $N$ is the number of amplifiers per package, and $I_S$ is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier’s AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, such as the LT1229 and LT1230, the EL2260C/EL2460C...
Applications Information — Contd.

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2260C/EL2460C have internal current limits that protect the circuit in the event of the output being shorted to ground. This limit is set at 100 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 65 mA. If any one output is shorted to ground, the power dissipation could be well over 1W, and much greater if all outputs are shorted. Heat removal is required in order for the EL2260C/EL2460C to survive an indefinite short.

Channel to Channel Isolation

Due to careful biasing connections within the internal circuitry of the EL2260C/EL2460C, exceptionally good channel to channel isolation is obtained. Isolation is over 70 dB at video frequencies of 4 MHz, and over 65 dB up to 10 MHz. The EL2460C isolation is improved an additional 10 dB, up to about 5 MHz, for amplifiers A to B and amplifiers C to D. Isolation is improved another 8 dB for amplifiers A to C and amplifiers B to D. See the curve in the Typical Performance Curves section for more detail.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2260C and EL2460C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, RG, can be chosen to make up for the gain loss created by this additional series resistor at the output.
EL2260C/EL2460C Macromodel

* Revision A, March 1993
* AC Characteristics used $C_{IN}$ (pin 2) = 1 pF; $R_F = 560\, \Omega$
* Connections:
  + input
  - input
  + $V_{supply}$
  - $V_{supply}$
  output

```
.subckt EL2260C/EL 3 2 7 4 6

* Input Stage
  e1 10 0 3 0 1.0
  vis 10 9 0V
  h2 9 12 vxx 1.0
  r1 2 11 130
  l1 11 12 25nH
  iinp 3 0 0.5\mu A
  iiim 2 0 5\mu A
  r12 3 0 2Meg

* Slew Rate Limiting
  h1 13 0 vis 600
  r2 13 14 1K
  d1 14 0 dclamp
  d2 0 14 dclamp

* High Frequency Pole
  *
  *e2 30 0 14 0 0.0016666666666
  l3 30 17 0.43\mu H
  c5 17 0 0.27\mu F
  r5 17 0 500

* Transimpedance Stage
  g1 0 18 17 0 1.0
  ro1 18 0 2Meg
  cdp 18 0 2.285\mu F

* Output Stage
  q1 4 18 19 qp
  q2 7 18 20 qn
  q3 7 19 21 qn
  q4 4 20 22 qp
  r7 21 6 4
  r8 22 6 4
  ios1 7 19 2mA
  ios2 20 4 2mA
```
EL2260C/EL2460C Macromodel — Contd.

* Supply Current
  * ips 7 4 2mA

* Error Terms
  *
  ivos 0 23 2mA
  vxxx 23 0 0V
  e4 24 0 3 0 1.0
  e5 25 0 7 0 1.0
  e6 26 0 4 0 1.0
  r9 24 23 562
  r10 25 23 1K
  r11 26 23 1K

* Models
  *
  .model qn nnn (is = 5e-15 bf = 100 tf = 0.1ns)
  .model qp pnp (is = 5e-15 bf = 100 tf = 0.1ns)
  .model dclamp d (is = 1e-30 ibv = 0.266 bv = 2.24 n = 4)
  .ends
Features
- Triple amplifier topology
- 130 MHz $-3$ dB bandwidth ($AV = +2$)
- 180 MHz $-3$ dB bandwidth ($AV = +1$)
- Wide supply range, $\pm 2V$ to $\pm 15V$
- 80 mA output current (peak)
- Low cost
- 1500 V/$\mu$s slew rate
- Input common mode range to within 1.5V of supplies
- 35 ns settling time to 0.1%
- Available in single (EL2160C), dual (EL2260C), and quad (EL2460C) form

Applications
- RGB amplifiers
- Video amplifiers
- Cable driver
- Test equipment amplifiers
- Current to voltage converters
- Video broadcast equipment

General Description
The EL2360C is a triple current-feedback operational amplifier which achieves a $-3$ dB bandwidth of 130 MHz at a gain of $+2$. Built using the Elantec proprietary monolithic complementary bipolar process, these amplifiers use current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback amplifier.

The EL2360C is designed to drive a double terminated 75Ω coax cable to video levels. It’s fast slew rate of 1500 V/$\mu$s, combined with the triple amplifier topology, makes it ideal for RGB video applications.

This amplifier can operate on any supply voltage from 4V ($\pm 2V$) to 33V ($\pm 16.5V$), yet consume only 8 mA per amplifier at any supply voltage. The EL2360C is available in 16-pin PDIP and SOIC packages.

For Single, Dual, or Quad applications, consider the EL2160C, EL2260C, or EL2460C all in industry standard pin outs. For Single applications with a power down feature, consider the EL2166C.

Connection Diagram

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2360CN</td>
<td>$-45^\circ$C to $+85^\circ$C 16-Pin PDIP MD-P031</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2360CS</td>
<td>$-45^\circ$C to $+85^\circ$C 16-Pin SOIC MD-P027</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between (V_{S+}) and (V_{S-})</td>
<td>(V_{S} = \pm 33V)</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>(V_{S-}) to (V_{S+})</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>(\mu V/\mu A)</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>(\pm 6V)</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>Current into +IN or -IN</td>
<td>(\pm 10 \mu A)</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>Internal Power Dissipation</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>(\mu A/\mu A)</td>
</tr>
<tr>
<td>Output Current (continuous)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
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<td>Operating Ambient Temperature Range</td>
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<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LT67 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25^\circ C) and QA sample tested at (T_A = 25^\circ C), (T_{MAX}) and (T_{MIN}) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25^\circ C) for information purposes only.</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics \(V_S = \pm 15V, R_L = 150\Omega, T_A = 25^\circ C\) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>2</td>
<td>10</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(TC_{VOS})</td>
<td>Average Input Offset Voltage Drift, (Note 1)</td>
<td></td>
<td>10</td>
<td></td>
<td>V</td>
<td>I</td>
<td>(\mu V/\mu A)</td>
</tr>
<tr>
<td>(+I_{IN})</td>
<td>+ Input Current</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>0.5</td>
<td>3</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(-I_{IN})</td>
<td>- Input Current</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>5</td>
<td>25</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(CMRR)</td>
<td>Common Mode Rejection Ratio, (Note 2)</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>50</td>
<td>55</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(-ICMR)</td>
<td>- Input Current Common Mode Rejection, (Note 2)</td>
<td>(V_S = \pm 5V, \pm 15V)</td>
<td>0.2</td>
<td>5</td>
<td></td>
<td>I</td>
<td>(\mu A/\mu A)</td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio, (Note 3)</td>
<td></td>
<td>75</td>
<td>95</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(-IPSRR)</td>
<td>- Input Current Power Supply Rejection, (Note 3)</td>
<td></td>
<td>0.2</td>
<td>5</td>
<td></td>
<td>I</td>
<td>(\mu A/\mu A)</td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Transimpedance, (Note 4)</td>
<td>(V_S = \pm 15V, R_L = 400\Omega)</td>
<td>500</td>
<td>2000</td>
<td>I</td>
<td>k\Omega</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 15V, R_L = 150\Omega)</td>
<td>500</td>
<td>1800</td>
<td>I</td>
<td>k\Omega</td>
<td></td>
</tr>
<tr>
<td>(+R_{IN})</td>
<td>+ Input Resistance</td>
<td></td>
<td>1.5</td>
<td>3</td>
<td></td>
<td>I</td>
<td>M\Omega</td>
</tr>
<tr>
<td>(+C_{IN})</td>
<td>+ Input Capacitance</td>
<td>PDIP package</td>
<td>1.5</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SOIC package</td>
<td>1</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>(CMIR)</td>
<td>Common Mode Input Range</td>
<td>(V_S = \pm 5V)</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 15V)</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 3.5)</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note 1:** Measured from \(T_{MIN}\) to \(T_{MAX}\).
**Note 2:** \(V_{CM} = \pm 10V\) for \(V_S = \pm 15V, V_{CM} = \pm 3V\) for \(V_S = \pm 5V\).
**Note 3:** The supplies are moved from \(\pm 2.5V\) to \(\pm 15V\).
**Note 4:** \(V_{OUT} = \pm 7V\) for \(V_S = \pm 15V, V_{OUT} = \pm 2V\) for \(V_S = \pm 5V\).
**DC Electrical Characteristics**  \( V_S = \pm 15V, R_L = 150\Omega, T_A = 25°C \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing</td>
<td>( V_S = \pm 15V, R_L = 400\Omega )</td>
<td>±12</td>
<td>±13.5</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 15V, R_L = 150\Omega )</td>
<td>±12</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, R_L = 150\Omega )</td>
<td>±3.0</td>
<td>±3.7</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Output Short Circuit Current, (Note 5)</td>
<td>( V_S = \pm 5V, \pm 15V )</td>
<td>60</td>
<td>100</td>
<td>150</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current (per amplifier)</td>
<td>( V_S = \pm 15V )</td>
<td>8.0</td>
<td>11.3</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>5.7</td>
<td>8.8</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

**AC Electrical Characteristics** (Note 8), \( V_S = \pm 15V, A_V = +2, R_F = R_Q = 560\Omega, R_L = 150\Omega, T_A = 25°C \) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( BW )</td>
<td>-3 dB Bandwidth</td>
<td>( V_S = \pm 15V, A_V = +2 )</td>
<td></td>
<td>130</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 15V, A_V = +1 )</td>
<td></td>
<td>180</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, A_V = +2 )</td>
<td></td>
<td>100</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V, A_V = +1 )</td>
<td></td>
<td>110</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>( SR )</td>
<td>Slew Rate (Note 6)</td>
<td>( R_L = 400\Omega )</td>
<td>1000</td>
<td>1500</td>
<td></td>
<td>IV</td>
<td>V/\mu s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_F = 1 \text{k}\Omega, R_Q = 110\Omega, R_L = 400\Omega )</td>
<td>1500</td>
<td></td>
<td></td>
<td>V</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>( t_r, t_f )</td>
<td>Rise Time, Fall Time</td>
<td>( V_{\text{OUT}} = \pm 500 \text{mV} )</td>
<td>2.7</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( \tau_{PD} )</td>
<td>Propagation Delay</td>
<td>( V_{\text{OUT}} = \pm 500 \text{mV} )</td>
<td>3.2</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( OS )</td>
<td>Overshoot</td>
<td>( V_{\text{OUT}} = \pm 500 \text{mV} )</td>
<td>0</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>( t_s )</td>
<td>0.1% Settling Time</td>
<td>( V_{\text{OUT}} = \pm 2.5V, A_V = -1 )</td>
<td>35</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( dG )</td>
<td>Differential Gain (Note 7)</td>
<td>( R_L = 150\Omega )</td>
<td>0.025</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 500\Omega )</td>
<td>0.006</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>( dP )</td>
<td>Differential Phase (Note 7)</td>
<td>( R_L = 150\Omega )</td>
<td>0.1</td>
<td></td>
<td></td>
<td>V</td>
<td>°</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 500\Omega )</td>
<td>0.005</td>
<td></td>
<td></td>
<td>V</td>
<td>°</td>
</tr>
</tbody>
</table>

Note 6: Slew Rate is with \( V_{\text{OUT}} \) from +10V to -10V and measured at +5V and -5V.

Note 7: DC offset from \(-0.714V\) to \(+0.714V\), AC amplitude 286 mVp-p, \( f = 3.58 \text{MHz} \).

Note 8: All AC tests are performed on a “warmed up” part, except Slew Rate, which is pulse tested.
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Frequency Response for Various $R_L$

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

Frequency Response for Various $R_F$ and $R_G$

3 dB Bandwidth vs Supply Voltage for $A_V = -1$

Peaking vs Supply Voltage for $A_V = -1$

3 dB Bandwidth vs Temperature for $A_V = -1$
Typical Performance Curves — Contd.

**3 dB Bandwidth vs Supply Voltage for AV = +1**

- $R_F = 560$
- $R_F = 430$
- $R_F = 750$

**Peaking vs Supply Voltage for AV = +1**

- $R_L = 150$
- $R_F = 360$
- $R_F = 560$

**3 dB Bandwidth vs Temperature for AV = +1**

- $V_S = \pm 15V$
- $V_S = \pm 10V$
- $V_S = \pm 2V$

**3 dB Bandwidth vs Supply Voltage for AV = +2**

- $R_F = 560$
- $R_F = 430$
- $R_F = 750$

**Peaking vs Supply Voltage for AV = +2**

- $R_L = 150$
- $R_F = 360$
- $R_F = 560$

**3 dB Bandwidth vs Temperature for AV = +2**

- $V_S = \pm 15V$
- $V_S = \pm 10V$
- $V_S = \pm 2V$

**3 dB Bandwidth vs Supply Voltage for AV = +10**

- $R_F = 560$
- $R_F = 430$
- $R_F = 750$

**Peaking vs Supply Voltage for AV = +10**

- $R_L = 150$
- $R_F = 360$
- $R_F = 560$

**3 dB Bandwidth vs Temperature for AV = +10**

- $V_S = \pm 15V$
- $V_S = \pm 10V$
- $V_S = \pm 2V$
Typical Performance Curves — Contd.

**Frequency Response for Various C<sub>L</sub>**

- C<sub>L</sub> = 80 pF
- C<sub>L</sub> = 47 pF
- C<sub>L</sub> = 20 pF
- C<sub>L</sub> = 0 pF

**Frequency Response for Various C<sub>IN</sub>**

- C<sub>IN</sub> = 3 pF
- C<sub>IN</sub> = 2 pF
- C<sub>IN</sub> = 1 pF
- C<sub>IN</sub> = 0 pF

**Channel to Channel Isolation vs Frequency**

**PSRR and CMRR vs Frequency**

**2nd and 3rd Harmonic Distortion vs Frequency**

**Transimpedance (R<sub>OL</sub>) vs Frequency**

**Voltage and Current Noise vs Frequency**

**Closed-Loop Output Impedance vs Frequency**

**Transimpedance (R<sub>OL</sub>) vs Die Temperature**
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)

Supply Current vs Die Temperature (Per Amplifier)

Supply Current vs Supply Voltage (Per Amplifier)

+ Input Resistance vs Die Temperature

Input Current vs Die Temperature

+ Input Bias Current vs Input Voltage

Output Voltage Swing vs Die Temperature

Short Circuit Current vs Die Temperature

PSRR & CMRR vs Die Temperature
**Typical Performance Curves — Contd.**

**Differential Gain vs DC Input Voltage, \( R_L = 150 \)**

![Differential Gain vs DC Input Voltage, \( R_L = 150 \)](image)

**Differential Phase vs DC Input Voltage, \( R_L = 180 \)**

![Differential Phase vs DC Input Voltage, \( R_L = 180 \)](image)

**Small Signal Pulse Response**

![Small Signal Pulse Response](image)

**Differential Gain vs DC Input Voltage, \( R_L = 500 \)**

![Differential Gain vs DC Input Voltage, \( R_L = 500 \)](image)

**Differential Phase vs DC Input Voltage, \( R_L = 500 \)**

![Differential Phase vs DC Input Voltage, \( R_L = 500 \)](image)

**Large Signal Pulse Response**

![Large Signal Pulse Response](image)

**Slew Rate vs Supply Voltage**

![Slew Rate vs Supply Voltage](image)

**Slew Rate vs Temperature**

![Slew Rate vs Temperature](image)
Typical Performance Curves — Contd.

**Settling Time vs Settling Accuracy**

- $\Delta V = \pm 10V$
- $R_L = 560$
- $V_S = \pm 15V$
- $A_V = +1$
- $A_V = -1$

**Long Term Settling Error**

- $\Delta V = \pm 10V$
- $R_L = 1k$
- $V_S = \pm 15V$
- $A_V = -1$
- $A_V = +1$

**16-Lead Plastic SO**
Maximum Power Dissipation vs Ambient Temperature

- $T_{j\text{max}} = 150°C$
- $\theta_{JA} = 115°/W$
- $\theta_{JC} = 40°/W$

**18-Lead Plastic DIP**
Maximum Power Dissipation vs Ambient Temperature

- $T_{j\text{max}} = 150°C$
- $\theta_{JA} = 74°/W$
- $\theta_{JC} = 40°/W$

Free Air
No Heat Sink
Differential Gain And Phase Test Circuit

Simplified Schematic (One Amplifier)
Applications Information

Product Description
The EL2360C is a triple current feedback amplifier that offers wide bandwidth and good video specifications at moderately low supply currents. It is built using Elantec's proprietary complimentary bipolar process and is offered in both a 16 pin PDIP and SOIC packages. Due to the current feedback architecture, the EL2360C closed-loop -3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, $R_F$, and then the gain is set by picking a gain resistor, $R_G$. The curves at the beginning of the Typical Performance Curves section show the effect of varying both $R_F$ and $R_G$. The -3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in the closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, preferably below $\frac{1}{4}''$. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input
Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. The characteristic curve of gain vs. frequency with variations in $C_{IN}$ emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2pF of capacitance at the $V_{IN-}$ pin. For inverting gains, this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains, this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

Feedback Resistor Values
The EL2360C has been designed and specified at a gain of $+2$ with $R_F = 560\Omega$. This value of feedback resistor yields relatively flat frequency response with little to no peaking out to 130 MHz. Since the EL2360C is a current-feedback amplifier, it is also possible to change the value of $R_F$ to get more bandwidth. As seen in the curve of Frequency Response For Various $R_F$ and $R_G$, bandwidth and peaking can be easily modified by varying the value of the feedback resistor. For example, by reducing $R_F$ to 430Ω, bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of $R_F$ to 360Ω increases the bandwidth to 195 MHz with about 2.5 dB of peaking.

Bandwidth vs Temperature
Whereas many amplifier's supply current and consequently -3 dB bandwidth drop off at high temperature, the EL2360C was designed to have little supply current variation with temperature. An immediate benefit from this is that the -3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth varies only from 150 MHz to 110 MHz over the entire die junction temperature range of $-50^\circ C < T < 150^\circ C$. 


Applications Information — Contd.

Supply Voltage Range and Single Supply Operation
The EL2360C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the −3 dB bandwidth at AV = +2 is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2360C at ±2V supplies, AV = +2, RF = RG = 560Ω, driving a load of 150Ω, showing a clean ±600 mV signal at the output.

![Oscilloscope Plot](image)

If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2360C, which is typically 1.5V from each supply rail.

Settling Characteristics
The EL2360C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2360C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for AV = +1, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For AV = −1, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With AV = −1, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation
The EL2360C amplifier combines both high speed and large output current capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2360C remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined according to [1]:

$$ PD_{\text{MAX}} = \frac{T_{\text{JMAX}} - T_{\text{AMAX}}}{\theta_{JA}} $$  [1]

where:

- $T_{\text{JMAX}}$ = Maximum Junction Temperature
- $T_{\text{AMAX}}$ = Maximum Ambient Temperature
- $\theta_{JA}$ = Thermal Resistance of the Package
- $PD_{\text{MAX}}$ = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$ PD_{\text{MAX}} = N(V_S * I_{\text{SMAX}} + (V_S - V_{\text{OUT}}) \frac{V_{\text{OUT}}}{R_L}) $$  [2]

where:

- $N$ = Number of amplifiers
- $V_S$ = Total Supply Voltage
- $I_{\text{SMAX}}$ = Maximum Supply Current per amplifier
- $V_{\text{OUT}}$ = Maximum Output Voltage of the Application
- $R_L$ = Load Resistance tied to Ground
Applications Information — Contd.

If we set the two PD\textsubscript{MAX} equations, [1] and [2], equal to each other, and solve for \( V_S \), we can get a family of curves for various loads and output voltages according to [3]:

\[
V_S = \frac{R_L(T_{J\text{MAX}} - T_{A\text{MAX}})}{N \cdot \theta_J} + \left(\frac{V_{\text{OUT}}}{I_S \cdot R_L}\right)^2 + V_{\text{OUT}}
\]

The figures below show total supply voltage \( V_S \) vs \( R_L \) for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of \( T_A = +85^\circ\text{C} \) and \( I_S = 11.3 \text{ mA per amplifier} \). The curves do not include heat removal or forcing air, or the simple fact that the package will be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2360C has internal current limits that protect the circuit in the event of an output being shorted to ground. This limit is set at 100 mA nominally and reduces with the junction temperature. At \( T_J = 150^\circ\text{C} \), the current limits at about 65 mA. If any one output is shorted to ground, the power dissipation could be well over 1W, and much greater if all outputs are shorted. Heat removal is required in order for the EL2360C to survive an indefinite short.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2360C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5\( \Omega \) and 50\( \Omega \)) can be placed in series with the output to eliminate most peaking. The gain resistor (\( R_G \)) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (\( R_F \)) to reduce the peaking.
EL2360C Macromodel

* EL2360C Macromodel
* Revision A, June 1996
* AC characteristics used: $R_f = R_g = 560$ ohms
* Pin numbers reflect a standard single opamp
* Connections: + input
* -input + $V_{supply}$ - $V_{supply}$ output
* .subckt EL2360/EL 3 2 7 4 6
* * Input Stage
* e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5μA
iimm 2 0 5μA
r12 3 0 2 Meg
* * Slew Rate Limiting
* h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
* * High Frequency Pole
* e2 30 0 14 0 0.0016666666666
l3 30 17 0.43μH
c5 17 0 0.27pF
r5 17 0 500
* * Transimpedance Stage
* g1 0 18 17 0 1.0
cdp 18 0 2.285pF
* * Output Stage
* c1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
* * Supply Current
* ips 7 4 2.5mA
* * Error Terms
* ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 0 -1.0
rl 9 24 23 562
r10 25 23 1K
r11 26 23 1K
* * Models
* .model qn npn(is = 5e-15 bf = 100 tf = 0.1 ns)
.model qn npn(is = 5e-15 bf = 100 tf = 0.1 ns)
.model dclamp d(is = 1e-30 ibv = 0.266
+ bv = 2.24v n = 4)
.ends
EL2360C Macromodel — Contd.
Features

- 35 MΩ transimpedance
- 30 MHz −3dB bandwidth (AV = +1)
- 30 MHz −3dB bandwidth (AV = +2)
- 1 mV input offset voltage
- 2 μA negative input bias current
- 86 dB common mode rejection ratio
- 92 dB power supply rejection ratio
- Low supply current, 4 mA
- Wide supply range, ±4.5V to ±16.5V
- 55 mA output peak current
- High capacitive load tolerance
- Low cost
- Input/output compliance to ±2V of supplies
- 500 V/μs slew rate
- 65 ns settling to 0.1%
- 110 ns settling to 0.01%
- −68 dBc distortion @ 1 MHz

Applications

- Instrumentation circuitry
- Current to voltage convertors
- DAC/ADC output amplifier/ buffer
- Cable drivers
- Low distortion communications
- Medical imaging
- CCD imaging
- Infrared image enhancement

General Description

The EL2165C is a low offset, high transimpedance current mode feedback amplifier with a −3 dB bandwidth of 30 MHz at a gain of +2. Built on Elantec’s proprietary monolithic complementary bipolar process, this amplifier uses current feedback to achieve more bandwidth at a given gain than conventional voltage feedback amplifiers.

The high 35 MΩ transimpedance gain and low input referred offset of the EL2165 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

In addition, the common-mode and power supply rejection have been greatly improved over earlier current mode feedback amplifiers and the input offset voltage and current have been trimmed to rival that of good conventional voltage feedback amplifiers. The part has a typical slew rate of 500 V/μs and a 0.01% settling time of less than 110ns in inverting mode. At a gain of +2 and an output signal level of 2 Vp-p, the total harmonic distortion is only −68 dB at 1 MHz.

The amplifier can operate on any supply from 9V (±4.5V) to 33V (±16.5V), yet consumes only 4 mA at any supply voltage. Using the industry standard 8-pin pinout, the EL2165C is available in both P-DIP and SO packages.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2165CN</td>
<td>−40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2165CS</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Manufactured under U.S. Patent No. 5,418,495, 5,420,542, 5,479,133
Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between ( V_+ ) and ( V_- )</td>
<td></td>
<td></td>
<td>+33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage between ( I_+ ) and ( I_- )</td>
<td></td>
<td></td>
<td>±6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current into ( I_+ ) and ( I_- )</td>
<td></td>
<td></td>
<td>4 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

Open Loop DC Electrical Characteristics
\( (V_S = \pm 15V, R_L = 500\Omega, T_A = 25^\circ C \) unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>( 25^\circ C )</td>
<td>1</td>
<td>3</td>
<td>I</td>
<td>mV</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>TC ( V_{OS} )</td>
<td>Average Offset Voltage Drift (Note 1)</td>
<td>Full</td>
<td>2</td>
<td>V</td>
<td>( \mu V/\circ C )</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IN}^+ )</td>
<td>+ Input Current</td>
<td>( 25^\circ C )</td>
<td>-1</td>
<td>( \pm 6 )</td>
<td>I</td>
<td>( \mu A )</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( I_{IN}^- )</td>
<td>- Input Current</td>
<td>( 25^\circ C )</td>
<td>( \pm 2 )</td>
<td>( \pm 7 )</td>
<td>I</td>
<td>( \mu A )</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( CMRR )</td>
<td>Common Mode Rejection Ratio (Note 2)</td>
<td>( 25^\circ C )</td>
<td>79</td>
<td>86</td>
<td>I</td>
<td>dB</td>
<td>I</td>
<td>nA/V</td>
</tr>
<tr>
<td>( ICMR^- )</td>
<td>- Input Current Common Mode Rejection (Note 2)</td>
<td>( 25^\circ C )</td>
<td>23</td>
<td>100</td>
<td>I</td>
<td>nA/V</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( PSRR )</td>
<td>Power Supply Rejection Ratio (Note 3)</td>
<td>( 25^\circ C )</td>
<td>84</td>
<td>93</td>
<td>I</td>
<td>dB</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( IPSR^- )</td>
<td>- Input Current Power Supply Rejection (Note 3)</td>
<td>( 25^\circ C )</td>
<td>75</td>
<td>225</td>
<td>I</td>
<td>nA/V</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( R_{OL} )</td>
<td>Transimpedance (Note 4)</td>
<td>( V_S = \pm 15V )</td>
<td>25^\circ C</td>
<td>35</td>
<td>V</td>
<td>M\Omega</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 500\Omega )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>25^\circ C</td>
<td>5.0</td>
<td>12.4</td>
<td>I</td>
<td>M\Omega</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 150\Omega )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{IN}^+ )</td>
<td>+ Input Resistance</td>
<td>( 25^\circ C )</td>
<td>18</td>
<td>36</td>
<td>I</td>
<td>M\Omega</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( C_{IN}^+ )</td>
<td>+ Input Capacitance</td>
<td>( 25^\circ C )</td>
<td>2.5</td>
<td>V</td>
<td></td>
<td>pF</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( CMIR )</td>
<td>Common Mode Input Range (Note 2)</td>
<td>( V_S = \pm 15V )</td>
<td>25^\circ C</td>
<td>( \pm 12 )</td>
<td>( \pm 12.5 )</td>
<td>I</td>
<td>V</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = \pm 5V )</td>
<td>25^\circ C</td>
<td>( \pm 2.0 )</td>
<td>( \pm 2.5 )</td>
<td>I</td>
<td>V</td>
<td>I</td>
</tr>
</tbody>
</table>
### Open Loop DC Electrical Characteristics

*(V<sub>S</sub> = ±15V, R<sub>L</sub> = 500Ω, T<sub>A</sub> = 25°C unless otherwise specified) — Contd.*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
</table>
| VO        | Output Voltage Swing              | R<sub>L</sub> = 500Ω  
V<sub>S</sub> = ±15V | 25°C  | ±12.3 | ±13  |      | I    | V         |
|           |                                   | R<sub>L</sub> = 150Ω  
V<sub>S</sub> = ±15V | 25°C  | ±11.6 |      |      | V    | V         |
|           |                                   | R<sub>L</sub> = 150Ω  
V<sub>S</sub> = ±5V  | 25°C  | ±2.7  | ±3.0 |      | I    | V         |
| ISC       | Output Short Circuit Current      |             | 25°C  | 55   | 80   |      | I         | mA    |
| ISC       | *(Note 4 and 5)*                  |             | 25°C  | 55   | 80   |      | I         | mA    |
| IS        | Supply Current                    |             | 25°C  | 4.0  | 5.25 |      | I         | mA    |
## Closed Loop AC Electrical Characteristics

\(V_S = \pm 15V, \; A_V = +2, \; R_F = 1K\Omega, \; R_L = 500\Omega, \; T_A = 25^\circ C\) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>(-3dB) (Note 8)</td>
<td>(V_S = \pm 15V, A_V = +2, ; R_F = 1K\Omega)</td>
<td>30</td>
<td>25</td>
<td>50</td>
<td>V</td>
<td>V/MHz</td>
</tr>
<tr>
<td></td>
<td>(V_S = \pm 15V, A_V = +1, ; R_F = 1.3K)</td>
<td></td>
<td>28</td>
<td>25</td>
<td>50</td>
<td>V</td>
<td>V/MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (Notes 6 and 8)</td>
<td>(R_L = 500\Omega)</td>
<td>250</td>
<td>100</td>
<td>500</td>
<td>I</td>
<td>V/ \mu S</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(R_F = 1K\Omega, ; R_O = 110\Omega, R_L = 400\Omega)</td>
<td>500</td>
<td>100</td>
<td>500</td>
<td>V</td>
<td>V/ \mu S</td>
</tr>
<tr>
<td>(t_r, t_f)</td>
<td>Rise Time, Fall Time (Note 8)</td>
<td>(V_{OUT} = \pm 500; mV)</td>
<td>14</td>
<td>10</td>
<td>20</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td>(t_{pd})</td>
<td>Propagation Delay (Note 8)</td>
<td></td>
<td>12</td>
<td>10</td>
<td>20</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td>(O_S)</td>
<td>Overshoot (Note 8)</td>
<td>(V_{OUT} = \pm 500; mV)</td>
<td>2</td>
<td>1</td>
<td>10</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>(t_s)</td>
<td>0.1% Settling Time (Note 8)</td>
<td>(V_{OUT} = \pm 10V)</td>
<td>120</td>
<td>65</td>
<td>100</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(A_V = 1)</td>
<td>65</td>
<td>35</td>
<td>100</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(A_V = -1)</td>
<td>100</td>
<td>50</td>
<td>200</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(A_V = 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_s)</td>
<td>0.01% Settling Time (Note 8)</td>
<td>(V_{OUT} = \pm 10V)</td>
<td>750</td>
<td>375</td>
<td>1000</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(A_V = 1)</td>
<td>375</td>
<td>187</td>
<td>500</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(A_V = -1)</td>
<td>1000</td>
<td>500</td>
<td>1000</td>
<td>V</td>
<td>nS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(A_V = 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Measured from \(T_{MIN}\) to \(T_{MAX}\).

Note 2: \(V_{CM} = \pm 12V\) for \(V_S = \pm 15V\) and \(T_A = 25^\circ C\).
\(V_{CM} = \pm 2V\) for \(V_S = \pm 5V\) and \(T_A = 25^\circ C\).

CMIR is guaranteed by the part passing CMRR at the rated common-mode swing.

Note 3: The supplies are moved from \(\pm 4.5V\) to \(\pm 15V\).

Note 4: \(V_{OUT} = \pm 10V\) for \(V_S = \pm 15V\), and \(V_{OUT} = \pm 2V\) for \(V_S = \pm 5V\).

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 6: Slew Rate is with \(V_{OUT}\) from \(+10V\) to \(-10V\) and measured at the 25\% and 75\% points.

Note 7: DC offset from \(-0.714V\) through \(+0.714V\), AC amplitude 286 mV_{pp}, \(f = 3.58\; MHz\).

Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
Typical Performance Curves

Frequency Response for $A_V = -1$ and for Various $R_F$ Values

Frequency Response for $A_V = +1$ and for Various $R_F$ Values

Frequency Response for $A_V = +2$ and for Various $R_F$ Values

Frequency Response for $A_V = +10$ and for Various $R_L$ Values

Frequency Response for Various Values of $C_L$

Frequency Response for Various Values of $R_L$

3 dB Bandwidth vs Supply Voltage for $A_V = -1$

Peaking vs Supply Voltage for $A_V = -1$

3 dB Bandwidth vs Temperature for $A_V = -1$
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_v = +1$

3 dB Bandwidth vs Supply Voltage for $A_v = +2$

3 dB Bandwidth vs Supply Voltage for $A_v = +10$

Peaking vs Supply Voltage for $A_v = +1$

Peaking vs Supply Voltage for $A_v = +2$

Peaking vs Supply Voltage for $A_v = +10$

3 dB Bandwidth vs Temperature for $A_v = +1$

3 dB Bandwidth vs Temperature for $A_v = +2$

3 dB Bandwidth vs Temperature for $A_v = +10$
Typical Performance Curves — Contd.

- Frequency Response for Various Values of $C_{IN}$

- PSRR and CMRR vs Frequency

- Voltage and Current Noise vs Frequency

- Transimpedance ($R_{OL}$) vs Frequency

- Closed-Loop Output Impedance vs Frequency

- Slew Rate vs Supply Voltage

- Slew Rate vs Temperature
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)

Supply Current vs Die Temperature

Supply Current vs Supply Voltage

Input Resistance vs Die Temperature

Input Current vs Die Temperature

Output Voltage Swing vs Die Temperature

PSRR and CMRR vs Die Temperature
Typical Performance Curves — Contd.

Small Signal Pulse Response

Typical Performance Curves — Contd.

Large Signal Pulse Response

Settling Time vs Settling Accuracy

8-Pin Package
Power Dissipation vs Ambient Temperature

Long Term Settling Error

\[ \Delta V = \pm 10V \]
\[ R_c = 1k \]
\[ R_L = 1k \]
\[ V_S = \pm 15V \]

\[ A_V = -1 \]
\[ A_V = +1 \]

\[ 8\text{-PIN DIP} \]

\[ 8\text{-PIN SO} \]

\[ 170^\circ C/\text{W} \]

\[ 100^\circ C/\text{W} \]

\[ 0.04 \]

\[ 0.03 \]

\[ 0.02 \]

\[ 0.01 \]

\[ 0.00 \]

\[ 0.04 \]

\[ 0.03 \]

\[ 0.02 \]

\[ 0.01 \]

\[ 0.00 \]
Applications Information

Product Description
The EL2165C is a single current mode feedback amplifier that offers wide bandwidth, high gain, low distortion and exceptional DC specifications for a CMF type amplifier at moderate supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in the industry standard pin-out. Due to the current feedback architecture, the EL2165 closed loop 3 dB bandwidth is dependent on the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, RF, and then the gain is set by picking the gain set resistor, RG. The curves at the beginning of the Typical Performance Curves section show the effect of varying both RF and RG. The 3 dB bandwidth is significantly less dependent on supply voltage than earlier CMF amplifiers where increasing junction capacitances with decreasing supply voltage caused a much larger reduction in bandwidth. To compensate for the remaining effect, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to ensure stability. A 1.0 µF tantalum capacitor in parallel with a 0.01 µF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should have low inductance for best performance. Use of sockets, particularly for SO packages, should be avoided. Sockets have parasitic inductance and capacitance which will cause peaking and overshoot.

Capacitance at the Inverting Input
Due to the topology of the conventional current feedback amplifiers, stray capacitance at the inverting input will affect their AC and transient performance when operating in the non-inverting configuration. This may cause design, development and production difficulties. The EL2165 has been designed in such a way as to largely ignore such strays. The characteristic curves of gain vs. frequency with varying values of Cin illustrate this effect which produces only a slight increase in peaking with Cin values up to 5 pF with almost no change in 3 dB bandwidth.

In the inverting gain mode, added capacitance at the inverting input has almost no effect at all. This is because the inverting input is now a virtual ground and the stray capacitance is not therefore “seen” by the amplifier.

Feedback Resistors Values
The EL2165 has been designed and specified with \( RF = 1 \, \text{KΩ} \) for \( AV = +2 \). This value of feedback resistor yields an extremely flat frequency response with little or no peaking out to 30 MHz. As is the case with all CMF amplifiers, wider bandwidth, at the expense of peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at lower frequency. For example, the 3 dB bandwidth of the EL2165 connected for \( AV = -1 \) and \( RF = 1 \, \text{KΩ} \) is about 34 MHz. If \( RF \) is reduced to 750n \( the bandwidth increases to 48 MHz. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors, supply voltages and temperature.

Bandwidth vs. Temperature
The supply current of many amplifiers, and consequently their 3 dB bandwidths, drop off significantly with increasing temperature. The EL2165 was designed to have nearly constant supply current over temperature resulting in a part with much less bandwidth vs. temperature sensitivity. With \( VS = \pm 15V \) and \( AV = +2 \), the bandwidth only varies from 38 MHz to 29 MHz over the entire die temperature range of 0°C < T < 150°C.
Applications Information — Contd.

Supply Voltage Range
The EL2165 has been designed to operate comfortably with supply voltages from \( \pm 5 \text{V} \) to \( \pm 15 \text{V} \). AC characterization has been conducted down to supply voltages of \( \pm 3.5 \text{V} \). However, this low value will not allow the part to power up and function properly at the lowest portion of the part's operating temperature range (-40°C to +85°C). In general, bandwidth, slew rate and video characteristics will tend to improve with increasing supply voltages.

If a single supply is desired, values from +9V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and DC couple the signal, or 2) ensure the driving a signal is within the input common mode range of the EL2165.

Settling Characteristics
The EL2165 offers superb settling characteristics to 0.1\%, typically 65 ns operating in inverting mode. The inverting 0.01\% settling time is about 110 ns. The EL2165 is not slew rate limited, therefore a step size up to \( \pm 10 \text{V} \) gives the same settling time. The high 35 MΩ transimpedance gain and low input referred offsets of the EL2165 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

The noninverting (\( A_V = +1 \)) 0.1\% settling time is about 120 ns. As can be seen from the Long Term Settling Error graph, for \( A_V = +1 \), there is approximately a 0.04\% residual which tails away to 0.01\% in about 750 ns. This is a thermal settling error caused by a power dissipation change in the input stage devices (before and after the voltage step). All others CMF amplifier exhibit 0.01\% thermal settling tails of several tens of microseconds under the same conditions. The input stage of the EL2165 has been designed to greatly reduce this effect. For \( A_V = -1 \), the inverting input is a virtual ground, therefore this tail does not appear even in conventional CMF amplifiers since the input stage does not experience the large voltage change that it does in noninverting mode.

Distortion Performance
The distortion performance of all high frequency amplifiers degrade with increasing frequency. The EL2165 is no exception. However, due to the part's high transimpedance, its distortion performance at a given frequency can be 4 dB–8 dB better than other high speed amplifiers available, with the same power dissipation.

Power Dissipation
The EL2165 amplifier combines both high speed and large output drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature and loading conditions. To ensure that the EL2165 remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by it's thermal resistance and the amount of temperature rise according to:

\[
P_{\text{Dmax}} = \frac{(T_{J,\text{MAX}} - T_{A,\text{MAX}})}{\theta_{JA}}
\]

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power dissipated in the IC due to the load, or:

\[
P_{\text{Dmax}} = N \times (2 \times V_S \times I_S + (V_S - V_{\text{OUT}}) \times V_{\text{OUT}} / R_L)
\]

where \( N \) is the number of amplifiers per package, and \( I_S \) is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term when the output is driving a load. That is to say, due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher temperatures and lower supply current. Unlike some amplifiers, the EL2165 and many other Elantec amplifiers maintain almost constant supply current over temperature so that
Applications Information — Contd.

The AC performance is not degraded as much at the upper end of the operating temperature range.

The EL2165 consumes typically 4 mA and a maximum of 5 mA. The worst case power dissipated in an IC amplifier operating from split supplies with a grounded load occurs when the output is between ground and half of one of its supplies or, if it can't go that far due to drive limitations, at its maximum value. If we assume that the EL2165 is used for double terminated cable driving application (RL = 150Ω), and AV = +2, then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two PD_max equations equal to each other, and solve for VS, we get a family of curves for various packages options according to:

$$V_S = \frac{RL \times (TJ_{MAX} - T_{MAX})}{N \times \theta JA} + (V_{OUT}) \times (V_{OUT})$$

$$+ \frac{(2 \times I_S \times RL)}{(V_{OUT})}$$

The following curve shows supply voltage (±VS) vs. temperature for the EL2165's two packages assuming AV = +2, RL = 150, and V_{OUT} (peak) = 2V. The curves include the worst case supply specification (IS = 5 mA).

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the device.

Output Current Drive

The EL2165 does not have output short circuit protection. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2165 to survive an indefinite short.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For these applications, the back termination series resistor will decouple the EL2165 from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. The EL2165 has particularly high capacitive load toleration and can drive a 50 pF load with only 0.3 dB of peaking and a 100 pF load with only 0.5 dB of peaking and without any instability. If higher capacitive loads must be driven or if little or no peaking is required, an additional small value (50–500) resistor can be placed in series with the output. The gain resistor, RG, can be chosen to make up for the gain loss created by this additional series resistance at the output.
Features

- 110 MHz 3 dB bandwidth \((AV = +2)\)
- 115 MHz 3 dB bandwidth \((AV = +1)\)
- 0.01% differential gain, \(RL = 500\Omega\)
- 0.01° differential phase, \(RL = 500\Omega\)
- Low supply current, 7.5 mA
- Fast disable < 75 ns
- Low cost
- 1500 V/µs slew rate

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters
- Broadcast equipment
- High speed communications
- Video multiplexing

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline#</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2166CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2166CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

General Description

The EL2166C is a current feedback operational amplifier with \(-3\) dB bandwidth of 110 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

The EL2166C is designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω \((<0.01%/<0.01°)\) and double terminated 75Ω cables \((0.025%/0.05° @ VS = \pm 15V, 0.04%/0.02° @ VS = \pm 5V)\).

The EL2166C has a superior output disable function. Time to enable or disable is < 75 ns. The DISABLE pin is TTL/CMOS compatible. In disable mode, the amplifier can withstand over 1500 V/µs signals at their outputs. The amplifier can operate on any supply voltage from 10V \((\pm 5V)\) to 33V \((\pm 16.5V)\), yet consume only 7.5 mA at any supply voltage. The EL2166C is available in 8-pin P-DIP and 8-pin SO packages.

Connection Diagram

```
EL2166C SO, P-DIP Packages

GND IN+ IN- DISABLE Vs+

out NC

Top View

2166-1
```

Manufactured under U.S. Patent No. 5,420,542, 4,893,091
Absolute Maximum Ratings ($T_A = 25^\circ C$)

- Voltage between $V_{S+}$ and $V_{S-}$: $+33V$
- Voltage between $+IN$ and $-IN$: $\pm 6V$
- Current into $+IN$ or $-IN$: $10mA$
- Output Current: $\pm 50mA$
- Current into $DISABLE$ Pin: $\pm 5mA$
- Voltage between $DISABLE$ Pin and GND Pin: $\pm 7V$

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level | Test Procedure
---|---
I | 100% production tested and QA sample tested per QA test plan QCX0002.
II | $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.
III | $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.
IV | QA sample tested per QA test plan QCX0002.
V | Parameter is guaranted (but not tested) by Design and Characterization Data.

Open Loop DC Electrical Characteristics

$V_S = \pm 15V, R_L = 150\Omega, T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$VOS$</td>
<td>Input Offset Voltage</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>2</td>
<td>10</td>
<td>I</td>
</tr>
<tr>
<td>$TC_VOS$</td>
<td>Average Offset Voltage Drift (Note 1)</td>
<td>Full</td>
<td>$25^\circ C$</td>
<td>10</td>
<td>V</td>
<td>$\mu V/^\circ C$</td>
</tr>
<tr>
<td>$+ I_{IN}$</td>
<td>+ Input Current</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>0.5</td>
<td>5</td>
<td>I</td>
</tr>
<tr>
<td>$- I_{IN}$</td>
<td>- Input Current</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>5</td>
<td>20</td>
<td>I</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio (Note 2)</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>55</td>
<td>62</td>
<td>II</td>
</tr>
<tr>
<td>$- ICMR$</td>
<td>- Input Current Common Mode Rejection (Note 2)</td>
<td>$V_S = \pm 5V, \pm 15V$</td>
<td>$25^\circ C$</td>
<td>0.1</td>
<td>2</td>
<td>I</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Note 3)</td>
<td></td>
<td>$25^\circ C$</td>
<td>65</td>
<td>72</td>
<td>II</td>
</tr>
<tr>
<td>$- IPSR$</td>
<td>- Input Current Power Supply Rejection (Note 3)</td>
<td></td>
<td>$25^\circ C$</td>
<td>0.1</td>
<td>2</td>
<td>I</td>
</tr>
</tbody>
</table>
### Open Loop DC Electrical Characteristics — Contd.

*V_s = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_{OL}$ Transimpedance (Note 4)</td>
<td>$V_s = ±15V$</td>
<td>25°C</td>
<td>500 2000</td>
<td>1</td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 400Ω$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = ±5V$</td>
<td>25°C</td>
<td>500 1200</td>
<td>1</td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 150Ω$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$+R_{IN}$</td>
<td>$+\text{Input Resistance}$</td>
<td>$V_s = ±15V$</td>
<td>25°C</td>
<td>2.0 5.0</td>
<td>1</td>
<td>MΩ</td>
</tr>
<tr>
<td>$+C_{IN}$</td>
<td>$+\text{Input Capacitance}$</td>
<td>$V_s = ±15V$</td>
<td>25°C</td>
<td>2.5</td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td>CMIR</td>
<td>Common Mode Input Range</td>
<td>$V_s = ±15V$</td>
<td>25°C</td>
<td>±12.6 ±13.2</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = ±5V$</td>
<td>25°C</td>
<td>±2.6 ±3.2</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing</td>
<td>$R_L = 400Ω, V_s = ±15V$</td>
<td>25°C</td>
<td>±12 ±13.5</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 150Ω, V_s = ±15V$</td>
<td>25°C</td>
<td>±11.4</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 150Ω, V_s = ±5V$</td>
<td>25°C</td>
<td>±3.0 ±3.7</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Output Short Circuit Current (Note 5)</td>
<td>$V_s = ±5V, V_s = ±15V$</td>
<td>25°C</td>
<td>50 80 130</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$V_s = ±15V, V_s = ±5V$</td>
<td>25°C</td>
<td>7.5 10.0</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{S, OFF}$</td>
<td>Supply Current Disabled, Pin 8 = 0V</td>
<td></td>
<td>25°C</td>
<td>7.3 10.0</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OUT, OFF}$</td>
<td>Output Current Disabled, Pin 8 = 0V</td>
<td>$A_V = +1$</td>
<td>25°C</td>
<td>2.0 50.0</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>DISABLE Pin Voltage for Output Enabled (Note 9)</td>
<td>$A_V = +1$</td>
<td>25°C</td>
<td>0.8</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>DISABLE Pin Threshold for Output Disabled</td>
<td></td>
<td>25°C</td>
<td>0.8</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DIS, ON}$</td>
<td>DISABLE Pin Input Current, Pin 8 = +5V</td>
<td></td>
<td>25°C</td>
<td>70 150</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{DIS, OFF}$</td>
<td>DISABLE Pin Input Current, Pin 8 = 0V</td>
<td></td>
<td>25°C</td>
<td>−150 −60</td>
<td>1</td>
<td>µA</td>
</tr>
</tbody>
</table>
### Closed Loop AC Electrical Characteristics

$V_S = \pm 15V, A_V = \pm 2, R_F = 560\Omega, R_L = 150\Omega, T_A = 25^\circ C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>-3 dB Bandwidth (Note 8)</td>
<td>$V_S = \pm 15V, A_V = +2$</td>
<td>110</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V, A_V = +1$</td>
<td>115</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V, A_V = +2$</td>
<td>95</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 5V, A_V = +1$</td>
<td>100</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (Notes 6, 8)</td>
<td>$R_L = 400\Omega$</td>
<td>1000</td>
<td>1500</td>
<td>IV</td>
</tr>
<tr>
<td>t_r, t_f</td>
<td>Rise Time, Fall Time, (Note 8)</td>
<td>$V_{OUT} = \pm 500mV$</td>
<td>3.2</td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>t pd</td>
<td>Propagation Delay (Note 8)</td>
<td>$V_{OUT} = \pm 500 mV$</td>
<td>4.3</td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot (Note 8)</td>
<td>$V_{OUT} = \pm 500mV$</td>
<td>7</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>t_s</td>
<td>0.1% Settling Time (Note 8)</td>
<td>$V_{OUT} = \pm 10V$</td>
<td>35</td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain (Notes 7, 8)</td>
<td>$R_L = 150\Omega, V_S = \pm 15V$</td>
<td>0.025</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 150\Omega, V_S = \pm 5V$</td>
<td>0.05</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 500\Omega, V_S = \pm 15V$</td>
<td>0.01</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 500\Omega, V_S = 5V$</td>
<td>0.01</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase (Notes 7, 8)</td>
<td>$R_L = 150\Omega, V_S = \pm 15V$</td>
<td>0.04</td>
<td>V</td>
<td>deg (*)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 150\Omega, V_S = \pm 5V$</td>
<td>0.02</td>
<td>V</td>
<td>deg (*)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 500\Omega, V_S = \pm 15V$</td>
<td>0.01</td>
<td>V</td>
<td>deg (*)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 500\Omega, V_S = 5V$</td>
<td>0.01</td>
<td>V</td>
<td>deg (*)</td>
</tr>
<tr>
<td>tDIS</td>
<td>Disable/Enable Time (Note 10)</td>
<td>$V_{OUT} = \pm 7V$</td>
<td>75</td>
<td>V</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 1:** Measured from $T_{MIN}$ to $T_{MAX}$.
**Note 2:** $V_{CM} = \pm 12.6V$ for $V_S = \pm 15V$ and $T_A = 25^\circ C$.
**Note 3:** $V_{CM} = \pm 2.6V$ for $V_S = \pm 5V$ and $T_A = 25^\circ C$.
**Note 4:** The supplies are moved from $\pm 5V$ to $\pm 15V$.
**Note 5:** $V_OUT = \pm 7V$ for $V_S = \pm 15V$, and $V_OUT = \pm 2V$ for $V_S = \pm 5V$.
**Note 6:** A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
**Note 7:** DC offset from $-0.714V$ through $+0.714V$, AC amplitude 286 mVp-p, $f = 3.58 MHz$.
**Note 8:** All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
**Note 9:** The EL2166C will remain ENABLED if pin 8 is either left unconnected or $V_{IH}$ is applied to pin 8.
**Note 10:** Disable/Enable time is defined as the time from when the logic signal is applied to the DISABLE pin to when the output voltage has gone 50% of the way from its initial to its final value.
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Frequency Response for Various $R_L$

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

Frequency Response for Various $R_p$ and $R_Q$

3 dB Bandwidth vs Supply Voltage for $A_V = -1$

Peaking vs Supply Voltage for $A_V = -1$

3 dB Bandwidth vs Temperature for $A_V = -1$
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_V = +1$

Peaking vs Supply Voltage for $A_V = +1$

3 dB Bandwidth vs Temperature for $A_V = +1$

3 dB Bandwidth vs Supply Voltage for $A_V = +2$

Peaking vs Supply Voltage for $A_V = +2$

3 dB Bandwidth vs Temperature for $A_V = +2$

3 dB Bandwidth vs Supply Voltage for $A_V = +10$

Peaking vs Supply Voltage for $A_V = +10$

3 dB Bandwidth vs Temperature for $A_V = +10$
Typical Performance Curves — Contd.

**Frequency Response for Various $C_L$**

- $C_L = 100 \text{ pF}$
- $C_L = 50 \text{ pF}$
- $C_L = 20 \text{ pF}$
- $C_L = 0 \text{ pF}$

**Frequency Response for Various $C_{IN-}$**

- $C_{IN-} = 5 \text{ pF}$
- $C_{IN-} = 3 \text{ pF}$
- $C_{IN-} = 2 \text{ pF}$
- $C_{IN-} = 1 \text{ pF}$

**PSRR and CMRR vs Frequency**

**Frequency Response for Various $C_{IN-}$**

- $C_{IN-} = 5 \text{ pF}$
- $C_{IN-} = 3 \text{ pF}$
- $C_{IN-} = 2 \text{ pF}$
- $C_{IN-} = 1 \text{ pF}$

**2nd and 3rd Harmonic Distortion vs Frequency**

**Transimpedance ($R_{OL}$) vs Frequency**

**Transimpedance ($R_{OL}$) vs Die Temperature**
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature

Supply Current vs Die Temperature

Supply Current vs Supply Voltage

+ Input Resistance vs Die Temperature

Input Current vs Die Temperature

+ Input Bias Current vs Input Voltage

Output Voltage Swing vs Die Temperature

Short Circuit Current vs Die Temperature

PSRR & CMRR vs Die Temperature
Typical Performance Curves — Contd.

**Differential Gain vs DC Input Voltage, \( R_L = 150 \)**

\[ V_S = \pm 5V, \quad V_S = \pm 10V, \quad V_S = \pm 15V \]

\[ R_F = 560, \quad A_P = +2 \]

**Differential Phase vs DC Input Voltage, \( R_L = 150 \)**

\[ V_S = \pm 5V, \quad V_S = \pm 10V, \quad V_S = \pm 15V \]

\[ R_F = 560, \quad A_P = +2 \]

**Small Signal Pulse Response**

\[ R_F = R_G = 560 \]

\[ V_S = \pm 15V, \quad R_L = 150 \]

**Differential Gain vs DC Input Voltage, \( R_L = 500 \)**

\[ V_S = \pm 5V, \quad V_S = \pm 10V, \quad V_S = \pm 15V \]

\[ R_F = 560, \quad A_P = +2 \]

**Differential Phase vs DC Input Voltage, \( R_L = 500 \)**

\[ V_S = \pm 5V, \quad V_S = \pm 10V, \quad V_S = \pm 15V \]

\[ R_F = 560, \quad A_P = +2 \]

**Large Signal Pulse Response**

\[ R_F = R_G = 560 \]

\[ V_S = \pm 15V, \quad R_L = 150 \]

**Slew Rate vs Supply Voltage**

\[ R_F = R_G = 560 \]

\[ V_S = \pm 5V, \quad V_S = \pm 10V, \quad V_S = \pm 15V \]

\[ R_L = 500 \]

**Slew Rate vs Temperature**

\[ V_S = \pm 10V, \quad V_S = \pm 15V \]

\[ R_F = R_G = 560 \]

**Settling Time vs Settling Accuracy**

\[ \Delta V = \pm 10V, \quad \Delta V = \pm 15V \]

\[ R_F = R_G = 560 \]

\[ R_L = 1k \]

\[ V_S = \pm 15V \]
Typical Performance Curves — Contd.

**Long Term Settling Error**

- **ΔV** = ±10V
- **R<sub>f</sub>** = 560
- **V<sub>S</sub>** = ±15V

- **A<sub>V</sub>** = ±1
- **A<sub>V</sub>** = +1

**8-Lead Plastic DIP**

- Maximum Power Dissipation vs Ambient Temperature

**8-Lead Plastic SO**

- Maximum Power Dissipation vs Ambient Temperature

**ENABLE Response for a Family of D.C. Inputs**

- **A<sub>V</sub>** = +2, **R<sub>L</sub>** = 150, **V<sub>S</sub>** = ±15V

**DISABLE Response for a Family of D.C. Inputs**

- **A<sub>V</sub>** = +2, **R<sub>L</sub>** = 150, **V<sub>S</sub>** = ±15V

**Burn-In Circuit**

![Burn-In Circuit Diagram]
Differential Gain and Phase Test Circuit

Simplified Schematic
Applications Information

Product Description
The EL2166C is a current mode feedback amplifier that offers wide bandwidth and good video specifications at a moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL2166C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, $R_F$, and then the gain is set by picking the gain resistor, $R_G$. The curves at the beginning of the Typical Performance Curves section show the effect of varying both $R_F$ and $R_G$. The 3 dB bandwidth is only slightly dependent on the power supply voltage. The bandwidth reduces from 110 MHz to 95 MHz as supplies are varied from ±15V to ±5V. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below $\frac{1}{4}$". The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 $\mu$F tantalum capacitor in parallel with a 0.01 $\mu$F ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input
Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2166C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN^-}$ emphasizes this effect. The curve illustrates how the bandwidth can be extended over 30 MHz with some additional peaking with an additional 5 pF of capacitance at the $V_{IN^-}$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values
The EL2166C has been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields relatively flat frequency response with <1.5 dB peaking out to 110 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing $R_F$ to 430$\Omega$, bandwidth can be extended to 120 MHz with 4.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature
Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2166C was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 115 MHz to 95 MHz over the entire die junction temperature range of $0^\circ C < T < 150^\circ C$. 
Applications Information — Contd.

Supply Voltage Range
The EL2166C has been designed to operate with supply voltages from ±5V to ±15V. AC performance, including −3 dB bandwidth and differential gain and phase, shows little degradation as the supplies are lowered to ±5V. For example, as supplies are lowered from ±15V to ±5V, −3 dB bandwidth reduces only 15 MHz, and differential gain and phase remain less than 0.05%/0.02° respectively.

If a single supply is desired, values from +10V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2166C.

Disable Function
The EL2166C has a superior disable function that has been optimized for video performance. Time to disable/enable is around 75 ns.

During disable, the output of the EL2166C can withstand over 1500 V/μs slew rate signals at its output and the output does not draw excessive currents. The feed-through can be modeled as a 1.5 pF capacitor from VIN+ to the output, and the output impedance can be modeled as 4.4 pF in parallel with 180 kΩ to ground when disabled. Consequently, multiplexing with the EL2166C is very easy. Simply tie the outputs of multiple EL2166Cs together and drive the /DISABLE pins with standard TTL or CMOS signals. The disable signal applied to the /DISABLE pin is referenced to the GND pin. The GND pin can be tied as low as the VSS pin. This allows the EL2166C to be operated on a single supply. For example, one could tie the VSS and GND pins to 0V and VSS+ to +10V, and then use standard TTL or CMOS to drive the /DISABLE pin. Remember to keep the inputs of the EL2166C within their common mode range.

Multiplexing with the EL2166C
An example of multiplexing with the EL2166C and its response curve is shown below. Always be sure that no more than ±5V is applied between VIN+ and VIN−, which is compatible with standard video signals. This usually becomes an issue only when using the disable feature and amplifying large voltages.

Dual EL2166C Multiplexer

In the multiplexer above, suppose one amp is disabled and the other has amplified a signal to +10V at VOUT. The voltage at pin 2 of the dis-
Applications Information — Contd.

abled amplifier will now be +5V due to the resistor divider action. Therefore, any applied voltage at pin 3 of the disabled amplifier must remain above 0V if the voltage between pins 2 and 3 of the disabled amplifier is to remain less than 5V. Also keep in mind that each disabled amplifier adds more capacitance to the bus, as discussed above. See Disable Function, and Driving Cables and Capacitive Loads in this section, and the Frequency Response for Various \( C_L \) curves in the Typical Performance Curve section.

Settling Characteristics

The EL2166C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2166C is not slew rate limited, therefore any size step up to \( \pm 10V \) gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for \( AV = +1 \), there is approximately a 0.02% residual which tails away to 0.01% in about 20 \( \mu s \). This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For \( AV = -1 \), due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With \( AV = -1 \), 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2166C amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2166C remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

\[
P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}
\]

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

\[
P_{DMAX} = 2 \cdot V_S \cdot I_S + (V_S - V_{OUT}) \cdot \frac{V_{OUT}}{R_L}
\]

where \( I_S \) is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL2166C maintains almost constant supply current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

The EL2166C consumes typically 7.5 mA and maximum 10.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum values if it cannot reach half supply. If we set the two \( P_{DMAX} \) equations equal to each other, and solve for \( V_S \), we can get a family of curves for various loads and output voltages according to:

\[
V_S = \frac{R_L \cdot (T_{JMAX} - T_{AMAX}) + (V_{OUT})^2}{\theta_{JA} \cdot (2 \cdot I_S \cdot R_L) + V_{OUT}}
\]
Applications Information — Contd.
The following curves show supply voltage (± V<sub>S</sub>) vs R<sub>LOAD</sub> for various output voltage swings for the 2 different packages. The curves assume worst case conditions of T<sub>A</sub> = +85°C and I<sub>S</sub> = 10 mA.

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit
The EL2166C has an internal current limit that protects the circuit in the event of the output being shorted to ground. This limit is set at 80 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 50 mA. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2166C to survive an indefinite short.

Driving Cables and Capacitive Loads
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2166C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, R<sub>G</sub>, can be chosen to make up for the gain loss created by this additional series resistor at the output.
**EL2166C Macromodel**

* Revision A, May 1994
* AC Characteristics used $C_{IN}$ (pin 2) = 1 pF; $R_F = 560\Omega$
* Connections: + input  
  *  
  *  
  *  
  *  
  *  
  *  
  .subckt EL2166C/EL 3 2 7 4 6
  *
* Input Stage
* e1 10 0 3 0 1.0
  via 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5μA
iihm 2 0 5μA
rl2 3 0 2Meg
*
* Slew Rate Limiting
* h1 13 0 via 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
* e2 30 0 14 0 0.00166666666
l3 30 17 0.8μH
r5 17 0 500
*
* Transimpedance Stage
* g1 0 18 17 0 1.0
ro1 18 0 2Meg
cdp 18 0 2.9pF
*
* Output Stage
* q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
* Supply Current
* ips 74 2mA
*
* Error Terms
* ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.35K
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is = 5e−15 bf = 200 tf = 0.1ns)
.model qp npn (is = 5e−15 bf = 200 tf = 0.1ns)
.model dclamp d (is = 1e−30 ibv = 0.266 bv = 2.8 n = 4)
.ends
Features

- Single (EL2170C), dual (EL2270C) and quad (EL2470C) topologies
- 1 mA supply current (per amplifier)
- 70 MHz −3 dB bandwidth
- Tiny SOT23-5 Package (EL2170C)
- Low cost
- Single- and dual-supply operation down to ±1.5V
- 0.15%/0.15° diff. gain/diff. phase into 150Ω
- 800 V/µs slew rate
- Large output drive current: 100 mA (EL2170C)
  - 55 mA (EL2270C)
  - 55 mA (EL2470C)
- Also available with disable in single (EL2176C) and dual (EL2276C)
- Higher speed EL2180C/EL2186C family also available (3 mA/250 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

General Description

The EL2170C/EL2270C/EL2470C are single/dual/quad current-feedback operational amplifiers which achieve a −3 dB bandwidth of 70 MHz at a gain of +1 while consuming only 1 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. In spite of their low supply current, the EL2270C and the EL2470C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2170C can output 100 mA with similar output swings. These attributes make the EL2170C/EL2270C/EL2470C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For applications where board space is extremely critical, the EL2170C is available in the tiny 5-Lead SOT23 package, which has a footprint 28% the size of an 8-Lead SOIC. The EL2170C/EL2270C/EL2470C are each also available in industry standard pinouts in PDIP and SOIC packages.

For Single and Dual applications with disable, consider the EL2176C (8-Pin Single) or EL2276C (14-Pin Dual). For higher speed applications where power is still a concern, consider the EL2180C/EL2186C family which also comes in similar Single, Dual, Triple and Quad configurations. The EL2180C/EL2186C family provides a −3 dB bandwidth of 250 MHz while consuming 3 mA of supply current per amplifier.

Connection Diagrams

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2170CN</td>
<td>−40°C to +85°C</td>
<td>8-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2170CS</td>
<td>−40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2170CW</td>
<td>−40°C to +85°C</td>
<td>5-Pin SOT23</td>
<td>MDP0038</td>
</tr>
<tr>
<td>EL2270CN</td>
<td>−40°C to +85°C</td>
<td>8-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2270CS</td>
<td>−40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2470CN</td>
<td>−40°C to +85°C</td>
<td>14-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2470CS</td>
<td>−40°C to +85°C</td>
<td>14-Pin SOIC</td>
<td>MDP0027</td>
</tr>
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*See Ordering Information section of databook.*
## Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between ( V_{S+} ) and ( V_{S-} )</td>
<td>+12.6 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Common-Mode Input Voltage ( V_{S-} ) to ( V_{S+} )</td>
<td>±6 V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Differential Input Voltage</td>
<td>±6 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current into +IN or -IN</td>
<td>±7.5 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Power Dissipation</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>-40°C to +85°C</td>
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<td></td>
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<tr>
<td>Operating Junction Temperature</td>
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### Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

## Test Level:

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
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<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at ( T_A = 25^\circ C ) and QA sample tested at ( T_A = 25^\circ C ).</td>
</tr>
<tr>
<td>III</td>
<td>( T_{MAX} ) and ( T_{MIN} ) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at ( T_A = 25^\circ C ) for information purposes only.</td>
</tr>
</tbody>
</table>

## DC Electrical Characteristics \( V_S = \pm 5V, R_L = 150\Omega, T_A = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td></td>
<td>2.5</td>
<td>15</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Average Input Offset Voltage Drift</td>
<td>Measured from ( T_{MIN} ) to ( T_{MAX} )</td>
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<td></td>
<td></td>
<td>V</td>
<td>( \mu V/\circ C )</td>
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<tr>
<td>( dV_{OS} )</td>
<td>( V_{OS} ) Matching</td>
<td>EL2270C, EL2470C only</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>mV</td>
</tr>
<tr>
<td>( +I_{IN} )</td>
<td>+ Input Current</td>
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<td>0.5</td>
<td>5</td>
<td></td>
<td>I</td>
<td>( \mu A )</td>
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<tr>
<td>( d+I_{IN} )</td>
<td>+ ( I_{IN} ) Matching</td>
<td>EL2270C, EL2470C only</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>nA</td>
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<tr>
<td>( -I_{IN} )</td>
<td>- Input Current</td>
<td></td>
<td>4</td>
<td>15</td>
<td></td>
<td>I</td>
<td>( \mu A )</td>
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<td>( d-I_{IN} )</td>
<td>- ( I_{IN} ) Matching</td>
<td>EL2270C, EL2470C only</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
<td>( \mu A )</td>
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<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>( V_{CM} = \pm 3.5V )</td>
<td>45</td>
<td>50</td>
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<td>I</td>
<td>dB</td>
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<td>(-ICMR)</td>
<td>- Input Current Common Mode Rejection</td>
<td>( V_{CM} = \pm 3.5V )</td>
<td>4</td>
<td>10</td>
<td></td>
<td>I</td>
<td>( \mu A/V )</td>
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<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S ) is moved from ( \pm 4V ) to ( \pm 6V )</td>
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<td>70</td>
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<td>I</td>
<td>dB</td>
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<tr>
<td>(-IPSR)</td>
<td>- Input Current Power Supply Rejection</td>
<td>( V_S ) is moved from ( \pm 4V ) to ( \pm 6V )</td>
<td>0.5</td>
<td>5</td>
<td></td>
<td>I</td>
<td>( \mu A/V )</td>
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<tr>
<td>( R_{OL} )</td>
<td>Transimpedance</td>
<td>( V_{OUT} = \pm 2.5V )</td>
<td>150</td>
<td>400</td>
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<td>I</td>
<td>k( \Omega )</td>
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<td>( +R_{IN} )</td>
<td>+ Input Resistance</td>
<td>( V_{CM} = \pm 3.5V )</td>
<td>1</td>
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<td></td>
<td>I</td>
<td>M( \Omega )</td>
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<td>( +C_{IN} )</td>
<td>+ Input Capacitance</td>
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<td>V</td>
<td>pF</td>
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<td>CMIR</td>
<td>Common Mode Input Range</td>
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<td>±4.0</td>
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<td>I</td>
<td>V</td>
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2-386
**DC Electrical Characteristics — Contd.**

\( V_S = \pm 5\text{V}, R_L = 1500\text{\Omega}, T_A = 25^\circ\text{C} \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing</td>
<td>( V_S = \pm 5 )</td>
<td>( \pm 3.5 )</td>
<td>( \pm 4.0 )</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5 \text{ Single-Supply, High} )</td>
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<td>V</td>
<td>V</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( V_S = +5 \text{ Single-Supply, Low} )</td>
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<td>Output Current</td>
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<td>100</td>
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<td>mA</td>
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<td>EL2270C only, per Amplifier</td>
<td>50</td>
<td>55</td>
<td>I</td>
<td>mA</td>
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<td></td>
<td></td>
<td>EL2470C only, per Amplifier</td>
<td>50</td>
<td>55</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>Per Amplifier</td>
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<td>2</td>
<td>I</td>
<td>mA</td>
</tr>
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</table>

**AC Electrical Characteristics**

\( V_S = \pm 5\text{V}, R_F = R_G = 1 \text{k\Omega}, R_L = 1500\text{\Omega}, T_A = 25^\circ\text{C} \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
</tr>
</thead>
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<tr>
<td>(-3\text{ dB BW})</td>
<td>(-3\text{ dB Bandwidth})</td>
<td>( A_V = +1 )</td>
<td>70</td>
<td>V</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>(-3\text{ dB BW})</td>
<td>(-3\text{ dB Bandwidth})</td>
<td>( A_V = +2 )</td>
<td>60</td>
<td>V</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>( V_{OUT} = \pm 2.5\text{V}, A_V = +2 )</td>
<td>400</td>
<td>800</td>
<td>IV</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>( t_r, t_f )</td>
<td>Rise and Fall Time</td>
<td>( V_{OUT} = \pm 500\text{mV} )</td>
<td>4.5</td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{pd} )</td>
<td>Propagation Delay</td>
<td>( V_{OUT} = \pm 500\text{mV} )</td>
<td>4.5</td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>( V_{OUT} = \pm 500\text{mV} )</td>
<td>3.0</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( t_s )</td>
<td>0.1% Settling</td>
<td>( V_{OUT} = \pm 2.5\text{V}, A_V = -1 )</td>
<td>40</td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>( A_V = +2, R_L = 150\Omega ) (Note 1)</td>
<td>0.15</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>dP</td>
<td>Differential Gain</td>
<td>( A_V = +2, R_L = 150\Omega ) (Note 1)</td>
<td>0.02</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>( A_V = +1, R_L = 50\Omega ) (Note 1)</td>
<td>0.02</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>dP</td>
<td>Differential Gain</td>
<td>( A_V = +1, R_L = 50\Omega ) (Note 1)</td>
<td>0.01</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>C_S</td>
<td>Channel Separation</td>
<td>EL2270C, EL2470 only, ( f = 5\text{MHz} )</td>
<td>85</td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** DC offset from 0V to 0.714V, AC amplitude 286 mVp.p, \( f = 3.58\text{MHz} \).
Test Circuit (per Amplifier)

![Test Circuit Diagram]

Simplified Schematic (per Amplifier)

![Simplified Schematic Diagram]
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Frequency Response for Various \( R_p \) and \( R_G \)

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

Frequency Response for Various \( R_L \) and \( C_L \)

Transimpedance (\( R_{OL} \))

PSRR and CMRR

Frequency Response for Various \( C_{IN-} \)
Typical Performance Curves — Contd.

-3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains

Supply Current vs Supply Voltage

Common-Mode Input Range vs Supply Voltage

Slew Rate vs Supply Voltage
Typical Performance Curves — Contd.

**Input Bias Current vs Die Temperature**

**Short-Circuit Current vs Die Temperature**

**Transimpedance (R<sub>OL</sub>) vs Die Temperature**

**-3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains**

**-3 dB Bandwidth and Peaking vs Die Temperature for Various Inverting Gains**

**Supply Current vs Die Temperature**

**Input Voltage Range vs Die Temperature**

**Slew Rate vs Die Temperature**
Typical Performance Curves — Contd.

**Differential Gain and Phase vs DC Input Voltage at 3.58 MHz/Av = +2**

![Graph showing differential gain and phase vs DC input voltage](image1)

**Differential Gain and Phase vs DC Input Offset at 3.58 MHz/Av = +1**

![Graph showing differential gain and phase vs DC input offset](image2)

**Settling Time vs Settling Accuracy**

![Graph showing settling time vs settling accuracy](image3)

**Small-Signal Step Response**

![Small-signal step response](image4)

**Large-Signal Step Response**

![Large-signal step response](image5)

**8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature**

![Graph showing power dissipation vs temperature](image6)

**8-Lead SO Maximum Power Dissipation vs Ambient Temperature**

![Graph showing power dissipation vs temperature](image7)
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

14-Lead SO
Maximum Power Dissipation vs Ambient Temperature

Channel Separation vs Frequency

5-Lead Plastic SOT23
Maximum Power Dissipation vs Ambient Temperature

2170-39

2170-40

2170-41

2170-47
Applications Information

Product Description

The EL2170C/EL2270C/EL2470C are current-feedback operational amplifiers that offer a wide -3 dB bandwidth of 70 MHz and a low supply current of 1 mA per amplifier. All of these products also feature high output current drive. The EL2170C can output 100 mA, while the EL2270C and the EL2470C can output 55 mA per amplifier. The EL2170C/EL2270C/EL2470C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2170C/EL2270C/EL2470C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their -3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2170C/EL2270C/EL2470C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For applications where board space is extremely critical, the EL2170C is available in the tiny 5-Lead SOT23 package, which has a footprint 28% the size of an 8-Lead SOIC. The EL2170C/EL2270C/EL2470C are each also available in industry standard pinouts in PDIP and SOIC packages.

For Single and Dual applications with disable, consider the EL2176C (8-Pin Single) and EL2276C (14-Pin Dual). If higher speed is required, refer to the EL2180C/EL2186C family which provides Singles, Duals, Triples, and Quads with 250 MHz of bandwidth while consuming 3 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input

Any manufacturer’s high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.
Applications Information — Contd.
The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2170C/EL2270C/EL2470C have less bandwidth than expected. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various \( R_F \) and \( R_G \), and Frequency Response for Various \( C_{IN} \).

Feedback Resistor Values
The EL2170C/EL2270C/EL2470C have been designed and specified at gains of +1 and +2 with \( R_F = 1 \text{k}\Omega \). This value of feedback resistor gives 70 MHz of -3 dB bandwidth at \( A_V = +1 \) with about 1.5 dB of peaking, and 60 MHz of -3 dB bandwidth at \( A_V = +2 \) with about 0.5 dB of peaking. Since the EL2170C/EL2270C/EL2470C are current-feedback amplifiers, it is also possible to change the value of \( R_F \) to get more bandwidth. As seen in the curve of Frequency Response For Various \( R_F \) and \( R_G \), bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2170C/EL2270C/EL2470C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2170C/EL2270C/EL2470C to maintain about the same -3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of \( R_F \) below the specified 1 k\Omega and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation
The EL2170C/EL2270C/EL2470C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2170C/EL2270C/EL2470C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2170C/EL2270C/EL2470C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2170C/EL2270C/EL2470C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2170C/EL2270C/EL2470C have an input range which spans from 1V to 4V. The output range of the EL2170C/EL2270C/EL2470C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance
For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2170C/EL2270C/EL2470C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically more than the entire 1 mA supply current of each EL2170C/EL2270C/EL2470C amplifier! Special circuitry has been incorporated in the EL2170C/EL2270C/EL2470C to reduce the variation of output impedance with current output. This results in \( dG \) and \( dP \) specifications of 0.15% and 0.15° while driving 150Ω at a gain of +2.
Applications Information — Contd.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2170C/EL2270C/EL2470C have dG and dP specifications of 0.01% and 0.02° respectively while driving 500 Ω at Av = +1.

Output Drive Capability

In spite of its low 1 mA of supply current, the EL2170C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2270C and the EL2470C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2170C is capable of driving 500 Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2270C and EL2470C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2170C/EL2270C/EL2470C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (Rg) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (RF) to reduce the peaking.

Current Limiting

The EL2170C/EL2270C/EL2470C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2170C/EL2270C/EL2470C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when RL falls below about 25Ω, it is important to calculate the maximum junction temperature (TjMAX) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2170C/EL2270C/EL2470C to remain in the safe operating area. These parameters are calculated as follows:

\[
Tj_{\text{MAX}} = T_{\text{MAX}} + (\theta_{JA} \times n \times P_{\text{DMAX}}) \quad [1]
\]

where:

- \(T_{\text{MAX}}\) = Maximum Ambient Temperature
- \(\theta_{JA}\) = Thermal Resistance of the Package
- \(n\) = Number of Amplifiers in the Package
- \(P_{\text{DMAX}}\) = Maximum Power Dissipation of Each Amplifier in the Package.

\(P_{\text{DMAX}}\) for each amplifier can be calculated as follows:

\[
P_{\text{DMAX}} = (2 \times V_{S} \times I_{S_{\text{MAX}}}) + (V_{S} - V_{\text{OUTMAX}}) \times (V_{\text{OUTMAX}}/R_{L}) \quad [2]
\]

where:

- \(V_{S}\) = Supply Voltage
- \(I_{S_{\text{MAX}}}\) = Maximum Supply Current of 1 Amplifier
- \(V_{\text{OUTMAX}}\) = Max. Output Voltage of the Application
- \(R_{L}\) = Load Resistance
Typical Application Circuits

Inverting 200 mA Output Current Distribution Amplifier

Fast-Settling Precision Amplifier
Typical Application Circuits — Contd.

**Differential Line-Driver/Receiver**

![Differential Line-Driver/Receiver Diagram]

- **Transmitter**:
  - 2x IN+ with +5V and 0.1 μF capacitors.
  - EL2170C or 1/2 EL2270C or 1/4 EL2470C with VD+.
  - IN- with -5V and 0.1 μF capacitors.
  - OUT+ and OUT- with 120, 240, 1k, and 0.1 μF components.
- **Receiver**:
  - 2x IN+ with +5V and 0.1 μF capacitors.
  - EL2170C or 1/2 EL2270C or 1/4 EL2470C with VD+.
  - IN- with -5V and 0.1 μF capacitors.
  - OUT with 240, 1k, 1k, and 0.1 μF components.

2-398
EL2170C/EL2270C/EL2470C Macromodel

* Revision A, March 1995
* AC characteristics used $R_f = R_g = 1 \Omega$, $RL = 150 \Omega$
* Connections:
  * + input
  * − input
  * + $V_{supply}$
  * − $V_{supply}$
  * output

.subckt EL2170/el 3 2 7 4 6

* Transimpedance Stage
  * $g_1 \ 0 \ 18 \ 17 \ 0 \ 1.0$
  * $r_0 \ 18 \ 0 \ 400 \ K$
  * $c_{dp} \ 18 \ 0 \ 1.9 \ pF$

* Output Stage

* Input Stage
  * $e_{11} \ 0 \ 0 \ 3 \ 0 \ 1.0$
  * $v_{is} \ 10 \ 9 \ 0 \ V$
  * $h_{2} \ 9 \ 12 \ v_{xx} \ 1.0$
  * $r_{1} \ 2 \ 11 \ 165$
  * $l_{1} \ 11 \ 12 \ 25 \ nH$
  * $i_{inp} \ 3 \ 0.5 \ uA$
  * $i_{inm} \ 2 \ 0.4 \ uA$
  * $r_{12} \ 3 \ 0 \ 4 \ M\Omega$

* Slew Rate Limiting
  * $h_{1} \ 13 \ 0 \ v_{is} \ 600$
  * $r_{2} \ 13 \ 14 \ 1 \ K$
  * $d_{1} \ 14 \ 0 \ dclamp$
  * $d_{2} \ 0 \ 14 \ dclamp$

* High Frequency Pole
  * $e_{2} \ 30 \ 0 \ 14 \ 0 \ 0.0016666666666666$
  * $l_{3} \ 30 \ 17 \ 0.5 \ uH$
  * $c_{5} \ 17 \ 0 \ 0.69 \ pF$
  * $r_{5} \ 17 \ 0 \ 300$

* Supply Current
  * $i_{ps} \ 7 \ 4 \ 1 \ nA$

* Error Terms
  * $i_{vos} \ 0 \ 23 \ 2 \ mA$
  * $v_{xx} \ 23 \ 0 \ V$
  * $e_{4} \ 24 \ 0 \ 3 \ 0 \ 1.0$
  * $e_{5} \ 25 \ 0 \ 7 \ 0 \ 1.0$
  * $e_{6} \ 26 \ 0 \ 4 \ 0 \ -1.0$
  * $r_{9} \ 24 \ 23 \ 0.316 \ K$
  * $r_{10} \ 25 \ 23 \ 3.2 \ K$

* Models
  * .model qn npn(is = 5e-15 bf = 200 tf = 0.01nS)
  * .model qp npn(is = 5e-15 bf = 200 tf = 0.01nS)
  * .model dclamp d(is = 1e-30 ibv = 0.266
    + bv = 1.3v n = 4)
.ends
EL2170C/EL2270C/EL2470C Macromodel — Contd.
**Features**

- 30 MΩ transimpedance
- 142 MHz - 3 dB bandwidth ($A_v = +1$)
- 120 MHz - 3 dB bandwidth ($A_v = +2$)
- 1 mV input offset voltage
- 2 μA negative input bias current
- 86 dB common-mode rejection ratio
- 92 dB power supply rejection ratio
- Low supply current, 8.5 mA
- Wide supply range, ±4.5V to ±16.5V
- 80 mA peak output current
- High capacitive load toleration
- Input/output compliance to ±2V of supplies
- 1,000 V/μs slew rate
- 50 ns settling to 0.1%
- 90 ns settling to 0.01%
- -70 dB distortion @ 4 MHz
- Low cost

**Applications**

- Instrumentation ciruity
- Current to voltage convertors
- RGB amplifiers
- DAC/ADC output amplifier/ buffer
- Cable drivers
- Low distortion communications
- Medical imaging
- CCD imaging
- Infrared image enhancement

**General Description**

The EL2175C is a low offset, high transimpedance current mode feedback amplifier with a -3 dB bandwidth of 120 MHz at a gain of +2. Built on Elantec's proprietary monolithic complementary bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than conventional voltage feedback amplifiers.

The high 30 MΩ transimpedance gain and low input referred offset of the EL2175 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

In addition, the common-mode and power supply rejection have been greatly improved over earlier current mode feedback amplifiers and the input offset voltage and current have been trimmed to rival that of good conventional voltage feedback amplifiers. The part has a typical slew rate of 1,000 V/μs and a 0.01% settling time of less than 90 ns in inverting mode. At a gain of +2 and an output signal level of 2 Vp-p, the total harmonic distortion is only -70 dB at 4 MHz.

The amplifier can operate on any supply from 9V (±4.5V) to 33V (±16.5V), yet consumes only 8.5 mA at any supply voltage. Using the industry standard pinout, the EL2175C is available in both P-DIP and SO packages.

**Connection Diagram**

![Connection Diagram](image-url)

Manufactured under U.S. Patent No. 5,418,495
### Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between (V_{S+}) and (V_S-)</td>
<td>+33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Voltage between (I_{N+}) and (I_{N-})</td>
<td>±6V</td>
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<td></td>
<td></td>
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<tr>
<td>Current into (I_{N+}) and (I_{N-})</td>
<td>4 mA</td>
<td></td>
<td></td>
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<tr>
<td>Operating Ambient Temperature Range</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Operating Junction Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

### Test Level

- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at \(T_A = 25°C\) and QA sample tested at \(T_A = 25°C\).
- **III**: QA sample tested per QA test plan QCX0002.
- **IV**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at \(T_A = 25°C\) for information purposes only.

### Open Loop DC Electrical Characteristics

\(V_S = \pm 15V, R_L = 500\Omega, T_A = 25°C\) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td></td>
<td>25°C</td>
<td>1</td>
<td>3</td>
<td></td>
<td>I</td>
<td>mV</td>
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<tr>
<td>(TC V_{OS})</td>
<td>Average Offset Voltage Drift (Note 1)</td>
<td>Full</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu V/°C)</td>
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<tr>
<td>(I_{IN+})</td>
<td>+ Input Current</td>
<td>25°C</td>
<td></td>
<td>-2.5</td>
<td>±6</td>
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<td>I</td>
<td>(\mu A)</td>
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<td>(I_{IN-})</td>
<td>- Input Current</td>
<td>25°C</td>
<td></td>
<td>±2</td>
<td>±7</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
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<td>CMRR</td>
<td>Common Mode Rejection Ratio (Note 2)</td>
<td>25°C</td>
<td>79</td>
<td>86</td>
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<td>II</td>
<td>dB</td>
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<td>ICMR</td>
<td>-Input Current Common Mode Rejection (Note 2)</td>
<td>25°C</td>
<td>27</td>
<td>100</td>
<td></td>
<td></td>
<td>I</td>
<td>nA/V</td>
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<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Note 3)</td>
<td>25°C</td>
<td>84</td>
<td>92</td>
<td></td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>IPSR</td>
<td>-Input Current Power Supply Rejection (Note 3)</td>
<td>25°C</td>
<td>28</td>
<td>225</td>
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<td></td>
<td>I</td>
<td>nA/V</td>
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<tr>
<td>(R_{OL})</td>
<td>Transimpedance (Note 4)</td>
<td>(V_S = \pm 15V, R_L = 500\Omega)</td>
<td>25°C</td>
<td>30</td>
<td></td>
<td></td>
<td>I</td>
<td>(M\Omega)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5V, R_L = 150\Omega)</td>
<td>25°C</td>
<td>5</td>
<td>25</td>
<td></td>
<td>I</td>
<td>(M\Omega)</td>
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<tr>
<td>(R_{IN+})</td>
<td>+ Input Resistance</td>
<td>25°C</td>
<td>18</td>
<td>25</td>
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<td></td>
<td>II</td>
<td>(M\Omega)</td>
</tr>
<tr>
<td>(C_{IN+})</td>
<td>+ Input Capacitance</td>
<td>25°C</td>
<td>2.5</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>(pF)</td>
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<tr>
<td>CMIR</td>
<td>Common Mode Input Range (Note 2)</td>
<td>(V_S = \pm 15V)</td>
<td>25°C</td>
<td>12</td>
<td>±12.5</td>
<td></td>
<td>I</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td>(V_S = \pm 5V)</td>
<td>25°C</td>
<td>2.0</td>
<td>±2.5</td>
<td></td>
<td>I</td>
<td>V</td>
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Open Loop DC Electrical Characteristics

$V_S = \pm 15V, R_L = 500\Omega, T_A = 25^\circ C$ unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Levels</th>
<th>Units</th>
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<tbody>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing</td>
<td>$R_L = 500\Omega$ $V_S = \pm 15V$</td>
<td>$25^\circ C$</td>
<td>$\pm 12, 3$</td>
<td>$\pm 13$</td>
<td>I</td>
<td></td>
<td>I</td>
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<tr>
<td></td>
<td></td>
<td>$R_L = 150\Omega$ $V_S = \pm 15V$</td>
<td>$25^\circ C$</td>
<td>$\pm 11.7$</td>
<td></td>
<td>V</td>
<td></td>
<td>V</td>
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<td></td>
<td></td>
<td>$R_L = 150\Omega$ $V_S = \pm 5V$</td>
<td>$25^\circ C$</td>
<td>$\pm 2.7$</td>
<td>$\pm 3.0$</td>
<td>I</td>
<td></td>
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<td>$I_{SC}$</td>
<td>Output Short Circuit Current (Note 4)</td>
<td>$V_S = \pm 5V$</td>
<td>$25^\circ C$</td>
<td>$55$</td>
<td>$90$</td>
<td>I</td>
<td>mA</td>
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<td></td>
<td></td>
<td>$V_S = \pm 15V$</td>
<td>$80$</td>
<td>$135$</td>
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<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$V_S = \pm 15V$</td>
<td>$25^\circ C$</td>
<td>$8.5$</td>
<td>$10.25$</td>
<td>I</td>
<td>mA</td>
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**Closed Loop AC Electrical Characteristics**

\( V_S = \pm 15V, A_V = +2, R_P = 750\Omega, R_L = 500\Omega, T_A = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>BW</td>
<td>( V_S = \pm 15V, A_V = +2, R_P = 750\Omega )</td>
<td>120</td>
<td>V</td>
<td>MHz</td>
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<td></td>
<td>( V_S = \pm 15V, A_V = +1, R_P = 1K\Omega )</td>
<td>142</td>
<td>V</td>
<td>MHz</td>
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<td></td>
<td>( V_S = \pm 5V, A_V = +2, R_P = 750\Omega )</td>
<td>98</td>
<td>V</td>
<td>MHz</td>
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<td></td>
<td>( V_S = \pm 5V, A_V = +1, R_P = 1K\Omega )</td>
<td>113</td>
<td>V</td>
<td>MHz</td>
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<td>SR</td>
<td>Slew Rate (Notes 6, 8)</td>
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<td></td>
<td>I</td>
<td>V/μs</td>
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<tr>
<td></td>
<td>( R_L = 500\Omega )</td>
<td>500</td>
<td></td>
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<tr>
<td></td>
<td>( R_P = 1 K\Omega, R_G = 110\Omega R_L = 500\Omega )</td>
<td>1000</td>
<td>V</td>
<td>V/μs</td>
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<tr>
<td></td>
<td>Rise Time, Fall Time (Note 8)</td>
<td>3.7</td>
<td>V</td>
<td>ns</td>
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<tr>
<td></td>
<td>Propagation Delay</td>
<td>7.7</td>
<td>V</td>
<td>ns</td>
<td></td>
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<tr>
<td>( t_S )</td>
<td>Overshoot (Note 8)</td>
<td>6</td>
<td>V</td>
<td>%</td>
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<tr>
<td></td>
<td>( V_{OUT} = \pm 500 \text{ mV} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_s )</td>
<td>0.1% Settling Time (Note 8)</td>
<td>( \Delta V_{OUT} = \pm 10V ) ( A_V = 1 )</td>
<td>70</td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( A_V = -1 )</td>
<td>50</td>
<td>V</td>
<td>ns</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( A_V = 2 )</td>
<td>60</td>
<td>V</td>
<td>ns</td>
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<tr>
<td>( t_s )</td>
<td>0.01% Settling Time</td>
<td>( \Delta V_{OUT} = \pm 10V ) ( A_V = 1 )</td>
<td>900</td>
<td>V</td>
<td>ns</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( A_V = -1 )</td>
<td>90</td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( A_V = 2 )</td>
<td>500</td>
<td>V</td>
<td>ns</td>
<td></td>
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<tr>
<td>dG</td>
<td>Differential Gain (Notes 7, 8)</td>
<td>( R_L = 150\Omega )</td>
<td>0.09</td>
<td>V</td>
<td>%</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( R_L = 500\Omega )</td>
<td>0.02</td>
<td>V</td>
<td>%</td>
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<tr>
<td>dP</td>
<td>Differential Phase (Notes 7, 8)</td>
<td>( R_L = 150\Omega )</td>
<td>0.5</td>
<td>V</td>
<td>deg (°)</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( R_L = 500\Omega )</td>
<td>0.16</td>
<td>V</td>
<td>deg (°)</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Measured from \( T_{MIN} \) to \( T_{MAX} \)

**Note 2:** \( V_{CM} = \pm 12V \) for \( V_S = \pm 15V \) and \( T_A = 25^\circ C \)

\( V_{CM} = \pm 2V \) for \( V_S = \pm 5V \) and \( T_A = 25^\circ C \)

CMIR is guaranteed by the part passing CMRR at the rated common-mode swing.

**Note 3:** The supplies are moved from \( \pm 4.5V \) to \( \pm 15V \).

**Note 4:** \( V_{OUT} = \pm 10V \) for \( V_S = \pm 15V \), and \( V_{OUT} = \pm 2V \) for \( V_S = \pm 5V \).

**Note 5:** A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

**Note 6:** Slew Rate is with \( V_{OUT} \) from \( +10V \) to \( -10V \) and measured at the 25% and 75% points.

**Note 7:** DC offset from \( -0.714V \) through \( +0.714V \), AC amplitude \( 286 \text{ mV}_{pp} \), \( f = 3.58 \text{ MHz} \).

**Note 8:** All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
Typical Performance Curves

Frequency Response for $A_v = -1$ and for Various $R_p$ Values

Frequency Response for $A_v = +1$ and for Various $R_p$ Values

Frequency Response for $A_v = +2$ and for Various $R_p$ Values

Frequency Response for $A_v = +10$ and for Various $R_p$ Values

Frequency Response for Various Values of $R_L$

Frequency Response for Various Values of $C_L$

3 dB Bandwidth vs Supply Voltage for $A_v = -1$

Peaking vs Supply Voltage for $A_v = -1$

3 dB Bandwidth vs Temperature for $A_v = -1$
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_v = +1$

- $R_e = 500 \Omega$
- $R_f = 560 \Omega$
- $R_f = 750 \Omega$

Supply Voltage (±V)

Peaking vs Supply Voltage for $A_v = +1$

- $R_e = 500 \Omega$
- $R_f = 560 \Omega$
- $R_f = 750 \Omega$
- $R_f = 1.3k$
- $R_f = 1k$

Supply Voltage (±V)

3 dB Bandwidth vs Temperature for $A_v = +1$

- $V_s = ±15V$
- $R_f = 1k$
- $V_s = ±10V$
- $R_f = 500 \Omega$
- $V_s = ±5V$
- $V_s = ±3.5V$

Die Temperature (°C)

3 dB Bandwidth vs Supply Voltage for $A_v = +2$

- $R_e = 500 \Omega$
- $R_f = 560 \Omega$
- $R_f = 750 \Omega$
- $R_f = 1.3k$
- $R_f = 1k$

Supply Voltage (±V)

Peaking vs Supply Voltage for $A_v = +2$

- $R_e = 500 \Omega$
- $R_f = 560 \Omega$
- $R_f = 750 \Omega$
- $R_f = 1.3k$
- $R_f = 1k$

Supply Voltage (±V)

3 dB Bandwidth vs Temperature for $A_v = +2$

- $V_s = ±15V$
- $RF = 750n$
- $V_s = ±10V$
- $RF = 500n$
- $V_s = ±5V$
- $V_s = ±3.5V$

Die Temperature (°C)

3 dB Bandwidth vs Supply Voltage for $A_v = +10$

- $R_e = 560 \Omega$
- $R_f = 750 \Omega$
- $R_f = 1k$
- $R_f = 1.3k$
- $R_f = 500 \Omega$

Supply Voltage (±V)

Peaking vs Supply Voltage for $A_v = +10$

- $R_e = 500 \Omega$
- $R_f = 560 \Omega$, $750 \Omega$, $1k$, $1.3k$

Supply Voltage (±V)

3 dB Bandwidth vs Temperature for $A_v = +10$

- $V_s = ±15V$
- $R_f = 750 \Omega$
- $V_s = ±10V$
- $R_f = 500 \Omega$
- $V_s = ±5V$
- $V_s = ±3.5V$

Die Temperature (°C)
Typical Performance Curves — Contd.

Frequency Response for Various Values of CIN

Voltage and Current Noise vs Frequency

Transimpedance (R_{OL}) vs Frequency

Closed-Loop Output Impedance vs Frequency

Slew Rate vs Supply Voltage

Slew Rate vs Temperature

PSRR and CMRR vs Frequency

Second and Third Harmonic Distortion vs Frequency

Transimpedance (R_{OL}) vs Die Temperature

Voltage and Current Noise vs Frequency

Transimpedance (R_{OL}) vs Die Temperature

Slew Rate vs Temperature
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)

Supply Current vs Die Temperature

Supply Current vs Supply Voltage

Input Resistance vs Die Temperature

Input Current vs Die Temperature

Output Voltage Swing vs Die Temperature

PSRR and CMRR vs Die Temperature

DIE TEMPERATURE (°C)

DIE TEMPERATURE (°C)

DIE TEMPERATURE (°C)

DIE TEMPERATURE (°C)
Typical Performance Curves — Contd.

Small Signal Pulse Response

Large Signal Pulse Response

Settling Time vs Setting Accuracy

8-Pin Package
Power Dissipation vs Ambient Temperature

Long Term Settling Error

Differential Phase vs DC Input Voltage
$R_L = 500$

Differential Gain vs DC Input Voltage
$R_L = 500$

Differential Phase vs DC Input Voltage
$R_L = 150$

Differential Gain vs DC Input Voltage
$R_L = 150$
Applications Information

Product Description
The EL2175 is a single current mode feedback amplifier that offers wide bandwidth, high gain, low distortion and exceptional DC specifications for a CMF type amplifier at moderate supply current. Due to the current feedback architecture, the closed loop 3 dB bandwidth is dependent on the feedback resistor, RF, and then the gain is set by picking the gain set resistor, RG. The curves at the beginning of the “Typical Performance Curves” section show the effect of varying both RF and RG. The 3 dB bandwidth is significantly less dependent on supply voltage than earlier CMF amplifiers where increasing junction capacitance’s with decreasing supply voltage caused a much larger reduction in bandwidth. To compensate for the remaining effect, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing And Printed Circuit Board Layout
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below 1/4”. The power supply pins must be well bypassed to ensure stability. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should have low inductance for best performance. Use of sockets, particularly for SO packages, should be avoided. Sockets have parasitic inductance and capacitance which will cause peaking and overshoot.

Capacitance at the Inverting Input
Due to the topology of the conventional current feedback amplifiers, stray capacitance at the inverting input will affect their AC and transient performance when operating in the non-inverting configuration. This may cause design, development and production difficulties. The EL2175 has been designed in such a way as to largely ignore such strays. The characteristic curves of gain vs. frequency with varying values of Cin illustrate this effect which produces only a slight increase in peaking with Cin values up to 5 pF with almost no change in 3 dB bandwidth.

In the inverting gain mode, added capacitance at the inverting input has almost no effect at all. This is because the inverting input is now a virtual ground and the stray capacitance is not therefore “seen” by the amplifier.

Feedback Resistor Values
The EL2175 has been designed and specified with RF = 750Ω for AV = +2. This value of feedback resistor yields an extremely flat frequency response with little or no peaking out to 120 MHz. As is the case with all CMF amplifiers, wider bandwidth, at the expense of peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause roll-off to occur at lower frequency. This dependence of bandwidth on feedback resistance value is not as pronounced with the EL2175 at low non-inverting gains as with other CMF amplifiers. However, it is at all other gain conditions. For example, the 3 dB bandwidth of the EL2175 connected for AV = −1 and RF = 750Ω is about 65 MHz. If RF is reduced to 560Ω, the bandwidth increases to about 88 MHz. See “Typical Performance Curves” section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistor, supply voltages and temperatures.

Bandwidth vs Temperature
The supply currents of many amplifiers and consequently their 3 dB bandwidths drop off significantly with increasing temperature. The EL2175 was designed to have nearly constant supply current over temperature resulting in a device with much less bandwidth vs. temperature sensitivity. With VS = +15V and AV = +2, the bandwidth only varies from 123 MHz to 96 MHz over the entire die temperature range of 0°C < T < 150°C.
Applications Information — Contd.

Supply Voltage Range
The EL2175 has been designed to operate comfortably with supply voltages from ±5V to ±15V. AC characterization has been conducted down to supply voltages of ±3.5V. However, this low value will not allow the part to power up and function properly at the lowest portion of the part's operating temperature range (-40°C to +85°C). In general, bandwidth, slew rate and video characteristics will tend to improve with increasing supply voltages.

If a single supply is desired, values from +9V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the input common mode range of the EL2175.

Settling Characteristics
The EL2175 offers superb settling characteristics to 0.1%, typically 50 ns operating in inverting mode. The inverting 0.01% settling time is about 90 ns. The EL2175 is not slew rate limited, therefore step size up to ±10V gives approximately the same settling time. The high 30 MΩ transimpedance gain and low input referred offsets of the EL2175 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

The non-inverting (AV = +1) 0.1% settling time is about 70 ns. As can be seen from the Long Term Settling Error graph, for AV = +1, there is approximately a 0.04% residual which tails away to 0.01% in about 900 ns. This is a thermal settling error caused by a power dissipation change in the input stage devices (before and after the voltage step). All other CMF amplifiers exhibit 0.01% thermal settling tails of several tens of microseconds under the same conditions. The input stage of the EL2175 has been designed to greatly reduce this effect. For AV = −1, because the inverting input is then a virtual ground, this tail does not appear even in conventional CMF amplifiers since the input stage does not experience the large voltage change that it does in non-inverting mode.

Distortion Performance
The distortion performance of all high frequency amplifiers degrade with increasing frequency. The EL2175 is no exception. However, due to its high transimpedance, it's distortion performance at a given frequency can be 10–14 dB better than other high speed amplifiers available.

Power Dissipation
The EL2175 combines both high speed and large output drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature and loading conditions. To ensure that the EL2175 remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to:

$$ P_{D_{MAX}} = \frac{(T_{J_{MAX}} - T_{A_{MAX}})}{\theta_{JA}} $$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power dissipated in the IC due to the load, or:

$$ P_{D_{MAX}} = N \times (2 \times V_S \times I_S + (V_S - V_{OUT}) \times V_{OUT} / R_L) $$

where N is the number of amplifiers per package, and IS is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term when the output is driving a load. That is to say, due to the class AB nature of the output stage, the output driver current is now included in the second term.) In general, an amplifier's AC performance degrades at higher temperatures and lower supply current. Unlike some amplifiers, the EL2175 and many other Elantec amplifiers maintain almost constant supply current over temperature so that the AC performance is not degraded as much at the upper end of the operating temperature range.

The EL2175 consumes typically 8.5 mA and a maximum of 10 mA. The worst case power in an amplifier operating from split supplies with a grounded load occurs when the output is between ground and half of one of it's supplies or, if it can't go that far due to drive limitations, at it's
Applications Information — Contd.

maximum value. If we assume that the EL2175 is used for double terminate video cable driving applications \((R_L = 150\Omega)\), and \(A_V = +2\), then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two \(P_{D_{MAX}}\) equations equal to each other, and solve for \(V_S\), we get a family of curves for various package options according to:

\[
V_S = \frac{R_L \times (T_{IMAX} - T_{AMAX}) / N \times \theta_{JA} + (V_{OUT}) \times (V_{OUT})}{(2 \times I_S \times R_L) + (V_{OUT})}
\]

The following curve shows supply voltage \(\pm V_S\) vs. temperature for the EL2175's two packages, assuming \(A_V = +2\), \(R_L = 150\Omega\), and \(V_{OUT}\) (peak) = 2V. The curves include the worst case supply specification \((I_S = 10 \text{ mA})\)

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the device.

Output Current Drive

The EL2175 does not have output short circuit protection. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2175 to survive a continuous short.

Driving Cables And Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For these applications, the back termination series resistor will decouple the EL2175 from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. The EL2175 has particularly high capacitive load tolerance and can drive a 50 pF load with only 3 dB of peaking and a 100 pF load with only 4 dB of peaking and without any instability. If higher capacitive loads must be driven or if little or no peaking is required, an additional small value \((5\Omega - 50\Omega)\) resistor can be placed in series with the output. The gain resistor, \(R_G\), can be chosen to make up for the gain loss created by this additional series resistance at the output.
Features
- Single (EL2176C) and dual (EL2276C) topologies
- 1 mA supply current (per amplifier)
- 70 MHz – 3 dB bandwidth
- Low cost
- Fast disable
- Powers down to 0 mA
- Single- and dual-supply operation down to ± 1.5V
- 0.15%/0.15° diff. gain/diff. phase into 150Ω
- 800V/μs slew rate
- Large output drive current: 100 mA (EL2176C) 55 mA (EL2276C)
- Also available without disable in single (EL2170C), dual (EL2270C) and quad (EL2470C)
- Higher speed EL2180C/EL2186C family also available (3 mA/250 MHz) in single, dual and quad

Applications
- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

General Description
The EL2176C/EL2276C are single/dual current-feedback operational amplifiers which achieve a -3 dB bandwidth of 70 MHz at a gain of +1 while consuming only 1 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from ±3V to +12V. The EL2176C/EL2276C also include a disable/power-down feature which reduces current consumption to 0 mA while placing the amplifier output in a high impedance state. In spite of its low supply current, the EL2276C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2176C can output 100 mA with similar output swings. These attributes make the EL2176C/EL2276C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For Single, Dual and Quad applications without disable, consider the EL2170C (8-Pin Single), EL2270C (8-Pin Dual) or EL2470C (14-Pin Quad). For higher bandwidth applications where low power is still a concern, consider the EL2180C/EL2186C family which also comes in similar Single, Dual and Quad configurations. The EL2180C/EL2186C family provides a -3 dB bandwidth of 250 MHz while consuming 3 mA of supply current per amplifier.

Connection Diagrams

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
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<tbody>
<tr>
<td>EL2176CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2176CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2276CN</td>
<td>-40°C to +85°C</td>
<td>14-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2276CS</td>
<td>-40°C to +85°C</td>
<td>14-Pin SOIC</td>
<td>MDP0027</td>
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Manufactured under U.S. Patent No. 5,352,989, 5,351,012, 5,418,495
## Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
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<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between (V_{S+}) and (V_{S-})</td>
<td>(+12.6V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>(V_{S-} \text{ to } V_{S+})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>(\pm 6V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current into +IN or -IN</td>
<td>(\pm 7.5) mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Power Dissipation</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>(-40^\circ C \text{ to } +85^\circ C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

## DC Electrical Characteristics

\(V_S = \pm 5V, R_L = 150\Omega, \text{ENABLE} = 0V, T_A = 25^\circ C\) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td></td>
<td>2.5</td>
<td></td>
<td>15</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(TCV_{OS})</td>
<td>Average Input Offset Voltage Drift</td>
<td>Measured from (T_{MIN}) to (T_{MAX})</td>
<td>5</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu V/^\circ C)</td>
</tr>
<tr>
<td>(dV_{OS})</td>
<td>(V_{OS}) Matching</td>
<td>(EL2276C)</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>mV</td>
</tr>
<tr>
<td>(+I_{IN})</td>
<td>+ Input Current</td>
<td></td>
<td>0.5</td>
<td></td>
<td>5</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(d+I_{IN})</td>
<td>+ (I_{IN}) Matching</td>
<td>(EL2276C)</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>nA</td>
</tr>
<tr>
<td>(-I_{IN})</td>
<td>- Input Current</td>
<td></td>
<td>4</td>
<td></td>
<td>15</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(d-I_{IN})</td>
<td>- (I_{IN}) Matching</td>
<td>(EL2276C)</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(CMRR)</td>
<td>Common Mode Rejection Ratio</td>
<td>(V_{CM} = \pm 3.5) V</td>
<td>45</td>
<td></td>
<td>50</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(-ICMR)</td>
<td>- Input Current Common Mode Rejection</td>
<td>(V_{CM} = \pm 3.5) V</td>
<td>4</td>
<td></td>
<td>10</td>
<td>I</td>
<td>(\mu A/V)</td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td>(V_S) is moved from (\pm 4V) to (\pm 6V)</td>
<td>60</td>
<td></td>
<td>70</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(-IPS)</td>
<td>- Input Current Power Supply Rejection</td>
<td>(V_S) is moved from (\pm 4V) to (\pm 6V)</td>
<td>0.5</td>
<td></td>
<td>5</td>
<td>I</td>
<td>(\mu A/V)</td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Transimpedance</td>
<td>(V_{OUT} = \pm 2.5V)</td>
<td>150</td>
<td></td>
<td>400</td>
<td>I</td>
<td>k\Omega</td>
</tr>
<tr>
<td>(+R_{IN})</td>
<td>+ Input Resistance</td>
<td>(V_{CM} = \pm 3.5V)</td>
<td>1</td>
<td></td>
<td>4</td>
<td>I</td>
<td>M\Omega</td>
</tr>
<tr>
<td>(+C_{IN})</td>
<td>+ Input Capacitance</td>
<td></td>
<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td>(CMIR)</td>
<td>Common Mode Input Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
## DC Electrical Characteristics — Contd.

$V_S = \pm 5V, R_L = 150\Omega, \text{ENABLE} = 0V, T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing</td>
<td>$V_S = \pm 5$</td>
<td>±3.5</td>
<td>±4.0</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = +5$ Single-Supply, High</td>
<td>4.0</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = +5$ Single-Supply, Low</td>
<td>0.3</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_O$</td>
<td>Output Current</td>
<td>$EL2176C$ only</td>
<td>80</td>
<td>100</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$EL2276C$ only, per Amplifier</td>
<td>50</td>
<td>55</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>ENABLE = 2.0V, per Amplifier</td>
<td>1</td>
<td>2</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{S(DI)}$</td>
<td>Supply Current (Disabled)</td>
<td>ENABLE = 4.5V</td>
<td>0</td>
<td>20</td>
<td>I</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$C_{OUT(DI)}$</td>
<td>Output Capacitance (Disabled)</td>
<td>ENABLE = 4.5V</td>
<td>4.4</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$R_{EN}$</td>
<td>Enable Pin Input Resistance</td>
<td>Measured at ENABLE = 2.0V, 4.5V</td>
<td>45</td>
<td>85</td>
<td>I</td>
<td>k$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>Measured at ENABLE, ENABLE = 4.5V</td>
<td>-0.04</td>
<td></td>
<td>V</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>Measured at ENABLE, ENABLE = 0V</td>
<td>-53</td>
<td></td>
<td>V</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$V_{DIS}$</td>
<td>Minimum Voltage at ENABLE to Disable</td>
<td></td>
<td>4.5</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{EN}$</td>
<td>Maximum Voltage at ENABLE to Enable</td>
<td></td>
<td>2.0</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

## AC Electrical Characteristics

$V_S = \pm 5V, R_P = R_G = 1.0 \, k\Omega, R_L = 150\Omega, \text{ENABLE} = 0V, T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3 dB BW</td>
<td>-3 dB Bandwidth</td>
<td>$A_V = +1$</td>
<td>70</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>-3 dB BW</td>
<td>-3 dB Bandwidth</td>
<td>$A_V = +2$</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>$V_{OUT} = \pm 2.5V, A_V = +2$</td>
<td>400</td>
<td>800</td>
<td></td>
<td>IV</td>
<td>V/$\mu$A</td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Rise and Fall Time</td>
<td>$V_{OUT} = \pm 500$ mV</td>
<td>4.5</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>Propagation Delay</td>
<td>$V_{OUT} = \pm 500$ mV</td>
<td>4.5</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>$V_{OUT} = \pm 500$ mV</td>
<td>3.0</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>ts</td>
<td>0.1% Settling</td>
<td>$V_{OUT} = \pm 2.5V, A_V = -1$</td>
<td>40</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>$A_Y = +2, R_L = 150\Omega$ (Note 1)</td>
<td>0.15</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase</td>
<td>$A_Y = +2, R_L = 150\Omega$ (Note 1)</td>
<td>0.15</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>$A_Y = +1, R_L = 500\Omega$ (Note 1)</td>
<td>0.02</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase</td>
<td>$A_Y = +1, R_L = 500\Omega$ (Note 1)</td>
<td>0.01</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>$t_{ON}$</td>
<td>Turn-On Time</td>
<td>$A_Y = +2, V_{IN} = +1V, R_L = 150\Omega$ (Note 2)</td>
<td>40</td>
<td>100</td>
<td></td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OFF}$</td>
<td>Turn-Off Time</td>
<td>$A_Y = +2, V_{IN} = +1V, R_L = 150\Omega$ (Note 2)</td>
<td>1500</td>
<td>2000</td>
<td></td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>CS</td>
<td>Channel Separation</td>
<td>$EL2276C$ only, $f = 5$ MHz</td>
<td>85</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
</tbody>
</table>

Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mVp-p, $f = 3.58$ MHz.

Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.
**EL2176C/EL2276C**

70 MHz/1 mA Current Mode Feedback Amp w/Disable

Test Circuit (per Amplifier)

![Test Circuit Diagram](image)

Simplified Schematic (per Amplifier)

![Simplified Schematic Diagram](image)
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

Frequency Response for Various Rp and Rg

Frequency Response for Various RL and CL

Transimpedance (R0L)

PSRR and CMRR

Frequency Response for Various Cin
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency

2nd and 3rd Harmonic Distortion vs Frequency

Output Voltage vs Frequency

-3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains

-3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains

Output Voltage Swing vs Supply Voltage

Supply Current vs Supply Voltage

Common-Mode Input Range vs Supply Voltage

Slew Rate vs Supply Voltage
Typical Performance Curves — Contd.

- **Input Bias Current vs Die Temperature**
  ![Image](image1)

- **Short-Circuit Current vs Die Temperature**
  ![Image](image2)

- **Transimpedance (\(R_{OL}\)) vs Die Temperature**
  ![Image](image3)

- **-3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains**
  ![Image](image4)

- **-3 dB Bandwidth and Peaking vs Die Temperature for Various Inverting Gains**
  ![Image](image5)

- **Input Offset Voltage vs Die Temperature**
  ![Image](image6)

- **Supply Current vs Die Temperature**
  ![Image](image7)

- **Input Voltage Range vs Die Temperature**
  ![Image](image8)

- **Slew Rate vs Die Temperature**
  ![Image](image9)
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz/AV = +2

Differential Gain and Phase vs DC Input Offset at 3.58 MHz/AV = +1

Setting Time vs Settling Accuracy

Small-Signal Step Response

Large-Signal Step Response

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature

8-Lead SO Maximum Power Dissipation vs Ambient Temperature
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature

Channel Separation
vs Frequency (EL2275)
Applications Information

Product Description
The EL2176C/EL2276C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 70 MHz, a low supply current of 1 mA per amplifier and the ability to disable to 0 mA. Both products also feature high output current drive. The EL2176C can output 100 mA, while the EL2276C can output 55 mA per amplifier. The EL2176C/EL2276C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2176C/EL2276C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2176C/EL2276C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single, Dual and Quad applications without disable, consider the EL2170C (8-Pin Single), EL2270C (8-Pin Dual) and EL2470C (14-Pin Quad). If more AC performance is required, refer to the EL2180C/EL2186C family which provides Singles, Duals, and Quads with 250 MHz of bandwidth while consuming 3 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down
The EL2176C/EL2276C amplifiers can be disabled, placing their output in a high-impedance state. When disabled, each amplifier’s supply current is reduced to 0 mA. Each EL2176C/EL2276C amplifier is disabled when its ENABLE pin is floating or pulled up to within 0.5V of the positive supply. Similarly, each amplifier is enabled by pulling its ENABLE pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2176C/EL2276C amplifier will be enabled when ENABLE is at 2V or less, and disabled when ENABLE is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2176C/EL2276C to be enabled by tying ENABLE to ground, even in +3V single-supply applications. The ENABLE pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at ENABLE. For example, with the supply voltages of the EL2176C at ±5V, if ENABLE is tied to −5V (rather than ground) the supply current will increase about 15% to 1.15 mA.

Capacitance at the Inverting Input
Any manufacturer’s high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feed-
Applications Information — Contd.

back and gain resistors further exacerbates the problem by further lowering the pole frequency.

The EL2176C/EL2276C have been specially designed to reduce power dissipation in the feedback network by using large 1.0 kΩ feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2176C/EL2276C remain very stable. For less experienced users, this feature makes the EL2176C/EL2276C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2176C/EL2276 C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2176C/EL2276C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g., 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various RF and RG, and Frequency Response for Various CIN—.

Feedback Resistor Values

The EL2176C/EL2276C have been designed and specified at gains of +1 and +2 with RF = 1.0 kΩ. This value of feedback resistor gives 70 MHz of −3 dB bandwidth at AV = +1 with about 1.5 dB of peaking, and 60 MHz of −3 dB bandwidth at AV = +2 with about 0.5 dB of peaking. Since the EL2176C/EL2276C are current-feedback amplifiers, it is also possible to change the value of RF to get more bandwidth. As seen in the curve of Frequency Response for Various RF and RG, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2176C is a current-feedback amplifier, the gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2176C/EL2276C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases.

Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of RF below the specified 1.0 kΩ and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2176C/EL2276C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2176C/EL2276C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2176C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2176C/EL2276C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2176C/EL2276C have an input range which spans from 1V to 4V. The output range of the EL2176C /EL2276C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2176C/EL2276C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically in excess of the
Applications Information — Contd.

entire 1 mA supply current of each EL2176C/EL2276C amplifier. Special circuitry has been incorporated in the EL2176C/EL2276C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.15% and 0.15° while driving 150Ω at a gain of +2.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2176C/EL2276C have dG and dP specifications of 0.01% and 0.02° respectively while driving 500Ω at AV = +1.

Output Drive Capability

In spite of its low 1 mA of supply current, the EL2176C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2276C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2176C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2276C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2176C/EL2276C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (RG) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (RF) to reduce the peaking.

Current Limiting

The EL2176C/EL2276C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2176C/EL2276C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when RL falls below about 25Ω, it is important to calculate the maximum junction temperature (Tj) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2176C/EL2276C to remain in the safe operating area. These parameters are calculated as follows:

\[
T_{J\text{MAX}} = T_{MAX} + (\theta_{JA} \times n \times P_{D\text{MAX}}) \quad [1]
\]

where:

\[
T_{MAX} = \text{Maximum Ambient Temperature}
\]
\[
\theta_{JA} = \text{Thermal Resistance of the Package}
\]
\[
n = \text{Number of Amplifiers in the Package}
\]
\[
P_{D\text{MAX}} = \text{Maximum Power Dissipation of Each Amplifier in the Package.}
\]

\[P_{D\text{MAX}}\] for each amplifier can be calculated as follows:

\[
P_{D\text{MAX}} = (2 \times V_{S} \times I_{S\text{MAX}}) + (V_{S} - V_{\text{OUTMAX}}) \times (V_{\text{OUTMAX}}/R_{L}) \quad [2]
\]

where:

\[
V_{S} = \text{Supply Voltage}
\]
\[
I_{S\text{MAX}} = \text{Maximum Supply Current of 1 Amplifier}
\]
\[
V_{\text{OUTMAX}} = \text{Max. Output Voltage of the Application}
\]
\[
R_{L} = \text{Load Resistance}
\]
Typical Application Circuits

Low Power Multiplexer with Single-Ended TTL Input
Typical Application Circuits — Contd.

Inverting 200 mA Output Current Distribution Amplifier

![Circuit Diagram]

2176-49
Typical Application Circuits — Contd.

Differential Line-Driver/Receiver
Typical Application Circuits — Contd.

Fast-Settling Precision Amplifier

Vin --> 1k --> 1k --> 0.1 μF

\[ +5V \rightarrow IN+ \rightarrow \frac{1}{2} EL2276C \rightarrow OUT \rightarrow +5V \]

\[ IN- \rightarrow VS- \]

\[ -5V \rightarrow ENABLE \rightarrow IN- \rightarrow VS- \rightarrow -5V \rightarrow 0.1 \mu F \]

\[ VIN \rightarrow 1k \rightarrow 1k \rightarrow V_{OUT} \]
**EL2176C/EL2276C Macromodel**

* Revision A, March 1995
* AC characteristics used \( R_f = R_g = 1\,\text{K}\Omega, R_L = 150\,\Omega \)
* Connections:
  - \( + \text{input} \)
  - \( - \text{input} \)
  - \( + \text{Vs} \)
  - \( - \text{Vs} \)
  - \( \text{output} \)

```
.subckt EL2176/el 3 2 7 4 6

\* Input Stage
\* e1 10 0 3 0 1.0
\* vis 10 9 0V
\* h2 9 12 vxx 1.0
\* r1 2 11 165
\* li 11 12 25nH
\* iinp 0 0.5uA
\* iinm 2 0.4uA
\* r12 3 0 4Meg

\* Slew Rate Limiting
\* h1 13 0 vis 600
\* r2 13 14 1K
\* d1 14 0 dclamp
\* d2 0 14 dclamp

\* High Frequency Pole
\* e2 30 0 14 0 0.001666666666666
\* l3 30 17 0.5uH
\* c5 17 0 0.69pF
\* r5 17 0 300

\* Output Stage
\* g1 0 18 17 0 1.0
\* s 18 0 400K
\* cdp 18 0 1.9pF

\* Supply Current
\* ips 7 4 1nA

\* Error Terms
\* ivos 0 23 2mA
\* vxx 23 0 0V
\* e4 24 0 3 0 1.0
\* e5 25 0 7 0 1.0
\* e6 26 0 4 0 1.0
\* r9 24 23 0.316K
\* r10 25 23 3.2K
\* r11 26 23 3.2K

\* Models
\* .model qn npn(is = 5e-15 bf = 200 tf = 0.01nS)
\* .model qp pnp(is = 5e-15 bf = 200 tf = 0.01nS)
\* .model dclamp d(is = 1e-30 ibv = 0.266
  + bv = 1.3v n = 4)
.ends
```
Features
• Single (EL2180C), dual (EL2280C) and quad (EL2480C) topologies
• 3 mA supply current (per amplifier)
• 250 MHz −3 dB bandwidth
• Tiny SOT23-5 Package (EL2180C)
• Low cost
• Single- and dual-supply operation down to ±1.5 V
• 0.05%/0.05° diff. gain/diff. phase into 150Ω
• 1200 V/μs slew rate
• Large output drive current: 100 mA (EL2180C)
  55 mA (EL2280C)
  55 mA (EL2480C)
• Also available with disable in single (EL2186C), dual (EL2286C), and triple (EL2386C)
• Lower power EL2170C/EL2176C family also available (1 mA/70 MHz) in single, dual and quad

Applications
• Low power/battery applications
• HDSL amplifiers
• Video amplifiers
• Cable drivers
• RGB amplifiers
• Test equipment amplifiers
• Current to voltage converters

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2180CN</td>
<td>−40°C to +85°C</td>
<td>8-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2180CS</td>
<td>−40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2180CW</td>
<td>−40°C to +85°C</td>
<td>5-Pin SOT23*</td>
<td>MDP0038</td>
</tr>
<tr>
<td>EL2280CN</td>
<td>−40°C to +85°C</td>
<td>8-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2280CS</td>
<td>−40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2480CN</td>
<td>−40°C to +85°C</td>
<td>14-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2480CS</td>
<td>−40°C to +85°C</td>
<td>14-Pin SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

*See Ordering Information section of databook.

General Description
The EL2180C/EL2280C/EL2480C are single/dual/quad current-feedback operational amplifiers which achieve a −3 dB bandwidth of 250 MHz at a gain of +1 while consuming only 3 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5 V to ±6 V, or from single supplies ranging from +3 V to +12 V. In spite of their low supply current, the EL2480C and the EL2280C can output 55 mA while swinging to ±4 V on ±5 V supplies. The EL2180C can output 100 mA with similar output swings. These attributes make the EL2180C/EL2280C/EL2480C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For applications where board space is extremely critical, the EL2180C is available in the tiny 5-lead SOT23 package, which has a footprint 28% the size of an 8-lead SOIC.

For Single, Dual, and Triple applications with disable, consider the EL2186C (8-Pin Single), EL2286C (14-Pin Dual) or EL2386C (16-Pin Triple). For lower power applications where speed is still a concern, consider the EL2170C/EL2176C family which also comes in similar Single, Dual and Quad configurations. The EL2170C/EL2176C family provides a −3 dB bandwidth of 70 MHz while consuming 1 mA of supply current per amplifier.

Connection Diagrams
### Absolute Maximum Ratings (TA = 25°C)

- Voltage between Vs+ and Vs−: +12.6V
- Common-Mode Input Voltage: Vs− to Vs+
- Differential Input Voltage: ±6V
- Current into +IN or −IN: ±7.5 mA
- Internal Power Dissipation: See Curves
- Operating Ambient Temperature Range: −40°C to +85°C
- Storage Temperature Range: −65°C to +150°C

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Tj = TC = TA.

### Test Level

<table>
<thead>
<tr>
<th>Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at TA = 25°C and QA sample tested at TA = 25°C, TMAX and TMIN per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at TA = 25°C for information purposes only.</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics

- **Conditions:** Vs = ±5V, RL = 150Ω, TA = 25°C unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td></td>
<td>2.5</td>
<td>15</td>
<td>I</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>TCVOS</td>
<td>Average Input Offset Voltage Drift</td>
<td>Measured from TMIN to TMAX</td>
<td>5</td>
<td></td>
<td>V</td>
<td>V</td>
<td>μV/°C</td>
</tr>
<tr>
<td>dVOS</td>
<td>VO(s) Matching</td>
<td>EL2280C, EL2480C only</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>+IIN</td>
<td>+ Input Current</td>
<td></td>
<td>1.5</td>
<td>15</td>
<td>I</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>d+IIN</td>
<td>+ IN Matching</td>
<td>EL2280C, EL2480C only</td>
<td>20</td>
<td></td>
<td>V</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>−IIN</td>
<td>− Input Current</td>
<td></td>
<td>16</td>
<td>40</td>
<td>I</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>d−IIN</td>
<td>− IN Matching</td>
<td>EL2280C, EL2480C only</td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>VCM = ±3.5V</td>
<td>45</td>
<td>50</td>
<td>I</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>−ICMR</td>
<td>− Input Current Common Mode Rejection</td>
<td>VCM = ±3.5V</td>
<td>5</td>
<td>30</td>
<td>I</td>
<td>I</td>
<td>μA/V</td>
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<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>VS is moved from ±4V to ±6V</td>
<td>60</td>
<td>70</td>
<td>I</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>−IPSR</td>
<td>− Input Current Power Supply Rejection</td>
<td>VS is moved from ±4V to ±6V</td>
<td>1</td>
<td>15</td>
<td>I</td>
<td>I</td>
<td>μA/V</td>
</tr>
<tr>
<td>Rol</td>
<td>Transimpedance</td>
<td>VOUT = ±2.5V</td>
<td>120</td>
<td>300</td>
<td>I</td>
<td>I</td>
<td>kΩ</td>
</tr>
<tr>
<td>+RIN</td>
<td>+ Input Resistance</td>
<td>VCM = ±3.5V</td>
<td>0.5</td>
<td>2</td>
<td>I</td>
<td>I</td>
<td>MΩ</td>
</tr>
<tr>
<td>+CIN</td>
<td>+ Input Capacitance</td>
<td></td>
<td>1.2</td>
<td></td>
<td>V</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CMIR</td>
<td>Common Mode Input Range</td>
<td></td>
<td>±3.5</td>
<td>±4.0</td>
<td>I</td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 150\Omega$, $T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing</td>
<td>$V_S = \pm 5$</td>
<td>± 3.5</td>
<td>± 4.0</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = +5$ Single-Supply, High</td>
<td>4.0</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = +5$ Single-Supply, Low</td>
<td>0.3</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_O$</td>
<td>Output Current</td>
<td>EL2180C only</td>
<td>80</td>
<td>100</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL2280C only, per Amplifier</td>
<td>50</td>
<td>55</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL2480C only, per Amplifier</td>
<td>50</td>
<td>55</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>Per Amplifier</td>
<td>3</td>
<td>6</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = R_G = 750\Omega$ for PDIP and SOIC packages, $R_F = R_G = 560\Omega$ for SOT23-5 package, $R_L = 150\Omega$, $T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-3 , dB$ BW</td>
<td>$-3 , dB$ Bandwidth</td>
<td>$A_V = +1$</td>
<td>250</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$-3 , dB$ BW</td>
<td>$-3 , dB$ Bandwidth</td>
<td>$A_V = +2$</td>
<td>180</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>0.1 dB BW</td>
<td>0.1 dB Bandwidth</td>
<td>$A_V = +2$</td>
<td>50</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>$V_{OUT} = \pm 2.5V, A_V = +2$</td>
<td>600</td>
<td>1200</td>
<td>IV</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Rise and Fall Time</td>
<td>$V_{OUT} = \pm 500 , mV$</td>
<td>1.5</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>Propagation Delay</td>
<td>$V_{OUT} = \pm 500 , mV$</td>
<td>1.5</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>$V_{OUT} = \pm 500 , mV$</td>
<td>3.0</td>
<td>V</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_s$</td>
<td>0.1% Settling</td>
<td>$V_{OUT} = \pm 2.5V, A_V = -1$</td>
<td>15</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>$A_V = +2, R_L = 150\Omega$ (Note 1)</td>
<td>0.05</td>
<td>V</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase</td>
<td>$A_V = +2, R_L = 150\Omega$ (Note 1)</td>
<td>0.05</td>
<td>V</td>
<td></td>
<td>*</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain</td>
<td>$A_V = +1, R_L = 500\Omega$ (Note 1)</td>
<td>0.01</td>
<td>V</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase</td>
<td>$A_V = +1, R_L = 500\Omega$ (Note 1)</td>
<td>0.01</td>
<td>V</td>
<td></td>
<td>*</td>
<td></td>
</tr>
<tr>
<td>$C_S$</td>
<td>Channel Separation</td>
<td>EL2280C, EL2480C only, $f = 5 , MHz$</td>
<td>85</td>
<td>V</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mVp-p, $f = 3.58 \, MHz$. 

2-433
Test Circuit (per Amplifier)

Simplified Schematic (per Amplifier)
Typical Performance Curves

Non-Inverting Frequency Response (Gain) (PDIP and SOIC Packages)

Inverting Frequency Response (Gain) (PDIP and SOIC Packages)

Non-Inverting Frequency Response (Phase) (PDIP and SOIC Packages)

Inverting Frequency Response (Phase) (PDIP and SOIC Packages)

Frequency Response for Various $R_p$ and $R_G$ (PDIP and SOIC Packages)

Frequency Response for Various $R_L$ and $R_L$ (PDIP and SOIC Packages)

Frequency Response for Various $C_{IN}$

Transimpedance ($R_{OL}$) vs Frequency

PSRR and CMRR vs Frequency

Frequency Response for Various $C_{IN}$
Typical Performance Curves — Contd.

- Voltage and Current Noise vs Frequency
- 2nd and 3rd Harmonic Distortion vs Frequency
- Output Voltage Swing vs Frequency

-3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains
-3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains

Supply Current vs Supply Voltage

Common-Mode Input Range vs Supply Voltage

Slew Rate vs Supply Voltage
Typical Performance Curves — Contd.

- **Input Bias Current vs Die Temperature**
  
- **Short-Circuit Current vs Die Temperature**
  
- **Transimpedance ($R_{OL}$) vs Die Temperature**

- **-3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains**

- **-3 dB Bandwidth vs Die Temperature for Various Inverting Gains**

- **Input Offset Voltage vs Die Temperature**

- **Supply Current vs Die Temperature**

- **Input Voltage Range vs Die Temperature**

- **Slew Rate vs Die Temperature**
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz

Settling Time vs Settling Accuracy

Small-Signal Step Response

Large-Signal Step Response

5-Lead Plastic SOT23
Maximum Power Dissipation vs Ambient Temperature

8-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

8-Lead SO
Maximum Power Dissipation vs Ambient Temperature

$V_G = \pm 5\, V$  $R_P = R_Q = 750\, \Omega$  $R_L = 150\, \Omega$  $A_V = +2$

$V_G = \pm 5\, V$  $R_P = R_Q = 750\, \Omega$  $R_L = 150\, \Omega$  $A_V = +2$

$T_J \text{ MAX} = 150^\circ C$  $

\theta JA = 95^\circ C/W$

$T_J \text{ MAX} = 150^\circ C$

$\theta JA = 150^\circ C/W$

$\theta JA = 325^\circ C/W$
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

-25 25 75 125 175
TEMPERATURE (°C)

Maximum Power Dissipation

vs Ambient Temperature

T MAX = 150°C
θ JA = 70°C/W

Non-Inverting Frequency Response (Gain)
(SOT23-5 Package)

RL = 150Ω

Ay = +1

Ay = +2

Ay = +5

Ay = +10

Ay = +2

Frequency (Hz)

1M 10M 100M 500M

Magnitude (Normalized) (dB)

Inverting Frequency Response (Gain)
(SOT23-5 Package)

RL = 150Ω

Ay = -1

Ay = -2

Ay = -5

Ay = -10

Frequency (Hz)

1M 10M 100M 500M

Magnitude (Normalized) (dB)

14-Lead SO
Maximum Power Dissipation vs Ambient Temperature

-25 25 75 125 175
TEMPERATURE (°C)

Maximum Power Dissipation

vs Ambient Temperature

T MAX = 110°C/W
θ JA = 70°C/W

Channel Separation vs Frequency

R L = 150Ω

EL2480 A to D and B to C

Frequency (Hz)

1M 10M 100M 1000M

Magnitude (Normalized) (dB)

Frequency Response for Various R F and R G
(SOT23-5 Package)

RL = 150Ω

V S = ±5V

Ay = +2

Ay = +5

Frequency (Hz)

1M 10M 100M 500M

Magnitude (Normalized) (dB)

Frequency Response (Phase)
(SOT23-5 Package)

RL = 150Ω

V S = ±5V

Ay = +2

Ay = -2

Frequency (Hz)

1M 10M 100M 500M

Phase (°)

3480-39

2180-39

2180-40

2180-41

2180-46

2180-49

2180-50

2180-51

2180-52
Applications Information

Product Description
The EL2180C/EL2280C/EL2480C are current-feedback operational amplifiers that offer a wide $-3\,\text{dB}$ bandwidth of 250 MHz and a low supply current of 3 mA per amplifier. All of these products also feature high output current drive. The EL2180C can output 100 mA, while the EL2280C and the EL2480C can output 55 mA per amplifier. The EL2180C/EL2280C/EL2480C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2180C/EL2280C/EL2480C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their $-3\,\text{dB}$ bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2180C/EL2280C/EL2480C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For applications where board space is extremely critical, the EL2180C is available in the tiny 5-lead SOT23 package, which has a footprint 28% the size of an 8-lead SOIC. The EL2180C/EL2280C/EL2480C are each also available in industry standard pinouts in PDIP and SOIC packages.

For Single, Dual and Triple applications with disable, consider the EL2186C (8-Pin Single), EL2286C (14-Pin Dual) and EL2386C (16-Pin Triple). If lower power is required, refer to the EL2170C/EL2176C family which provides Singles, Duals, and Quads with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 µF tantalum capacitor in parallel with a 0.1 µF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input
Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.
Applications Information — Contd.
The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2180C/EL2280C/EL2480C have less bandwidth than expected.

The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various $R_F$ and $R_G$, and Frequency Response for Various $C_{IN}$.

Feedback Resistor Values
The EL2180C/EL2280C/EL2480C have been designed and specified at gains of $+1$ and $+2$ with $R_F = 750\, \Omega$ in PDIP and SOIC packages and $R_F = 560\, \Omega$ in SOT23-5 package. These values of feedback resistors give 250 MHz of $-3\, \text{dB}$ bandwidth at $A_V = +1$ with about 2.5 dB of peaking, and 180 MHz of $-3\, \text{dB}$ bandwidth at $A_V = +2$ with about 0.1 dB of peaking. The SOT23-5 package is characterized with a smaller value of feedback resistor, for a given bandwidth, to compensate for lower parasitics within both the package itself and the printed circuit board where it will be placed. Since the EL2180C/EL2280C/EL2480C are current-feedback amplifiers, it is also possible to change the value of $R_F$ to get more bandwidth. As seen in the curve of Frequency Response For Various $R_F$ and $R_G$, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2180C/EL2280C/EL2480C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2180C/EL2280C/EL2480C to maintain about the same $-3\, \text{dB}$ bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of $R_F$ below the specified $560\, \Omega$ and $750\, \Omega$ and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation
The EL2180C/EL2280C/EL2480C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2180C/EL2280C/EL2480C will operate on dual supplies ranging from $\pm 1.5\, \text{V}$ to $\pm 6\, \text{V}$. With a single-supply, the EL2180C/EL2280C/EL2480C will operate from $+3\, \text{V}$ to $+12\, \text{V}$.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2180C/EL2280C/EL2480C have an input voltage range that extends to within 1V of either supply. So, for example, on a single $+5\, \text{V}$ supply, the EL2180C/EL2280C/EL2480C have an input range which spans from 1V to 4V. The output range of the EL2180C/EL2280C/EL2480C is also quite large, extending to within 1V of the supply rail. On a $\pm 5\, \text{V}$ supply, the output is therefore capable of swinging from $-4\, \text{V}$ to $+4\, \text{V}$. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single $+5\, \text{V}$ supply, output voltage range is about 0.3V to 4V.

Video Performance
For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of $150\, \Omega$, because of the change in output current with DC level. Until the EL2180C/EL2280C/EL2480C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2180C/EL2280C/EL2480C amplifier! Special circuitry has been incorporated in the EL2180C/EL2280C/EL2480C to reduce the variation of output impedance with current output. This results in $dG$ and $dP$ specifications of 0.05% and 0.05° while driving $150\, \Omega$ at a gain of $+2$. 
Applications Information — Contd.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2180C/EL2280C/EL2480C have dG and dP specifications of 0.01% and 0.01° respectively while driving 500Ω at AV = +1.

Output Drive Capability

In spite of its low 3 mA of supply current, the EL2180C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2280C and the EL2480C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2180C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2280C and EL2480C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2180C/EL2280C/EL2480C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (RG) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (RF) to reduce the peaking.

Current Limiting

The EL2180C/EL2280C/EL2480C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2180C/EL2280C/EL2480C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when RL falls below about 25Ω, it is important to calculate the maximum junction temperature (Tjunction) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2180C/EL2280C/EL2480C to remain in the safe operating area. These parameters are calculated as follows:

\[ T_{j_{\text{max}}} = T_{\text{max}} + (\theta_{ja} \cdot n \cdot P_{\text{dmax}}) \]  \[ 1 \]

where:

\[ T_{\text{max}} \] = Maximum Ambient Temperature

\[ \theta_{ja} \] = Thermal Resistance of the Package

\[ n \] = Number of Amplifiers in the Package

\[ P_{\text{dmax}} \] = Maximum Power Dissipation of Each Amplifier in the Package.

\[ P_{\text{dmax}} \] for each amplifier can be calculated as follows:

\[ P_{\text{dmax}} = (2 \cdot V_{s} \cdot I_{\text{sm}}) + (V_{s} - V_{\text{outmax}}) \cdot (V_{\text{outmax}}/R_{L}) \] \[ 2 \]

where:

\[ V_{s} \] = Supply Voltage

\[ I_{\text{sm}} \] = Maximum Supply Current of 1 Amplifier

\[ V_{\text{outmax}} \] = Max. Output Voltage of the Application

\[ R_{L} \] = Load Resistance
Typical Application Circuits

Inverting 200 mA Output Current Distribution Amplifier

Fast-Settling Precision Amplifier
Typical Application Circuits — Contd.

Differential Line-Driver/Receiver
EL2180C/EL2280C/EL2480C Macromodel

* EL2180 Macromodel
* Revision A, March 1995
* AC characteristics used: \( R_f = R_g = 750 \text{ ohms} \)
* Connections:
  * \( + \text{input} \)
  * \( + \text{Vs} \)
  * \( - \text{Vs} \)
  * \( \text{output} \)

.subckt EL2180/el 3 2 7 4 6
* Input Stage
* e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 400
l1 11 12 25nH
iimp 3 0 1.5uA
iimm 2 0 3uA
r12 3 0 2Meg
* Slew Rate Limiting
* h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
* High Frequency Pole
* e2 30 0 14 0 0.00166666666666
l3 30 17 150nH
c5 17 0 0.8pF
r5 17 0 165
* Transimpedance Stage
* g1 0 18 17 0 1.0
rol 18 0 450K
cdp 18 0 0.675pF
* Output Stage
* q1 4 18 19 qa
q2 7 18 20 qa
q3 7 19 21 qa
q4 4 20 22 qa
r7 21 6 4
r8 22 6 4
ios1 7 19 1mA
ios2 20 4 1mA
* Supply Current
* ips 7 4 0.2mA
* Error Terms
* ivos 0 23 0.2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 316
r10 25 23 3.2K
r11 26 23 3.2K
* Models
* .model qn npn(is = 5e-15 bf = 200 tf = 0.01nS)
.model qp pnp(is = 5e-15 bf = 200 tf = 0.01nS)
.model dclamp d(is = 1e-30 ibv = 0.266
  + bv = 0.711v n = 4)
.ends
EL2180C/EL2280C/EL2480C Macromodel — Contd.
Features

- Single (EL2186C) and dual (EL2286C) topologies
- 3 mA supply current (per amplifier)
- 250 MHz – 3 dB bandwidth
- Low cost
- Fast disable
- Powers down to 0 mA
- Single- and dual-supply operation down to ±1.5 V
- 0.05%/0.05° diff. gain/diff. phase into 150Ω
- 1200V/μs slew rate
- Large output drive current: 100 mA (EL2186C) 55 mA (EL2286C)
- Also available without disable in single (EL2180C), dual (EL2280C) and quad (EL2480C)
- Lower power EL2170C/EL2176C family also available (1 mA/70 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2186CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2186CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2286CN</td>
<td>-40°C to +85°C</td>
<td>14-Pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2286CS</td>
<td>-40°C to +85°C</td>
<td>14-Pin SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

General Description

The EL2186C/EL2286C are single/dual current-feedback operational amplifiers which achieve a –3 dB bandwidth of 250 MHz at a gain of +1 while consuming only 3 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5 V to ±6 V, or from single supplies ranging from +3 V to +12 V. The EL2186C/EL2286C also include a disable/power-down feature which reduces current consumption to 0 mA while placing the amplifier output in a high impedance state. In spite of its low supply current, the EL2286C can output 55 mA while swinging to ±4 V on ±5 V supplies. The EL2186C can output 100 mA with similar output swings. These attributes make the EL2186C/EL2286C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For Single, Dual and Quad applications without disable, consider the EL2180C (8-Pin Single), EL2280C (8-Pin Dual) or EL2480C (14-Pin Quad). For lower power applications where speed is still a concern, consider the EL2170C/EL2176C family which also comes in similar Single, Dual and Quad configurations. The EL2170C/EL2176C family provides a –3 dB bandwidth of 70 MHz while consuming 1 mA of supply current per amplifier.

Connection Diagrams
EL2186C/EL2286C
250 MHz/3 mA Current Mode Feedback Amp w/Disable

Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between ( V_S^+ ) and ( V_S^- )</td>
<td>+12.6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Common-Mode Input Voltage ( V_S^- ) to ( V_S^+ )</td>
<td>±6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±7.5 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current into +IN or -IN</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Ambient</td>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>−40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

DC Electrical Characteristics
\( V_S = \pm 5V, R_L = 150\Omega, ENABLE = 0V, T_A = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td></td>
<td>2.5</td>
<td></td>
<td>15</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Average Input Offset Voltage Drift</td>
<td>Measured from ( T_{MIN} ) to ( T_{MAX} )</td>
<td>5</td>
<td></td>
<td>V</td>
<td>V</td>
<td>\mu V/°C</td>
</tr>
<tr>
<td>( dV_{OS} )</td>
<td>( V_{OS} ) Matching</td>
<td>EL2286C only</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( +I_{IN} )</td>
<td>+ Input Current</td>
<td></td>
<td>1.5</td>
<td>15</td>
<td>1</td>
<td>I</td>
<td>\mu A</td>
</tr>
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<td>( d+I_{IN} )</td>
<td>+ ( I_{IN} ) Matching</td>
<td>EL2286C only</td>
<td>20</td>
<td></td>
<td>V</td>
<td></td>
<td>\mu A</td>
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<td>( -I_{IN} )</td>
<td>- Input Current</td>
<td></td>
<td>16</td>
<td>40</td>
<td></td>
<td>I</td>
<td>\mu A</td>
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<td>( d-I_{IN} )</td>
<td>- ( I_{IN} ) Matching</td>
<td>EL2286C only</td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
<td>\mu A</td>
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<tr>
<td>( CMRR )</td>
<td>Common Mode Rejection Ratio</td>
<td>( V_{CM} = \pm 3.5V )</td>
<td>45</td>
<td>50</td>
<td>1</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>( -ICMR )</td>
<td>- Input Current Common Mode Rejection</td>
<td>( V_{CM} = \pm 3.5V )</td>
<td>5</td>
<td>30</td>
<td>1</td>
<td>I</td>
<td>\mu A/V</td>
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<tr>
<td>( PSRR )</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S ) is moved from ( \pm 4V ) to ( \pm 6V )</td>
<td>60</td>
<td>70</td>
<td>1</td>
<td>I</td>
<td>dB</td>
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<tr>
<td>( -IPSRR )</td>
<td>- Input Current Power Supply Rejection</td>
<td>( V_S ) is moved from ( \pm 4V ) to ( \pm 6V )</td>
<td>1</td>
<td>15</td>
<td>1</td>
<td>I</td>
<td>\mu A/V</td>
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<tr>
<td>( R_{OL} )</td>
<td>Transimpedance</td>
<td>( V_{OUT} = \pm 2.5V )</td>
<td>120</td>
<td>300</td>
<td>1</td>
<td>I</td>
<td>k\Omega</td>
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<tr>
<td>( +R_{IN} )</td>
<td>+ Input Resistance</td>
<td>( V_{CM} = \pm 3.5V )</td>
<td>0.5</td>
<td>2</td>
<td>I</td>
<td>M\Omega</td>
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<tr>
<td>( +C_{IN} )</td>
<td>+ Input Capacitance</td>
<td></td>
<td>1.2</td>
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<td>V</td>
<td></td>
<td>pF</td>
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<td>( CMIR )</td>
<td>Common Mode Input Range</td>
<td></td>
<td>±3.5</td>
<td>±4.0</td>
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<td>I</td>
<td>V</td>
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**DC Electrical Characteristics — Contd.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>( V_O )</td>
<td>Output Voltage Swing</td>
<td>( V_S = \pm 5 )</td>
<td>±3.5</td>
<td>±4.0</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5 ) Single-Supply, High</td>
<td>4.0</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5 ) Single-Supply, Low</td>
<td>0.3</td>
<td>V</td>
<td>V</td>
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<td>( I_O )</td>
<td>Output Current</td>
<td>( \text{EL2186C only} )</td>
<td>80</td>
<td>100</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EL2286C only, per Amplifier} )</td>
<td>50</td>
<td>55</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>( \text{ENABLE} = 2.0V, \text{per Amplifier} )</td>
<td>3</td>
<td>6</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{S(DIS)} )</td>
<td>Supply Current (Disabled)</td>
<td>( \text{ENABLE} = 4.5V )</td>
<td>0</td>
<td>50</td>
<td>I</td>
<td>( \mu A )</td>
<td></td>
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<tr>
<td>( C_{OUT(DIS)} )</td>
<td>Output Capacitance (Disabled)</td>
<td>( \text{ENABLE} = 4.5V )</td>
<td>4.4</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
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<tr>
<td>( R_{EN} )</td>
<td>Enable Pin Input Resistance</td>
<td>Measured at ( \text{ENABLE} = 2.0V, 4.5V )</td>
<td>45</td>
<td>85</td>
<td>I</td>
<td>k\Omega</td>
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<tr>
<td>( I_{IH} )</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>Measured at ( \text{ENABLE, ENABLE} = 4.5V )</td>
<td>-0.04</td>
<td></td>
<td>V</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>Measured at ( \text{ENABLE, ENABLE} = 0V )</td>
<td>-53</td>
<td></td>
<td>V</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( V_{DIS} )</td>
<td>Minimum Voltage at ( \text{ENABLE} ) to Disable</td>
<td></td>
<td>4.5</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{EN} )</td>
<td>Maximum Voltage at ( \text{ENABLE} ) to Enable</td>
<td></td>
<td>2.0</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**AC Electrical Characteristics**

\( V_S = \pm 5V, R_F = R_G = 750\Omega, R_L = 150\Omega, \text{ENABLE} = 0V, T_A = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>(-3) dB BW</td>
<td>(-3) dB Bandwidth</td>
<td>( A_V = +1 )</td>
<td>250</td>
<td></td>
<td>V</td>
<td>MHz</td>
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<td>(-3) dB BW</td>
<td>(-3) dB Bandwidth</td>
<td>( A_V = +2 )</td>
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<td>(0.1) dB BW</td>
<td>(0.1) dB Bandwidth</td>
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<td></td>
<td>V</td>
<td>MHz</td>
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<tr>
<td>( S_R )</td>
<td>Slew Rate</td>
<td>( V_{OUT} = \pm 2.5V, A_V = +2 )</td>
<td>600</td>
<td>1200</td>
<td>IV</td>
<td>V/( \mu s )</td>
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<tr>
<td>( t_r, t_f )</td>
<td>Rise and Fall Time</td>
<td>( V_{OUT} = \pm 500mV )</td>
<td>1.5</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_p_d )</td>
<td>Propagation Delay</td>
<td>( V_{OUT} = \pm 500mV )</td>
<td>1.5</td>
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<td>V</td>
<td>ns</td>
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<tr>
<td>( O_S )</td>
<td>Overshoot</td>
<td>( V_{OUT} = \pm 500mV )</td>
<td>3.0</td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
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<tr>
<td>( t_s )</td>
<td>0.1% Settling</td>
<td>( V_{OUT} = \pm 2.5V, A_V = -1 )</td>
<td>15</td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( d_G )</td>
<td>Differential Gain</td>
<td>( A_V = +2, R_L = 150\Omega ) (Note 1)</td>
<td>0.05</td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( d_P )</td>
<td>Differential Phase</td>
<td>( A_V = +2, R_L = 150\Omega ) (Note 1)</td>
<td>0.05</td>
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<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( d_G )</td>
<td>Differential Gain</td>
<td>( A_V = +1, R_L = 500\Omega ) (Note 1)</td>
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<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( d_P )</td>
<td>Differential Phase</td>
<td>( A_V = +1, R_L = 500\Omega ) (Note 1)</td>
<td>0.01</td>
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<td>V</td>
<td>%</td>
<td></td>
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<td>( t_{ON} )</td>
<td>Turn-On Time</td>
<td>( A_V = +2, V_{IN} = +1V, R_L = 150\Omega ) (Note 2)</td>
<td>40</td>
<td>100</td>
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<td>ns</td>
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<td>( t_{OFF} )</td>
<td>Turn-Off Time</td>
<td>( A_V = +2, V_{IN} = +1V, R_L = 150\Omega ) (Note 2)</td>
<td>1500</td>
<td>2000</td>
<td>I</td>
<td>ns</td>
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<td>( C_S )</td>
<td>Channel Separation</td>
<td>( \text{EL2286C only, } f = 5MHz )</td>
<td>85</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
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</table>

Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mVp_p, \( f = 3.58 \) MHz.
Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.
**Test Circuit (per Amplifier)**

![Test Circuit Diagram](image)

**Simplified Schematic (per Amplifier)**

![Simplified Schematic Diagram](image)
Typical Performance Curves

Non-Inverting Frequency Response (Gain)

Non-Inverting Frequency Response (Phase)

Frequency Response for Various Rp and RG

Inverting Frequency Response (Gain)

Inverting Frequency Response (Phase)

Frequency Response for Various RL and RL

Transimpedance (R_LO) vs Frequency

PSRR and CMRR vs Frequency

Frequency Response for Various C_{IN-}
Typical Performance Curves — Contd.

- Voltage and Current Noise vs Frequency
- 2nd and 3rd Harmonic Distortion vs Frequency
- Output Voltage Swing vs Frequency
- -3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains
- -3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains
- Output Voltage Swing vs Supply Voltage
- Supply Current vs Supply Voltage
- Common-Mode Input Range vs Supply Voltage
- Slew Rate vs Supply Voltage
Typical Performance Curves — Contd.

- **Input Bias Current vs Die Temperature**
- **Short-Circuit Current vs Die Temperature**
- **Transimpedance ($R_{OL}$) vs Die Temperature**
- **-3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains**
- **-3 dB Bandwidth vs Die Temperature for Various Inverting Gains**
- **Input Offset Voltage vs Die Temperature**
- **Supply Current vs Die Temperature**
- **Input Voltage Range vs Die Temperature**
- **Slew Rate vs Die Temperature**
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz

Settling Time vs Settling Accuracy

Small-Signal Step Response

Large-Signal Step Response

8-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

8-Lead SO
Maximum Power Dissipation vs Ambient Temperature
Typical Performance Curves — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature

Channel Separation
vs Frequency (EL2286)

- Power Dissipation (W)
- Temperature (°C)
- T_J MAX = 150°C
- θ_JA = 70°C/W

- Channel Separation (dB)
- Frequency (Hz)
- θ_JA = 110°C/W

2186-39
2186-40
2186-41
Applications Information

Product Description
The EL2186C/EL2286C are current-feedback operational amplifiers that offer a wide –3 dB bandwidth of 250 MHz, a low supply current of 3 mA per amplifier and the ability to disable to 0 mA. Both products also feature high output current drive. The EL2186C can output 100 mA, while the EL2286C can output 55 mA per amplifier. The EL2186C/EL2286C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2186C/EL2286C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their –3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2186C/EL2286C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single, Dual and Quad applications without disable, consider the EL2180C (8-Pin Single), EL2280C (8-Pin Dual) and EL2480C (14-Pin Quad). If lower power is required, refer to the EL2170C/EL2176C family which provides Singles, Duals, and Quads with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down
The EL2186C/EL2286C amplifiers can be disabled, placing their output in a high-impedance state. When disabled, each amplifier’s supply current is reduced to 0 mA. Each EL2186C/EL2286C amplifier is disabled when its ENABLE pin is floating or pulled up to within 0.5V of the positive supply. Similarly, each amplifier is enabled by pulling its ENABLE pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2186C/EL2286C amplifier will be enabled when ENABLE is at 2V or less, and disabled when ENABLE is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2186C/EL2286C to be enabled by tying ENABLE to ground, even in ±3V single-supply applications. The ENABLE pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at ENABLE. For example, with the supply voltages of the EL2186C at ±5V, if ENABLE is tied to –5V (rather than ground) the supply current will increase about 15% to 3.45 mA.

Capacitance at the Inverting Input
Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the...
Applications Information — Contd.

The EL2186C/EL2286C have been specially designed to reduce power dissipation in the feedback network by using large value feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2186C/EL2286C remain very stable. For less experienced users, this feature makes the EL2186C/EL2286C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2186C/EL2286C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2186C/EL2286C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various RF and RG, and Frequency Response for Various CIN-.

Feedback Resistor Values

The EL2186C/EL2286C have been designed and specified at gains of +1 and +2 with RF = 750Ω. This value of feedback resistor gives 250 MHz of −3 dB bandwidth at AV = +1 with about 2.5 dB of peaking, and 180 MHz of −3 dB bandwidth at AV = +2 with about 0.1 dB of peaking. Since the EL2186C/EL2286C are current-feedback amplifiers, it is also possible to change the value of RF to get more bandwidth. As seen in the curve of Frequency Response For Various RF and RG, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2186C/EL2286C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2186C/EL2286C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases.

Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of RF below the specified 750Ω and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2186C/EL2286C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2186C/EL2286C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2176C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2186C/EL2286C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2186C/EL2286C have an input range which spans from 1V to 4V. The output range of the EL2186C/EL2286C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2186C/EL2286C, good Differ-
Applications Information — Contd.

Potential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2186C/EL2286C amplifier! Special circuitry has been incorporated in the EL2186C/EL2286C to reduce the variation of output impedance with current output. This results in \(dG\) and \(dP\) specifications of 0.05% and 0.05° respectively while driving 150Ω at a gain of +2.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2186C/EL2286C have \(dG\) and \(dP\) specifications of 0.01% and 0.01° respectively while driving 50Ω at a gain of \(\pm 1\).

Output Drive Capability

In spite of its low 3 mA of supply current, the EL2186C is capable of providing a minimum of \(\pm 80\) mA of output current. Similarly, each amplifier of the EL2286C is capable of providing a minimum of \(\pm 50\) mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum \(\pm 80\) mA of output drive, the EL2186C is capable of driving 50Ω loads to \(\pm 4\) V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the \(\pm 50\) mA minimum output drive of each EL2286C amplifier allows swings of \(\pm 2.5\) V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2186C/EL2286C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (\(R_G\)) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (\(R_F\)) to reduce the peaking.

Current Limiting

The EL2186C/EL2286C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2186C/EL2286C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when \(R_L\) falls below about 25Ω, it is important to calculate the maximum junction temperature (\(T_{J\text{max}}\)) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2186C/EL2286C to remain in the safe operating area. These parameters are calculated as follows:

\[
T_{J\text{max}} = T_{\text{MAX}} + (\theta_{JA} \times n \times P_{D\text{MAX}}) \quad [1]
\]

where:

- \(T_{\text{MAX}}\) = Maximum Ambient Temperature
- \(\theta_{JA}\) = Thermal Resistance of the Package
- \(n\) = Number of Amplifiers in the Package
- \(P_{D\text{MAX}}\) = Maximum Power Dissipation of Each Amplifier in the Package.

\(P_{D\text{MAX}}\) for each amplifier can be calculated as follows:

\[
P_{D\text{MAX}} = (2 \times V_S \times I_{\text{SMAX}}) + (V_S - V_{\text{OUTMAX}}) \times (V_{\text{OUTMAX}}/R_L) \quad [2]
\]

where:

- \(V_S\) = Supply Voltage
- \(I_{\text{SMAX}}\) = Maximum Supply Current of 1 Amplifier
- \(V_{\text{OUTMAX}}\) = Max. Output Voltage of the Application
- \(R_L\) = Load Resistance
Typical Application Circuits

Low Power Multiplexer with Single-Ended TTL Input

+5V

\(V_{IN_A}\)

10k

10k

\(RGA\)

\(RFA\)

ABSELECT

\(2N2222\)

1k

470

\(1N4001\)

\(+5V\)

\(V_{OUT}\)

\(0.1 \mu F\)

\(\text{EL2186C or EL2286C}\)

\(\text{IN+}\)

\(\text{IN-}\)

\(\text{ENABLE}\)

\(\text{OUT}\)

\(\text{VS+}\)

\(\text{VS-}\)

\(-5V\)

\(750\)

\(750\)

\(\text{RCA}\)

\(\text{RFB}\)

\(750\)

\(750\)

\(\text{RGB}\)

\(\text{RFB}\)

\(+5V\)

\(1k\)
Typical Application Circuits — Contd.

Inverting 200 mA Output Current Distribution Amplifier

![Typical Application Circuit Diagram]
Typical Application Circuits – Contd.

Differential Line-Driver/Receiver
Typical Application Circuits — Contd.

Fast-Settling Precision Amplifier

[Diagram of a precision amplifier with labels for inputs, outputs, and capacitors.]
EL2186C/EL2286C Macromodel

* EL2186 Macromodel
* Revision A, March 1995
* AC characteristics used: Rf = Rg = 750 ohms
* Connections:
  + input  |  −input  |  +Vsupply
  |  |  |  −Vsupply
  |  |  |  |  |  |  output
  |  |  |  |  |
.subckt EL2186/el 3 2 7 4 6

* Transimpedance Stage
  g1 0 18 17 0 1.0
  rol 18 0 450K
  cdp 18 0 0.675pF

* Input Stage
  e1 10 0 3 0 1.0
  vis 10 9 0V
  h2 9 12 vxx 1.0
  r1 2 11 400
  l1 11 12 25nH
  iinp 3 0 1.5uA
  iinn 2 0 3uA
  r12 3 0 2Meg

* Slew Rate Limiting
  h1 13 0 vis 600
  r2 13 14 1K
  d1 14 0 dclamp
  d2 0 14 dclamp

* High Frequency Pole
  e2 30 0 14 0 0.0016666666
  l3 30 17 150nH
  c5 17 0 0.8pF
  r5 17 0 165

* Output Stage
  q1 4 18 19 qn
  q2 7 18 20 qn
  q3 7 19 21 qn
  q4 4 20 22 qp
  r7 21 6 4
  r8 22 6 4
  ios1 7 19 1mA
  ios2 20 4 1mA

* Supply Current
  iinp 3 0 1.5uA
  iinn 2 0 3uA
  r12 3 0 2Meg

* Error Terms
  ips 7 4 0.2mA

* Models

.models qn npn(is = 5e-15 bf = 200 tf = 0.01ns)
.models qp pnp(is = 5e-15 bf = 200 tf = 0.01ns)
.models dclamp d(is = 1e-30 ibv = 0.266
  + bv = 0.71v n = 4)
.ends
EL2186C/EL2286C Macromodel — Contd.
Features
- Triple amplifier topology
- 3 mA supply current (per amplifier)
- 250 MHz - 3 dB bandwidth
- Low cost
- Fast disable
- Powers down to 0 mA
- Single- and dual-supply operation down to ±1.5V
- 0.05%/0.05° Diff. gain/Diff. phase into 150Ω
- 1200V/μs slew rate
- Large output drive current: 55 mA
- Available in single (EL2186C) and dual (EL2286C) form
- Non-power down versions available in single, dual, and quad (EL2180C, EL2280C, EL2480C)
- Lower power EL2170C/EL2176C family also available (1 mA/70 MHz) in single, dual and quad.

Applications
- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters
- Multiplexing
- Video broadcast equipment

General Description
The EL2386C is a triple current-feedback operational amplifier which achieves a -3 dB bandwidth of 250 MHz at a gain of +1 while consuming only 3 mA of supply current per amplifier. It will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. The EL2386C also includes a disable/power-down feature which reduces current consumption to 0 mA while placing the amplifier output in a high impedance state. In spite of its low supply current, the EL2386C can output 55 mA while swinging to ±4V on ±5V supplies. These attributes make the EL2386C an excellent choice for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For Single and Dual applications, consider the EL2186C/EL2286C. For Single, Dual and Quad applications without disable, consider the EL2180C, EL2280C, or EL2480C, all in industry standard pin outs. The EL2180C also is available in the tiny SOT-23 package, which is 28% the size of an SO8 package. For lower power applications where speed is still a concern, consider the EL2170C/EL2176C family which also comes in similar Single, Dual and Quad configurations. The EL2170C/EL2176C family provides a -3 dB bandwidth of 70 MHz while consuming 1 mA of supply current per amplifier.

Ordering Information

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<th>Temp. Range</th>
<th>Package</th>
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<tbody>
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<td>EL2386CN</td>
<td>-40°C to +85°C</td>
<td>16-Pin PDIP</td>
<td>MDPO031</td>
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<tr>
<td>EL2386CS</td>
<td>-40°C to +85°C</td>
<td>16-Pin SOIC</td>
<td>MDPO027</td>
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Connection Diagram

Manufactured under U.S. Patent No. 5,418,495.
## Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>VCC</td>
<td>Operating Ambient Temperature Range</td>
<td>-40°C to +85°C</td>
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<td></td>
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<tr>
<td>VCC</td>
<td>Operating Junction Temperature</td>
<td>150°C</td>
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<tr>
<td>Vs+ to Vs-</td>
<td>Common-Mode Input Voltage</td>
<td>±12.6V</td>
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<tr>
<td>Vs- to Vs+</td>
<td>Voltage between Vs+ and Vs-</td>
<td>±12.6V</td>
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<tr>
<td>±6</td>
<td>Differential Input Voltage</td>
<td>±6V</td>
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<td>±7.5mA</td>
<td>Current into +IN or -IN</td>
<td>±7.5mA</td>
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<td>See Curves</td>
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</table>

### Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Tj = TC = TA.

### DC Electrical Characteristics

Vs = ±5V, Rload = 150Ω, ENABLE = 0V, TA = 25°C unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td></td>
<td>2.5</td>
<td>15</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>TCVOS</td>
<td>Average Input Offset Voltage Drift</td>
<td>Measured from T_MIN to T_MAX</td>
<td>5</td>
<td></td>
<td>V</td>
<td>V</td>
<td>μV/°C</td>
</tr>
<tr>
<td>dVOS</td>
<td>VOS Matching</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>mV</td>
</tr>
<tr>
<td>+IIN</td>
<td>+ Input Current</td>
<td></td>
<td>1.5</td>
<td>15</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>d+IIN</td>
<td>+IIN Matching</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>nA</td>
</tr>
<tr>
<td>-IIN</td>
<td>- Input Current</td>
<td></td>
<td>16</td>
<td>40</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>d-IIN</td>
<td>-IIN Matching</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
<td>μA</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>VCM = ±3.5V</td>
<td>45</td>
<td>50</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>-ICMR</td>
<td>- Input Current Common Mode Rejection</td>
<td>VCM = ±3.5V</td>
<td>5</td>
<td>30</td>
<td></td>
<td>I</td>
<td>μA/V</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>VS = ±4V to ±6V</td>
<td>60</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>-IPSIR</td>
<td>- Input Current Power Supply Rejection</td>
<td>VS = ±4V to ±6V</td>
<td>1</td>
<td>15</td>
<td></td>
<td>I</td>
<td>μA/V</td>
</tr>
<tr>
<td>RSL</td>
<td>Transimpedance</td>
<td>VOUT = ±2.5V</td>
<td>120</td>
<td>300</td>
<td></td>
<td>I</td>
<td>kΩ</td>
</tr>
<tr>
<td>+RIN</td>
<td>+ Input Resistance</td>
<td>VCM = ±3.5V</td>
<td>0.5</td>
<td>2</td>
<td></td>
<td>I</td>
<td>MΩ</td>
</tr>
<tr>
<td>+CIN</td>
<td>+ Input Capacitance</td>
<td></td>
<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td>CMIR</td>
<td>Common Mode Input Range</td>
<td>VS = ±3.5 ±4.0</td>
<td>±3.5</td>
<td>±4.0</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td></td>
<td>±3.5</td>
<td>±4.0</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VO</td>
<td>VS = +5V Single-Supply, High</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VO</td>
<td>VS = +5V Single-Supply, Low</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Output Current</td>
<td></td>
<td>50</td>
<td>55</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics

\( V_S = \pm 5V, \, R_L = 1500, \, \text{ENABLE} = 0V, \, T_A = 25°C \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_S )</td>
<td>Supply Current—Enabled (per amplifier)</td>
<td>ENABLE = 2.0V</td>
<td>3</td>
<td>6</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{S(D)} )</td>
<td>Supply Current—Disabled (per amplifier)</td>
<td>ENABLE = 4.5V</td>
<td>0</td>
<td>50</td>
<td>I</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( C_{OUT(D)} )</td>
<td>Output Capacitance—Disabled</td>
<td>ENABLE = 4.5V</td>
<td>4.4</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( R_{IN-EN} )</td>
<td>ENABLE Pin Input Resistance</td>
<td>ENABLE = 2.0V to 4.5V</td>
<td>45</td>
<td>85</td>
<td>I</td>
<td>k( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( I_{IH-EN} )</td>
<td>ENABLE Pin Input Current—High</td>
<td>ENABLE = 4.5V</td>
<td>-0.04</td>
<td></td>
<td></td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{IL-EN} )</td>
<td>ENABLE Pin Input Current—Low</td>
<td>ENABLE = 0V</td>
<td>-53</td>
<td></td>
<td></td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( V_{DIS} )</td>
<td>Minimum Voltage at ENABLE to Disable</td>
<td></td>
<td>4.5</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{EN} )</td>
<td>Maximum Voltage at ENABLE to Enable</td>
<td></td>
<td>2.0</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

\( V_S = \pm 5V, \, R_P = R_G = 750 \, \Omega, \, R_L = 1500, \, \text{ENABLE} = 0V, \, T_A = 25°C \) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>-3 dB Bandwidth</td>
<td>( A_V = +1 )</td>
<td>250</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( A_V = +2 )</td>
<td>180</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>BW</td>
<td>±0.1 dB Bandwidth</td>
<td>( A_V = +2 )</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>( V_{OUT} = \pm 2.5V, , \text{Measured at} \pm 1.25V )</td>
<td>600</td>
<td>1200</td>
<td></td>
<td>IV</td>
<td>V/( \mu s )</td>
</tr>
<tr>
<td>( t_r, t_f )</td>
<td>Rise and Fall Time</td>
<td>( V_{OUT} = \pm 500mV )</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PD} )</td>
<td>Propagation Delay</td>
<td>( V_{OUT} = \pm 500mV )</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>( V_{OUT} = \pm 500mV )</td>
<td>3.0</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>( t_s )</td>
<td>0.1% Settling</td>
<td>( V_{OUT} = \pm 2.5V, A_V = -1 )</td>
<td>15</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain (Note 1)</td>
<td>( A_V = +2, , R_L = 150\Omega )</td>
<td>0.05</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase (Note 1)</td>
<td>( A_V = +2, , R_L = 150\Omega )</td>
<td>0.05</td>
<td></td>
<td></td>
<td>V</td>
<td>°</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain (Note 1)</td>
<td>( A_V = +1, , R_L = 500\Omega )</td>
<td>0.01</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase (Note 1)</td>
<td>( A_V = +1, , R_L = 500\Omega )</td>
<td>0.01</td>
<td></td>
<td></td>
<td>V</td>
<td>°</td>
</tr>
<tr>
<td>( t_{ON} )</td>
<td>Turn-On Time (Note 2)</td>
<td>( A_V = +2, , V_{IN} = +1V, , R_L = 150\Omega )</td>
<td>40</td>
<td>100</td>
<td>I</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{OFF} )</td>
<td>Turn-Off Time (Note 2)</td>
<td>( A_V = +2, , V_{IN} = +1V, , R_L = 150\Omega )</td>
<td>800</td>
<td>2000</td>
<td>I</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CS</td>
<td>Channel Separation</td>
<td>( f = 5, \text{MHz} )</td>
<td>85</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
</tbody>
</table>

Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mVp-p, \( f = 3.58\, \text{MHz} \).

Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.
Test Circuit (per Amplifier)

Simplified Schematic (per Amplifier)
Typical Performance Curves — Contd.

**Non-Inverting Frequency Response (Gain)**
- $R_r = 750 \Omega$
- $R_t = 150 \Omega$
- $A_v = +1$
- $A_v = +2$
- $A_v = +5$
- $A_v = +10$

**Inverting Frequency Response (Gain)**
- $R_r = 750 \Omega$
- $R_t = 150 \Omega$
- $A_v = -1$
- $A_v = -2$
- $A_v = -5$
- $A_v = -10$

**Transimpedance ($R_{OL}$) vs Frequency**

**PSRR and CMRR vs Frequency**

**Frequency Response for Various $R_p$ and $R_G$**
- $R_p = 430 \Omega$
- $V_s = \pm 5 \text{V}$
- $A_v = +2$
- $A_v = +5$

**Frequency Response for Various $R_L$ and $C_L$**
- $R_L = 750 \Omega$
- $C_L = 20 \text{pF}$, $R_L = 500 \Omega$
- $C_L = 50 \text{pF}$, $R_L = 150 \Omega$

**Frequency Response for Various $C_{IN-}$**
- $R_L = 750 \Omega$
- $R_t = 150 \Omega$
- $C_{IN-} = 2 \text{pF}$
- $C_{IN-} = 1 \text{pF}$
- $C_{IN-} = 0 \text{pF}$
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency

-3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains

-3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains

Output Voltage Swing vs Frequency

-3 dB Bandwidth and Peaking vs Supply Voltage

Output Voltage Swing vs Supply Voltage

Supply Current vs Supply Voltage

Common-Mode Input Range vs Supply Voltage

Slew Rate vs Supply Voltage
Typical Performance Curves — Contd.

- **Input Bias Current vs Die Temperature**
- **Short-Circuit Current vs Die Temperature**
- **Transimpedance (R<sub>OL</sub>) vs Die Temperature**
- **-3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains**
- **-3 dB Bandwidth vs Die Temperature for Various Inverting Gains**
- **Input Offset Voltage vs Die Temperature**
- **Supply Current vs Die Temperature**
- **Input Voltage Range vs Die Temperature**
- **Slew Rate vs Die Temperature**
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz

Settling Time vs Settling Accuracy

Small-Signal Step Response

Large-Signal Step Response

16-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature

16-Lead SO Maximum Power Dissipation vs Ambient Temperature

Channel to Channel Isolation vs Frequency

IN B, OUT A or IN C, OUT B IN B, OUT C or IN C, OUT A IN A, OUT C or IN A, OUT B
Applications Information

Product Description
The EL2386C is a current-feedback operational amplifier that offers a wide -3 dB bandwidth of 250 MHz, a low supply current of 3 mA per amplifier and the ability to power down to 0 mA. It also features high output current drive. The EL2386C can output 55 mA per amplifier. The EL2386C works with supply voltages ranging from a single 3V to ± 6V, and it is also capable of swinging to within 1V of either supply on the input and the output. Because of its current-feedback topology, the EL2386C does not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows its -3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2386C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single and Dual applications, consider the EL2186C/EL2286C. For Single, Dual and Quad applications without disable, consider the EL2180C, EL2280C, or EL2480C, all in industry standard pin outs. The EL2180C also is available in the tiny SOT-23 package, which is 28% the size of an SO8 package. For lower power applications where speed is still a concern, consider the EL2170C/EL2176C family which also comes in similar Single, Dual and Quad configurations with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 µF tantalum capacitor in parallel with a 0.1 µF capacitor has been shown to work well when placed at each supply pin. For single supply operation, where pin 3 (V₃₋) is connected to the ground plane, a single 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor across pins 14 and 3 will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down
The EL2386C amplifier can be disabled, placing its output in a high-impedance state. When disabled, the supply current is reduced to 0 mA. The EL2386C is disabled when its ENABLE pin is floating or pulled up to within 0.5V of the positive supply. Similarly, the amplifier is enabled by pulling its ENABLE pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2386C amplifier will be enabled when ENABLE is at 2V or less, and disabled when ENABLE is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2386C to be enabled by tying ENABLE to ground, even in +3V single-supply applications. The ENABLE pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at ENABLE. For example, with the supply voltages of the EL2186C at ±5V, if ENABLE is tied to -5V (rather than ground) the supply current will increase about 15% to 3.45 mA.
Applications Information — Contd.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2386C has less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various RF and RG, and Frequency Response for Various C_IN.

Feedback Resistor Values

The EL2386C has been designed and specified at gains of +1 and +2 with RF = 750Ω. This value of feedback resistor gives 250 MHz of -3 dB bandwidth at AV = +1 with about 2.5 dB of peaking, and 180 MHz of -3 dB bandwidth at AV = +2 with about 0.1 dB of peaking. Since the EL2386C is a current-feedback amplifier, it is also possible to change the value of RF to get more bandwidth. As seen in the curve of Frequency Response For Various RF and RG, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2386C is a current-feedback amplifier, its gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2386C to maintain about the same -3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of RF below the specified 750Ω and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2386C has been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2386C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2386C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2386C has an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2386C has an input range which spans from 1V to 4V. The output range of the EL2386C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2386C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2386C amplifier! Spe-
Applications Information — Contd.

cial circuitry has been incorporated in the EL2386C to reduce the variation of output impedance with current output. This results in $dG$ and $dP$ specifications of 0.05% and 0.05° while driving 150Ω at a gain of $+2$.

Video Performance has also been measured with a 500Ω load at a gain of $+1$. Under these conditions, the EL2386C has $dG$ and $dP$ specifications of 0.01% and 0.01° respectively while driving 500Ω at $AV = +1$.

For complete curves, see the Differential Gain and Differential Phase vs Input Voltage curves.

Output Drive Capability

In spite of its low 3 mA of supply current per amplifier, the EL2386C is capable of providing a minimum of ±50 mA of output current. This output drive level is unprecedented in amplifiers running at these supply currents. With a minimum ±50 mA of output drive, the EL2386C is capable of driving 50Ω loads to ±2.5V, making it an excellent choice for driving multiple video loads in RGB applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2386C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor ($R_G$) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor ($R_F$) to reduce the peaking.

Current Limiting

The EL2386C has no internal current-limiting circuitry. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±60 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Multiplexing with the EL2386C

The ENABLE pins on the EL2386C allow for multiplexing applications. Figure 1 shows an EL2386C with all 3 outputs tied together, driving a back terminated 75Ω video load. Three sine waves of varying amplitudes and frequencies are applied to the three inputs, while a 1 of 3 decoder selects one amplifier to be on at any given time. Figure 2 shows the resulting output wave form at

![Figure 1](image-url)
Applications Information — Contd.

These parameters are calculated as follows:

\[ T_{JMAX} = T_{MAX} + (\theta_{JA} \cdot n \cdot P_{D_{MAX}}) \]  \[1\]

where:

- \( T_{MAX} \) = Maximum Ambient Temperature
- \( \theta_{JA} \) = Thermal Resistance of the Package
- \( n \) = Number of Amplifiers in the Package
- \( P_{D_{MAX}} \) = Maximum Power Dissipation of Each Amplifier in the Package.

\( P_{D_{MAX}} \) for each amplifier can be calculated as follows:

\[ P_{D_{MAX}} = (2 \cdot V_{S} \cdot I_{S_{MAX}}) + (V_{S} - V_{OUT_{MAX}}) \cdot (V_{OUT_{MAX}} / R_{L}) \]  \[2\]

where:

- \( V_{S} \) = Supply Voltage
- \( I_{S_{MAX}} \) = Maximum Supply Current of 1 Amplifier
- \( V_{OUT_{MAX}} \) = Max. Output Voltage of the Application
- \( R_{L} \) = Load Resistance

\( V_{OUT} \). Switching is complete in about 100 ns. Notice the outputs are tied directly together. Decoupling resistors at each output are not required or advised when multiplexing.

Power Dissipation

With the high output drive capability of the EL2386C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when \( R_{L} \) falls below about 25Ω, it is important to calculate the maximum junction temperature (\( T_{J_{MAX}} \)) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2386C to remain in the safe operating area.
EL2386C Macromodel

* EL2386C Macromodel
* Revision A, July 1996
* AC characteristics used: \( R_f = R_g = 750 \) ohms
* Pin numbers reflect a standard single opamp

* Connections:
| + input | - input | + \( V_{\text{supply}} \) | - \( V_{\text{supply}} \) | output |

.*

.subeckt EL2386/EL 3 2 7 4 6

* Input Stage
| e1 10 0 3 0 1.0 |
| vis 10 9 0V |
| h2 9 12 vxx 1.0 |
| r1 2 11 400 |
| l1 11 12 25nH |
| jinp 3 0 1.5\( \mu \)A |
| jinn 2 0 3\( \mu \)A |
| r12 3 0 2Meg |

* Slew Rate Limiting
| h1 13 0 vis 600 |
| r2 13 14 1K |
| d1 14 0 dclamp |
| d2 0 14 dclamp |

* High Frequency Pole
| e2 30 0 14 0 0.001666666666 |
| 13 30 17 150nH |
| c5 17 0 0.8pF |
| r5 17 0 165 |

* Transimpedance Stage
| q1 0 18 17 0 1.0 |
| rol 18 0 450k |
| cdp 18 0 0.675pF |

* Output Stage
| q1 4 18 19 qp |
| q2 7 18 20 qn |
| q3 7 19 21 qn |
| q4 4 20 22 qp |
| r7 21 6 4 |
| r8 22 6 4 |
| ios1 7 19 1mA |
| ios2 20 4 1mA |

* Supply Current
| ips 7 4 0.2mA |

* Error Terms
| ivos 0 23 0.2mA |
| vxx 23 0 0V |
| e4 24 0 3 0 1.0 |
| e5 25 0 7 0 1.0 |
| e6 26 0 4 0 -1.0 |
| r9 24 23 316 |
| r10 25 23 3.2K |
| r11 26 23 3.2K |

* Models
| .model qn npn(is = 5e-15 bf = 200 tf = 0.1nS) |
| .model qp npn(is = 5e-15 bf = 200 tf = 0.1nS) |
| .model dclamp d(is = 1e-30 ibv = 0.266 + bv = 0.71v n = 4) |
| .ends |
EL2386C Macromodel — Contd.
Features

- Stable at gain of 2 and 100 MHz gain—bandwidth product (EL2211, EL2311, EL2411)
- Stable at gain of 1 and 50 MHz gain—bandwidth product (EL2210, EL2310, EL2410)
- 130V/μs slew rate
- Drives 150Ω load to video levels
- Inputs and outputs operate at negative supply rail
- ±5V or +10V supplies
- −60 dB isolation at 4.2 MHz

Applications

- Consumer video amplifier
- Active filters/integrators
- Cost sensitive applications
- Single supply amplifiers

General Description

This family of dual, triple and quad operational amplifiers built using Elantec’s Complementary Bipolar process offers unprecedented high frequency performance at a very low cost. They are suitable for any application such as consumer video, where traditional DC performance specifications are of secondary importance to the high frequency specifications. On ±5V supplies at a gain of +1 the EL2210C, EL2310C and the EL2410C will drive a 150Ω load to +2V, −1V with a bandwidth of 50 MHz and a channel to channel isolation of 60 dB or more. At a gain of +2 the EL2211C, EL2311C and EL2411C will drive a 150Ω load to +2V, −1V with a bandwidth of 100 MHz with the same channel to channel isolation. All four achieve 0.1 dB BW at 5 MHz.

The power supply operating range is fixed at ±5V or +10/0V. In single supply operation the inputs and outputs will operate to ground. Each amplifier draws only 7 mA of supply current.

Connection Diagrams
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Supply</td>
<td>18V</td>
<td>Power Dissipation</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>±Vs</td>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>6V</td>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>75 mA per amplifier</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantac performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_O = T_A$.

### Test Level
- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at $T_A = 25^\circ C$ and QA sample tested at $T_A = 25^\circ C$.
- **III**: QA sample tested per QA test plan QCX0002.
- **IV**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at $T_A = 25^\circ C$ for information purposes only.

## EL2210, EL2310, EL2410

### DC Electrical Characteristics

$V_S = \pm 5V, R_L = 1 \Omega$, Temp. = $25^\circ C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>EL2310C only</td>
<td>10</td>
<td>20</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL2311C only</td>
<td>10</td>
<td>25</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td></td>
<td>-15</td>
<td>-7</td>
<td>-3</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td></td>
<td>0.5</td>
<td>1.5</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{CLOS}$</td>
<td>Average Offset Current Drift</td>
<td>(Note 2)</td>
<td>-7</td>
<td></td>
<td></td>
<td>V</td>
<td>nA/°C</td>
</tr>
<tr>
<td>$A_{VOL}$</td>
<td>Open-Loop Gain</td>
<td></td>
<td>160</td>
<td>250</td>
<td>I</td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>160</td>
<td>250</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection</td>
<td>$V_S = \pm 4.5V$ to $\pm 5.5V$</td>
<td>50</td>
<td>60</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common Mode Rejection</td>
<td>$V_{CM} = \pm 2.4V, V_{OUT} = 0V$</td>
<td>60</td>
<td>80</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$CMIR$</td>
<td>Common Mode Input Range</td>
<td>$V_{S} = \pm 5V$</td>
<td>-5/+3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing</td>
<td>$R_L = R_F = 1 \Omega$ to Gnd</td>
<td>-2.5</td>
<td>-3.3</td>
<td>2.7</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = R_F = 1 \Omega$ to $150\Omega$ to Gnd</td>
<td>-0.45</td>
<td>-0.6, 2.9</td>
<td>2.5</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Output Short Circuit Current</td>
<td>Output to Gnd (Note 1)</td>
<td>75</td>
<td>125</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>No Load (per channel)</td>
<td>5.5</td>
<td>6.8</td>
<td>8.5</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$R_{IN}$</td>
<td>Input Resistance</td>
<td>Differential</td>
<td>150</td>
<td></td>
<td>V</td>
<td>KΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Common Mode</td>
<td>1.5</td>
<td></td>
<td>V</td>
<td>MΩ</td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>$A_V = +1 @ 10$ MHz</td>
<td>1</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$R_{OUT}$</td>
<td>Output Resistance</td>
<td></td>
<td>0.150</td>
<td></td>
<td>V</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>PSOR</td>
<td>Power Supply Operating Range</td>
<td>Dual Supply</td>
<td>±4.5</td>
<td>±6.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single Supply</td>
<td>9</td>
<td>13</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2-480
## EL2211, EL2311, EL2411

### DC Electrical Characteristics

\[ V_S = \pm 5V, R_L = 1 \, \text{k}\Omega, A_V = +2, \text{Temp.} = 25^\circ C \text{ unless otherwise noted} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td></td>
<td>5</td>
<td>12</td>
<td>1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Average Offset Voltage Drift (Note 2)</td>
<td></td>
<td>-25</td>
<td>V</td>
<td>( \mu V/\circ C )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td></td>
<td>-15</td>
<td>-7</td>
<td>-3</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_O )</td>
<td>Input Offset Current</td>
<td></td>
<td>0.5</td>
<td>1.5</td>
<td>I</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( TCI_{OS} )</td>
<td>Average Offset Current Drift (Note 2)</td>
<td></td>
<td>-7</td>
<td>V</td>
<td>( \text{nA/}^\circ \text{C} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Open-Loop Gain</td>
<td>( V_{OUT} = \pm 2V, R_L = 1 , \text{k}\Omega )</td>
<td>250</td>
<td>380</td>
<td></td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = +2V/0V, R_L = 150\Omega )</td>
<td>250</td>
<td>380</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( PSRR )</td>
<td>Power Supply Rejection</td>
<td>( V_S = \pm 4.5V ) to ( \pm 5.5V )</td>
<td>55</td>
<td>68</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( CMRR )</td>
<td>Common Mode Rejection</td>
<td>( V_{CM} = \pm 2.5V, V_{OUT} = 0V )</td>
<td>70</td>
<td>90</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( CMIR )</td>
<td>Common Mode Input Range</td>
<td>( V_S = \pm 5V )</td>
<td>-5/+3</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Voltage Swing</td>
<td>( R_L = R_F = 1 , \text{k}\Omega ) to Gnd</td>
<td>2.5</td>
<td>3.3</td>
<td>2.7</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = R_F = 1 , \text{k}\Omega + 150\Omega ) to Gnd</td>
<td>-0.45</td>
<td>-0.6</td>
<td>2.9</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = R_F = 1 , \text{k}\Omega ) to ( V_{EE} )</td>
<td>-4.95</td>
<td></td>
<td>3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Output Short Circuit Current</td>
<td>Output to Gnd (Note 1)</td>
<td>75</td>
<td>125</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>No Load</td>
<td>5.5</td>
<td>6.8</td>
<td>8.5</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( R_{IN} )</td>
<td>Input Resistance</td>
<td>Differential</td>
<td>150</td>
<td></td>
<td>V</td>
<td>( \text{k}\Omega )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Common Mode</td>
<td>1.5</td>
<td></td>
<td>V</td>
<td>( \text{M}\Omega )</td>
<td></td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td>( A_V = +1 ) @ 10 MHz</td>
<td>1</td>
<td></td>
<td>V</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>Output Resistance</td>
<td></td>
<td>0.150</td>
<td></td>
<td>V</td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( PSOR )</td>
<td>Power Supply Operating Range</td>
<td>Dual Supply</td>
<td>( \pm 4.5 )</td>
<td>( \pm 6.5 )</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single Supply</td>
<td>9</td>
<td>13</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

2-481
## EL2210, EL2310, EL2410

### Closed-Loop AC Characteristics

$V_S = \pm 5V$, AC Test Figure 1, Temp. = 25°C unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>$-3 \text{ dB Bandwidth (} V_{OUT} = 0.4 \text{ V}_{PP} \text{)}$</td>
<td>$A_V = +1$</td>
<td>110</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>$\pm 0.1 \text{ dB Bandwidth (} V_{OUT} = 0.4 \text{ V}_{PP} \text{)}$</td>
<td>$A_V = +1$</td>
<td>12</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain Bandwidth Product</td>
<td></td>
<td>55</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
<td></td>
<td>60</td>
<td>V</td>
<td>(°)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td></td>
<td>85</td>
<td>130</td>
<td>V</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>FBWP</td>
<td>Full Power Bandwidth (Note 3)</td>
<td></td>
<td>8</td>
<td>11</td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Rise Time, Fall Time</td>
<td>0.1V Step</td>
<td>2</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>0.1V Step</td>
<td>15</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay</td>
<td></td>
<td>3.5</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_S$</td>
<td>Settling to 0.1% ($A_V = 1$)</td>
<td>$V_S = \pm 5V, 2V$ Step</td>
<td>80</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$d_Q$</td>
<td>Differential Gain (Note 4)</td>
<td>NTSC/PAL</td>
<td>0.1</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$d_P$</td>
<td>Differential Phase (Note 4)</td>
<td>NTSC/PAL</td>
<td>0.2</td>
<td>V</td>
<td>(°)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$e_N$</td>
<td>Input Noise Voltage</td>
<td>10 KHz</td>
<td>15</td>
<td>V</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$i_N$</td>
<td>Input Noise Current</td>
<td>10 KHz</td>
<td>1.5</td>
<td>V</td>
<td>pA/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS</td>
<td>Channel Separation</td>
<td>$P = 5$ MHz</td>
<td>55</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Notes

- **Note 1:** A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
- **Note 2:** Measured from $T_{MIN}$ to $T_{MAX}$
- **Note 3:** For $V_S = \pm 5V$, $V_{OUT} = 4$ V_{PP}. Full power bandwidth is based on slew rate measurement using:
  \[ FPBW = \frac{SR}{(2\pi \cdot V_{peak})} \]
- **Note 4:** Video performance measured at $V_S = \pm 5V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$. 

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"2-482"
### EL2211, EL2311, EL2411

**Closed-Loop AC Characteristics**  \( V_S = \pm 5V, \) AC Test Figure 1, Temp. = 25°C unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>-3 dB Bandwidth (( V_{OUT} = 0.4 \text{ V}_{pp} ))</td>
<td>( A_V = +2 )</td>
<td>100</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>±0.1 dB Bandwidth (( V_{OUT} = 0.4 \text{ V}_{pp} ))</td>
<td>( A_V = +2 )</td>
<td>8</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain Bandwidth Product</td>
<td></td>
<td>130</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
<td></td>
<td>60</td>
<td>V</td>
<td>(%)</td>
<td>(*)</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td></td>
<td>100</td>
<td>140</td>
<td>V/\mu s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FBWP</td>
<td>Full Power Bandwidth</td>
<td>(Note 3)</td>
<td>8</td>
<td>11</td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>(t_r, t_f)</td>
<td>Rise Time, Fall Time</td>
<td>0.1V Step</td>
<td>2.5</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>0.1V Step</td>
<td>6</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{PD})</td>
<td>Propagation Delay</td>
<td></td>
<td>3.5</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_S)</td>
<td>Settling to 0.1% (( A_V = 1 ))</td>
<td>( V_S = \pm 5V, 2V ) Step</td>
<td>80</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(d_G)</td>
<td>Differential Gain (Note 4)</td>
<td>NTSC/PAL</td>
<td>0.04</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(d_p)</td>
<td>Differential Phase (Note 4)</td>
<td>NTSC/PAL</td>
<td>0.15</td>
<td>V</td>
<td>(%)</td>
<td>(*)</td>
<td></td>
</tr>
<tr>
<td>(i_N)</td>
<td>Input Noise Voltage</td>
<td>10 KHz</td>
<td>15</td>
<td>V</td>
<td>nV/rt (Hz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS</td>
<td>Channel Separation</td>
<td>( P = 5 \text{ MHz} )</td>
<td>55</td>
<td>V</td>
<td>pA/rt (Hz)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
2. Measured from \( T_{MIN} \) to \( T_{MAX} \)
3. For \( V_S = \pm 5V, V_{OUT} = 4 \text{ V}_{pp} \). Full power bandwidth is based on slew rate measurement using:
   \[ \text{FPBW} = \frac{\text{SR}}{2\pi \cdot V_{\text{peak}}} \]
4. Video performance measured at \( V_S = \pm 5V, A_V = +2 \) with 2 times normal video level across \( R_L = 150\Omega \).
Simplified Block Diagram

Typical Performance Curves

14-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

14-Lead SO
Maximum Power Dissipation vs Ambient Temperature

8-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

8-Lead SO
Maximum Power Dissipation vs Ambient Temperature

2210-3

2210-4
Application Information

Product Description
The EL2210, EL2310 and EL2410 are dual, triple and quad operational amplifiers stable at a gain of 1. The EL2211, EL2311 and the EL2411 are dual, triple and quad operational amplifiers stable at a gain of 2. All six are built on Elantec's proprietary complimentary process and share the same voltage mode feedback topology. This topology allows them to be used in a variety of applications where current mode feedback amplifiers are not appropriate because of restrictions placed on the feedback elements. These products are especially designed for applications where high bandwidth and good video performance characteristics are desired but the higher cost of more flexible and sophisticated products are prohibitive.

Power Supplies
These amplifiers are designed to work at a supply voltage difference of 10V to 12V. These amplifiers will work on any combination of ± supplies. All Electrical characteristics are measured with ±5V supplies. Below 9V total supply voltage the amplifiers' performance will degrade dramatically. The quiescent current is a direct function of total supply voltage. With a total supply voltage of 12V the quiescent supply current will increase from a typical 6.8 mA per amplifier to 8.5 mA per amplifier.

Output Swing vs Load
Please refer to the simplified block diagram. These amplifiers provide an NPN pull-up transistor output and a passive 1250Ω pull-down resistor to the most negative supply. In an application where the load is connected to $V_S-$ the output voltage can swing to within 200 mV of $V_S^-$. In split supply applications where the DC load is connected to ground the negative swing is limited by the voltage divider formed by the load, the internal 1250Ω resistor and any external pull-down resistor. If $R_L$ were 150Ω then it and the 1250Ω internal resistor limit the maximum negative swing to $(V_{EE}(150/1250 + 150)) - 0.53V$. The negative swing can be increased by adding an external resistor of appropriate value from the output to the negative supply. The simplified block diagram shows an 820Ω external pull-down resistor. This resistor is in parallel with the internal 1250Ω resistor. This will increase the negative swing to $V_{EE}(150/(1250 * 820/(1250 + 820) + 150)) - 1.16V$.

Power Dissipation and Loading
Without any load and a 10V supply difference the power dissipation is 70 mW per amplifier. At 12V supply difference this increases to 105 mW per amplifier. At 12V this translates to a junction temperature rise above ambient of 33° for the dual and 40° for the quad amplifier. When the amplifiers provide load current the power dissipation can rapidly rise.

In ±5V operation each output can drive a grounded 150Ω load to more than 2V. This operating condition will not exceed the maximum junction temperature limit as long as the ambient temperature is below 85°C, the device is soldered in place, and the extra pull-down resistor is 820Ω or more.

If the load is connected to the most negative voltage (ground in single supply operation) you can easily exceed the absolute maximum die temperature. For example the maximum die temperature should be 150°C. At a maximum expected ambient temperature of 85°C, the total allowable power dissipation for the SO-8 package would be:

$$P_D = (150 - 75)/180°C/W = 416 \text{ mW}$$

At 12V total supply voltage each amplifier draws a maximum of 8.5 mA and dissipates 12V * 8.5 mA = 100 mW or 200 mW for the dual amplifier. Which leaves 216 mW of increased power due to the load. If the load were 150Ω connected to the most negative voltage and the maximum voltage out were $V_S^- + 2V$ the load current would be 13 mA. Then an extra 266 mW ($(12V - 2V) * 13.3 \text{ mA} * 2$) would be dissipated in the EL2210 or EL2211. The total dual amplifier power dissipation would be 266 mW + 200 mW = 466 mW, more than the maximum 416 mW allowed. If the total supply difference were reduced to 10V, the same calculations would yield 170 mW quiescent power dissipation and 213 mW due to loading. This results in a die temperature of 143°C (75°C + 68°C).
Application Information — Contd.

In the above example, if the supplies were split \( \pm 6V \) and the 150\( \Omega \) loads were connected to ground, the load induced power dissipation would drop to \( 106 \, mW \) \((13.3 \, mA \times (6 - 2) \times 2)\) and the die temperature would be below the rated maximum.

Video Performance

Following industry standard practices (see EL2044 applications section) these six devices exhibit good differential gain (dG) and good differential phase (dP) with \( \pm 5V \) supplies and an external 820\( \Omega \) resistor to the negative supply, in a gain of 2 configuration. Driving 75\( \Omega \) back terminated cables to standard video levels \((1.428V \text{ at the amplifier})\) the EL2210, EL2310 and EL2410 have dG of 0.1% and dP of 0.2°. The EL2211, EL2311 and the EL2411 have dG of 0.04% and dP of 0.15°.

Due to the negative swing limitations described above, inverted video at a gain of 2 is just not practical. If swings below ground are required then changing the extra 820\( \Omega \) resistor to 500\( \Omega \) will allow reasonable dG and dP to approximately \(-0.75 \, mV\). The EL2211, EL2311 and EL2411 will achieve approximately 0.1%/0.4° between 0V and \(-0.75V\). Beyond \(-0.75V\) dG and dP get worse by orders of magnitude.

Differential gain and differential phase are fairly constant for all loads above 150\( \Omega \). Differential phase performance will improve by a factor of 3 if the supply voltage is increased to \( \pm 6V \).

Output Drive Capability

None of these devices have short circuit protection. Each output is capable of more than 100 mA into a shorted output. Care must be used in the design to limit the output current with a series resistor.

Printed-Circuit Layout

The EL2210C/EL2211C/EL2310C/EL2311C/EL2410C/EL2411C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 \( \mu F \) ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 \( K\Omega \) because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wirewound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.
**EL2210/EL2310/EL2410 Macromodel**

* Revision A, June 1994
* Application Hints:

* A pull down resistor between the output and V– is recommended
* to allow output voltages to swing close to V–. See datasheet
* for recommended values.

* Connections:

<table>
<thead>
<tr>
<th>+ In</th>
<th>– In</th>
<th>V+</th>
<th>V–</th>
<th>V_out</th>
</tr>
</thead>
</table>

.subckt EL2210/EL 3 2 8 4 1

q1 20 3 24 qp
q2 21 2 25 qp
q3 10 10 26 qp
q4 12 10 11 qp
q5 14 10 13 qp
q6 19 19 20 qn
q7 14 19 21 qn
q8 8 14 15 qn
q9 8 16 17 qn 10
r1 24 12 350
r2 12 25 350
r3 8 26 250
r4 8 11 150
r5 8 13 240
r6 20 4 150
r7 21 4 150
r8 15 17 700
r9 1 4 1250
r10 15 16 40
r11 17 1 15
r12 10 19 10K
r13 14 22 20
c1 22 4 0.45pF
c2 22 19 1pF
d1 1 14 dcap

.model qn npn(bf = 150 tf = 0.05nS)
.model qp pnp(bf = 90 tf = 0.05nS)
.model dcap d(rs = 200 cjo = 1e-12 vj = 0.8 tt = 100e-9)
.ends
EL2210C/11C/EL2310C/11C/EL2410C/11C
Low Cost, Dual, Triple and Quad Video Op Amps

EL2211/EL2311/EL2411 Macromodel

* Revision A, June 1994
* Application Hints:
  * A pull down resistor between the output and V- is recommended
  * to allow output voltages to swing close to V-. See datasheet
  * for recommended values.

* Connections:  + In
  * | - In
  * | V+
  * | V-
  * | Vout

.subckt EL2211/EL 3 2 8 4 1
q1 20 3 24 qp
q2 21 2 25 qp
q3 10 10 26 qp
q4 12 10 11 qp
q5 14 10 13 qp
q6 19 19 20 qn
q7 14 19 21 qn
q8 8 14 15 qn
q9 8 16 17 qn 10
r1 24 12 175
r2 12 25 175
r3 8 26 250
r4 8 11 150
r5 8 13 240
r6 20 4 150
r7 21 4 150
r8 15 17 700
r9 1 4 1250
r10 15 16 40
r11 17 1 15
r12 10 19 10K
r13 14 22 20
c1 22 4 0.42pF
c2 22 19 1pF
d1 1 14 dcap
.model qn nnp(bf = 150 tf = 0.05nS)
.model qp npn(bf = 90 tf = 0.05nS)
.model dcap d(rs = 200 cjo = 1e-12 vj = 0.8 tt = 100e-9)
.ends
Features
- 80 MHz $-3$ dB bandwidth for gains of 1 to 10
- 900 V/$\mu$s slew rate
- 10 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible
- Available in SOL-16

Applications
- RGB drivers
- RGB multiplexers
- RGB gain blocks
- Video gain blocks
- Coax cable driver
- ADC drivers/input multiplexer

General Description
The EL4393C is three wideband current-feedback amplifiers optimized for video performance. Each amplifier can drive a load of 150$\Omega$ at video levels. Each amplifier has a disable capability, which is controlled by a TTL/CMOS compatible logic signal. The EL4393C operates on supplies as low as $\pm 4$V up to $\pm 15$V.

Being a current-feedback design, the bandwidth stays relatively constant at approximately 80 MHz over the $\pm 1$ to $\pm 10$ gain range. The EL4393C has been optimized for use with 1300$\Omega$ feedback resistors at a gain of 2.

When the outputs are disabled, the supply current consumption drops, by about 4 mA per channel that is disabled. This feature can be used to reduce power dissipation.

Connection Diagram
Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between ( V_{S+} ) and ( V_{S-} )</td>
<td>Internal Power Dissipation</td>
<td>+33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage at ( V_{S+} )</td>
<td>Operating Ambient Temperature Range</td>
<td>+18V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage at ( V_{S-} )</td>
<td>Operating Junction Temperature</td>
<td>-18V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage between ( V_{IN+} ) and ( V_{IN-} )</td>
<td>Storage Temperature Range</td>
<td>±6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current into ( V_{IN+} ) or ( V_{IN-} )</td>
<td></td>
<td>5 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

Open Loop DC Electrical Characteristics Supplies at \( \pm 15V \), Load = 1 kΩ

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>+25°C</td>
<td>2</td>
<td>±15</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Temperature Coefficient of ( V_{OS} )</td>
<td>Full</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>( \mu V/°C )</td>
</tr>
<tr>
<td>( I_B^+ )</td>
<td>( I_{IN}^+ ) Input Bias Current</td>
<td>+25°C</td>
<td>0.2</td>
<td>5</td>
<td></td>
<td>I</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_B^- )</td>
<td>( I_{IN}^- ) Input Bias Current</td>
<td>+25°C</td>
<td>10</td>
<td>65</td>
<td></td>
<td>I</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( TCI_B^- )</td>
<td>Temperature Coefficient of ( I_B^- )</td>
<td>Full</td>
<td>25</td>
<td></td>
<td></td>
<td>V</td>
<td>( nA/°C )</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio (Note 1)</td>
<td>+25°C</td>
<td>50</td>
<td>58</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>( -ICMR )</td>
<td>( I_{IN}^- ) Input Common-Mode Current (Note 1)</td>
<td>+25°C</td>
<td>3</td>
<td>8</td>
<td></td>
<td>I</td>
<td>( \mu A/V )</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Note 2)</td>
<td>+25°C</td>
<td>50</td>
<td>58</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>( -IPSR )</td>
<td>( I_{IN}^- ) Current Supply Rejection (Note 2)</td>
<td>+25°C</td>
<td>2</td>
<td>5</td>
<td></td>
<td>I</td>
<td>( \mu A/V )</td>
</tr>
<tr>
<td>( R_{OL} )</td>
<td>Transimpedance</td>
<td>+25°C</td>
<td>100</td>
<td>217</td>
<td></td>
<td>I</td>
<td>kΩ</td>
</tr>
<tr>
<td>( R_{IN} )</td>
<td>( IN^+ ) Input Impedance</td>
<td>+25°C</td>
<td>2</td>
<td></td>
<td></td>
<td>I</td>
<td>MΩ</td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>( IN^+ ) Input Range</td>
<td>+25°C</td>
<td>±13</td>
<td>±13.5</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing; ( R_L = 1 ) kΩ</td>
<td>+25°C</td>
<td>±12</td>
<td>±13</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
### Open Loop DC Electrical Characteristics
Supplies at ±15V, Load = 1kΩ — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{SC})</td>
<td>Short-Circuit Current (Note 3)</td>
<td>+25°C</td>
<td>40</td>
<td>70</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{O, DIS})</td>
<td>Output Current when Disabled</td>
<td>+25°C</td>
<td>5</td>
<td>150</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(DIS V_{IL})</td>
<td>Disable Voltage for Logic Low</td>
<td>+25°C</td>
<td>0.8</td>
<td>I</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(DIS V_{IH})</td>
<td>Disable Voltage for Logic High</td>
<td>+25°C</td>
<td>2.2</td>
<td>I</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(DIS I_{IL})</td>
<td>Disable Logic Low Input Current</td>
<td>+25°C</td>
<td>3</td>
<td>25</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(DIS I_{IH})</td>
<td>Disable Logic High Input Current</td>
<td>+25°C</td>
<td>0</td>
<td>5</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{CC} (en))</td>
<td>Positive Supply Current all Channels Enabled</td>
<td>+25°C</td>
<td>15</td>
<td>20</td>
<td>±29</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{CC} (dis))</td>
<td>Positive Supply Current all Channels Disabled</td>
<td>+25°C</td>
<td>6</td>
<td>11</td>
<td>16</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{EE} (en))</td>
<td>Negative Supply Current all Channels Enabled</td>
<td>+25°C</td>
<td>13</td>
<td>18</td>
<td>±28</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{EE} (dis))</td>
<td>Negative Supply Current all Channels Disabled</td>
<td>+25°C</td>
<td>4</td>
<td>9</td>
<td>14</td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

Note 1: \(V_{CM} = \pm 10\)V for \(V_S = \pm 15\)V.
Note 2: \(V_{OS}\) is measured at \(V_S = \pm 4.5\)V and \(V_S = \pm 16\)V, both supplies are changed simultaneously.
Note 3: Only one output short circuited. Pulse test or use heatsink.

### Closed Loop AC Electrical Characteristics
Supplies at ±15V, Load = 150Ω and 15 pF, except where noted. \(R_f1\) and \(R_f2\) = 1500Ω; \(A_v = 2, T_A = 25°C\). (See note 8 re: test fixture)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate (Note 4)</td>
<td>960</td>
<td>V</td>
<td>V/μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate w/±5V Supplies (Note 5)</td>
<td>470</td>
<td>IV</td>
<td>V/μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_s)</td>
<td>Settling Time to 1% 5V, p-p 5V Step (Note 6)</td>
<td>32</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth, −3 dB</td>
<td>80</td>
<td>IV</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth, −0.1 dB</td>
<td>16</td>
<td>IV</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peaking</td>
<td>−3 dB BW Tests</td>
<td>0.6</td>
<td>IV</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(dG)</td>
<td>Differential Gain at 3.58 MHz at ±5V Supplies (Note 7)</td>
<td>0.03</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(d\theta)</td>
<td>Differential Phase at 3.58 MHz at ±5V Supplies (Note 7)</td>
<td>0.088</td>
<td>V</td>
<td>(%)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 4: \(R_L = 300\)Ω, −5V to +5V swing, SR measured at 20% to 80%.
Note 5: −2V to +2V swing, SR measured at 20% to 80%.
Note 6: \(R_L = 300\)Ω.
Note 7: DC offset from −0.7V through +0.7V AC amplitude is 286 mV, equivalent to 40 ire.
Note 8: Test fixture was designed to minimize capacitance at the \(I_{IN}^+\) input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.
Typical Performance Curves

Gain Flatness vs Rf at ± 5V

Gain Flatness vs Rf at ± 15V

Phase vs Rf at ± 5V

Phase vs Rf at ± 15V

Gain of 5, 10 vs Various Rf, Rg at ± 5V

Gain of 5, 10 vs Rf, Rg at ± 15V
Typical Performance Curves — Contd.

Disabled Isolation Test at ±5V

Disabled Isolation Test at ±15V

Cl Huffman Peaking

Voltage Noise

Differential Gain & Phase at 3.58 MHz

EL4393 MUX Channel Channel Isolation
Typical Performance Curves — Contd.

Supply Current vs Supply Voltage
MARKER (15.000V, 10.60 mA, -8.579 mA)

Max. Power Dissipation vs Ambient Temperature
16-Pin PDIP

Maximum Power Dissipation vs Ambient Temperature
16-Pin SOL

Small Signal Pulse Response

Large Signal Pulse Response

Enable/Disable with + VE Voltage Output

Enable/Disable with - VE Voltage Output
Typical Application for EL4393, and General Rules for PCB Layout

The figure shows two EL4393's configured as a 2:1 RGB multiplexer, and cable driver, driving 75Ω, back terminated cables. Each channel of the EL4393 is configured to give a gain of two, to make up for the losses of the back terminating resistor.

In this example, the Disable pins of each RGB section are driven by a complementary TTL "select" signal. Larger multiplexers can be assembled, with a 1-of-n TTL decoder selecting each RGB triplet.

The circuit gives channel isolations of typically better than $-50$ dB at 10 MHz, and with a 20 dB/decade slope, extending down to better than $-90$ dB at frequencies below 100 kHz.

The schematic does not show things like power supply decoupling, or pcb layout, grounding and signal returns, but these will all affect the overall performance of the circuit, and care should be taken with these aspects.

It is recommended that the $V_{CC}$ and $V_{EE}$ pins each be decoupled by a 0.1 μF NPO or X7R dielectric ceramic capacitors to ground within 0.1 inch of the part, and in parallel with the 0.1 μF, a 47 μF tantalum capacitor, also to ground. The 47 μF capacitors should be within 0.25 inch of their power pins. The ground plane should be underneath the package, but cut away from the In- inputs. Care should be taken with the center channel feedback—it must be kept away from any of the in+ or in- pins, if it has to go under the package. Route the G-out line between the pin 3 ground and the pin 4 in- if going under the package is essential. Otherwise, loop the G-out trace around all the other circuitry, to its Rf resistor. The Rf and if used, Rg resistors should be on the input side of the package, to minimize trace length on the in- pins.

The digital input disables are on the output side of the package, so that a good ground plane down the center of the board underneath the package will isolate any fast edges from the sensitive inputs.
Typical Application Circuit
**EL4393C Macromodel**

- Revision A, July 1993
- Enhancements include PSRR, CMRR, and Slew Rate Limiting
- Connections:
  - + input
  - - Input
  - + Vsupply
  - - Vsupply
  - Putput
- subckt EL4393/EL 3 2 7 4 6
- Input Stage
- e1 10 0 3 0 1.0
  - via 10 0 V0
h2 9 12 vxx 1.0
  - r1 2 11 50
  - l1 1 12 29 nH
  - iiinp 3 0 0.2 μA
  - iiinn 2 0 10 μA
- Slew Rate Limiting
  - h1 13 0 vis 600
  - r2 13 14 1K
  - d1 14 0 dclamp
  - d2 0 14 dclamp
- High Frequency Pole
  - c2 30 0 14 0 0.0016666666
  - l5 30 17 1.2 μH
  - c5 17 0 1 pF
  - r5 17 0 500
- Transimpedance Stage
  - g1 0 18 17 0 1.0
  - rol 18 0 250k
  - cdp 18 0 2.2 pF

* Output Stage
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5 mA
ios2 20 4 2.5 mA

* Error Terms
ivos 0 23 2 mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 33 1K

* Models
.model qn nnpn (is = 5e-15 bf = 100 tf = 0.2 nS)
.model qp npn (is = 5e-15 bf = 100 tf = 0.2 nS)
.model dclamp d (is = 1e-30 ibv = 0.266 bv = 1.5 n = 4)
.ends
EL4393C Macromodel — Contd.

Simplified Schematic of One Channel of EL4393
**Features**
- Fully differential inputs and feedback
  - Differential input range of ±2V
  - Common-mode range of ±12V
  - High CMRR at 4 MHz of 70 dB
  - Stable at gains of 1, 2
- Calibrated and clean input clipping
- EL4430—80 MHz @ G = 1
- EL4431—160 MHz GBWP
- 380V/μs slew rate
- 0.02% or ° differential gain or phase
- Operates on ±5 to ±15V supplies with no AC degradation

**Applications**
- Line receivers
- "Loop-through" interface
- Level translation
- Magnetic head pre-amplification
- Differential-to-single-ended conversion

**General Description**
The EL4430 and 4431 are video instrumentation amplifiers which are ideal for line receivers, differential-to-single-ended converters, transducer interfacing, and any situation where a differential signal must be extracted from a background of common-mode noise or DC offset.

These devices have two differential signal inputs and two differential feedback terminals. The FB terminal connects to the amplifier output, or a divided version of it to increase circuit gain, and the REF terminal is connected to the output ground or offset reference.

The EL4430 is compensated to be stable at a gain of 1 or more, and the EL4431 for a gain of 2 or more.

The amplifiers have an operational temperature of −40°C to +85°C and are packaged in plastic 8-pin DIP and SO-8.

The EL4430 and EL4431 are fabricated with Elancroc's proprietary complementary bipolar process which gives excellent signal symmetry and is free from latchup.

**Connection Diagram**

![Connection Diagram](image)
Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{+})</td>
<td>Positive Supply Voltage</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_S)</td>
<td>(V_+) to (V_-) Supply Voltage</td>
<td>33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Voltage at any Input or Feedback</td>
<td>16.5V to 33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{IN})</td>
<td>Difference between Pairs of Inputs or Feedback</td>
<td>6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{IN})</td>
<td>Current into any Input, or Feedback Pin</td>
<td>4 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_D = T_C = T_A\).

Open-Loop DC Electrical Characteristics

Power supplies at \(\pm 5V, T_A = 25°C\). For the EL4431, \(R_F = R_G = 500k\Omega\).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DIFF})</td>
<td>Differential input voltage - Clipping ((V_{CM} = 0))</td>
<td>2.0</td>
<td>2.3</td>
<td>1.8</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{DIFF})</td>
<td>0.1% nonlinearity</td>
<td>E1A430/31</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{CM})</td>
<td>Common-mode range ((V_{DIFF} = 0))</td>
<td>(V_S = \pm 5V)</td>
<td>(V_S = \pm 15V)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{OS})</td>
<td>Input offset voltage</td>
<td>E1A430/31</td>
<td>2</td>
<td>8</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(I_{B})</td>
<td>Input bias current ((IN+), (IN-), REF, and FB terminals)</td>
<td>12</td>
<td>20</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input offset current between (IN+) and (IN-) and between REF and FB</td>
<td>0.2</td>
<td>2</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(R_{IN})</td>
<td>Input resistance</td>
<td>E1A430/31</td>
<td>100</td>
<td>230</td>
<td>I</td>
<td>k\Omega</td>
</tr>
<tr>
<td>(CMRR)</td>
<td>Common-mode rejection ratio</td>
<td>70</td>
<td>90</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power supply rejection ratio</td>
<td>E1A430/31</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(E_G)</td>
<td>Gain error, excluding feedback resistors</td>
<td>E1A430/31</td>
<td>-1.5</td>
<td>-0.2</td>
<td>+0.5</td>
<td>I</td>
</tr>
<tr>
<td>(V_O)</td>
<td>Output voltage swing</td>
<td>E1A430, (V_S = \pm 5V)</td>
<td>(\pm 2)</td>
<td>(\pm 2.8)</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>(V_S = \pm 15V)</td>
<td>(\pm 12)</td>
<td>(\pm 12.8)</td>
<td></td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>EL4431, (V_S = \pm 5V)</td>
<td>(\pm 2.5)</td>
<td>(\pm 3.0)</td>
<td></td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>(V_S = \pm 15V)</td>
<td>(\pm 12.5)</td>
<td>(\pm 13.0)</td>
<td></td>
<td></td>
<td>I</td>
</tr>
<tr>
<td>(I_{SC})</td>
<td>Output short-circuit current</td>
<td>40</td>
<td></td>
<td>90</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(I_S)</td>
<td>Supply current, (V_S = \pm 15V)</td>
<td></td>
<td></td>
<td>13.5</td>
<td>16</td>
<td>I</td>
</tr>
</tbody>
</table>
**Closed-Loop AC Electrical Characteristics** Power supplies at ±12V, T_A = 25°C, R_L = 500Ω for the EL4430, R_L = 150Ω for the EL4431, C_L = 15 pF. For the EL4431, R_F = R_G = 500Ω.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW, –3 dB</td>
<td>–3 dB small-signal bandwidth</td>
<td>EL4430</td>
<td>82</td>
<td>80</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL4431</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>BW, ±0.1 dB</td>
<td>0.1 dB flatness bandwidth</td>
<td>EL4430</td>
<td>20</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL4431</td>
<td>14</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>Peaking</td>
<td>Frequency response peaking</td>
<td>EL4430</td>
<td>0.6</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL4431</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate, V_OUT between –2V and +2V</td>
<td>All</td>
<td>380</td>
<td></td>
<td>V</td>
<td>V/μs</td>
</tr>
<tr>
<td>V_N</td>
<td>Input-referred noise voltage density</td>
<td>EL4430/31</td>
<td>26</td>
<td></td>
<td>V</td>
<td>nV/rt-Hz</td>
</tr>
<tr>
<td>dG</td>
<td>Differential gain error, V_offset between –0.7V and +0.7V</td>
<td>EL4430</td>
<td>0.02</td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL4431, R_L = 150Ω</td>
<td>0.04</td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>dθ</td>
<td>Differential gain error, V_offset between –0.7V and +0.7V</td>
<td>EL4430</td>
<td>0.02</td>
<td></td>
<td>V</td>
<td>(%)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EL4431, R_L = 150Ω</td>
<td>0.08</td>
<td></td>
<td>V</td>
<td>(%)</td>
</tr>
<tr>
<td>T_S</td>
<td>Settling time, to 0.1% from a 4V step</td>
<td>EL4430</td>
<td>48</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Test Circuit**

![Test Circuit Diagram]

**Typical Performance Curves**

![Common-Mode Rejection Ratio vs Frequency]
Typical Performance Curves — Contd.

EL4430 Frequency Response for Various $R_L$, $C_L$
$V_S = \pm 5V$

- $R_L = 500\Omega$, $C_L = 41\ pF$
- $R_L = 500\Omega$, $C_L = 23\ pF$
- $R_L = 500\Omega$, $C_L = 8\ pF$
- $R_L = 150\Omega$, $C_L = 41\ pF$
- $R_L = 150\Omega$, $C_L = 23\ pF$
- $R_L = 150\Omega$, $C_L = 8\ pF$

EL4431 Frequency Response for Various $R_L$, $C_L$
$V_S = \pm 15V$

- $R_L = 500\Omega$, $C_L = 41\ pF$
- $R_L = 500\Omega$, $C_L = 23\ pF$
- $R_L = 500\Omega$, $C_L = 8\ pF$
- $R_L = 150\Omega$, $C_L = 41\ pF$
- $R_L = 150\Omega$, $C_L = 23\ pF$
- $R_L = 150\Omega$, $C_L = 8\ pF$

EL4431 Frequency Response for Various $R_L$, $C_L$
$V_S = \pm 15V$

- $R_L = 500\Omega$, $C_L = 41\ pF$
- $R_L = 500\Omega$, $C_L = 23\ pF$
- $R_L = 500\Omega$, $C_L = 8\ pF$
- $R_L = 150\Omega$, $C_L = 41\ pF$
- $R_L = 150\Omega$, $C_L = 23\ pF$
- $R_L = 150\Omega$, $C_L = 8\ pF$
Typical Performance Curves — Contd.

EL4430 Differential Gain and Phase vs Input Offset Voltage for $V_S = \pm 5V$

![Typical Performance Curves](image)

EL4431 Differential Gain and Phase vs Input Offset Voltage for $V_S = \pm 5V$

![Typical Performance Curves](image)

EL4430 Differential Gain and Phase Error vs $R_L$

![Typical Performance Curves](image)

EL4431 Differential Gain and Phase Error vs $R_L$

![Typical Performance Curves](image)

EL4430 Nonlinearity vs Input Signal Span

![Typical Performance Curves](image)

EL4431 Nonlinearity vs Input Signal Span

![Typical Performance Curves](image)
Typical Performance Curves — Contd.

EL4430 -3 dB Bandwidth and Peaking vs Supply Voltage for $\Delta V = +1$  

EL4430 -3 dB Bandwidth and Peaking vs Die Temperature for $\Delta V = +1$  

EL4430 Gain, -3 dB Bandwidth and Peaking vs Load Resistance for $\Delta V = +1$  

EL4431 -3 dB Bandwidth and Peaking vs Supply Voltage  

EL4431 -3 dB Bandwidth and Peaking vs Die Temperature for $\Delta V = +2$  

EL4431 Gain, -3 dB Bandwidth and Peaking vs Load Resistance for $\Delta V = +2$
Typical Performance Curves — Contd.

- **Slew Rate vs Supply Voltage**
- **Slew Rate vs Die Temperature**
- **Input Voltage and Current Noise vs Frequency**
- **Common Mode Input Range vs Supply Voltage**
- **Offset Voltage vs Die Temperature**
- **Bias Current vs Die Temperature**
- **Supply Current vs Supply Voltage**
- **Supply Current vs Die Temperature**
- **Power Dissipation vs Ambient Temperature**
Applications Information
The EL4430 and EL4431 are designed to convert a fully differential input to a single-ended output. It has two sets of inputs; one which is connected to the signal and does not respond to its common-mode level, and another which is used to complete a feedback loop with the output. Here is a typical connection:

The gain of the feedback divider is H. The transfer function of the part is

\[ V_{OUT} = A_O \times ((V_{IN}^+) - (V_{IN}^-) + (V_{REF} - V_{FB})). \]

\( V_{FB} \) is connected to \( V_{OUT} \) through a feedback network, so \( V_{FB} = H \times V_{OUT} \). \( A_O \) is the open-loop gain of the amplifier, and is about 600 for the EL4430 and EL4431. The large value of \( A_O \) drives

\[ (V_{IN}^+) - (V_{IN}^-) + (V_{REF} - V_{FB}) \rightarrow 0. \]

Rearranging and substituting for \( V_{FB} \)

\[ V_{OUT} = \frac{(V_{IN}^+) - (V_{IN}^-) + V_{REF}}{H}. \]

Thus, the output is equal to the difference of the \( V_{IN} \)'s and offset by \( V_{REF} \), all gained up by the feedback divider ratio. The input impedance of the FB terminal (equal to \( R_{IN} \) of the input terminals) is in parallel with an \( R_G \), and raises circuit gain slightly.

The EL4430 is stable for a gain of 1 (a direct connection between \( V_{OUT} \) and FB) or more and the EL4431 for gains of 2 or more. It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel of resistors \( R_F \) and \( R_G \) and stray capacitance should be at least 200 MHz; typical strays of 3 pF thus require a feedback impedance of 270Ω or less. Two 510Ω resistors are acceptable for a gain of 2; 300Ω and 2700Ω make a good gain-of-10 divider. Alternatively, a small capacitor across \( R_F \) can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB terminal input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors (for a gain of 2) across equal divider resistors will dominate parasitic effects and allow a higher divider resistance.

Input Connections
The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to 4" of unshielded wiring or about 6" of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often, placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of approximately 51Ω to de-Q the inputs.

Signal Amplitudes
Signal input common-mode voltage must be between (V-) + 3V and (V+) - 3V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4430 and EL4431. The input range is substantially constant with temperature.

The Ground Pin
The ground pin draws only 6µA maximum DC current, and may be biased anywhere between (V-) + 2.5V and (V+) - 3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances CMRR over frequency, and if connected to a potential other than ground, it must be bypassed.
Applications Information — Contd.

Power Supplies
The instrumentation amplifiers work well on any supplies from ±3V to ±15. The supplies may be of different voltages as long as the requirements of the Gnd pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7µF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as low as 0.01µF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V- to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the amplifiers increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

\[ P_D = 2 \times V_S \times I_{S, \text{max}} + (V_S - V_O) \times V_O/R_{\text{PAR}} \]

where \( I_{S, \text{max}} \) is the maximum supply current
\( V_S \) is the ± supply voltage (assumed equal)
\( V_O \) is the output voltage
\( R_{\text{PAR}} \) is the parallel of all resistors loading the output

For instance, the EL4431 draws a maximum of 16 mA and we might require a 2V peak output into 150Ω and a 270Ω + 270Ω feedback divider. The \( R_{\text{PAR}} \) is 117Ω. The dissipation with ±5V supplies is 201 mW. The maximum supply voltage that the device can run on for a given \( P_D \) and the other parameter is

\[ V_{S, \text{max}} = \frac{(P_D + V_O^2/R_{\text{PAR}})}{(2I_S + V_O/R_{\text{PAR}})} \]

The maximum dissipation a package can offer is

\[ P_{D, \text{max}} = \frac{(T_J, \text{max} - T_A, \text{max})}{\theta_{JA}} \]

where \( T_J, \text{max} \) is the maximum die junction temperature, 150°C for reliability, less to retain optimum electrical performance.
\( T_A, \text{max} \) is the ambient temperature, 70°C for commercial and 85°C for industrial range.
\( \theta_{JA} \) is the thermal resistance of the mounted package, obtained from datasheet dissipation curves.

The more difficult case is the SO-8 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 170°C/W gives a dissipation of 382 mW at 85°C. This allows a maximum supply voltage of ±8.5V for the EL4431 operated in our example. If an EL4430 were driving a light load (\( R_{\text{PAR}} \to \infty \)), it could operate on ±15V supplies at a 70°C maximum ambient.

Output Loading
The output stage of the instrumentation amplifiers is very powerful. It typically can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this datasheet, or higher purely transient currents.

Gain or gain accuracy degrades only 10% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads <100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it (12Ω to 51Ω should suffice). A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.
* Macromodel
* This is a Pspice-compatible macromodel of the EL4430 video instrumentation amplifier assembled as a subcircuit. The pins are numbered sequentially as the subcircuit interface nodes. T1 is a transmission line which provides a good emulation of the more complicated real device. This model correctly displays the characteristics of input clipping, frequency response, CMRR both AC and DC, output clipping, output sensitivity to capacitive loads, gain accuracy, slewrate limiting, input bias current and impedance. The macromodel does not exhibit proper results with respect to supply current, supply sensitivities, offsets, output current limit, differential gain or phase, nor temperature.

* Connections:

```
.SUBCKT EL4430/EL
*** EL4430 macromodel ***
*****
i1 7 10 .00103
i2 7 11 .00103
i3 7 12 .00105
i4 7 13 .00105
v1 7 14 3
v2 7 15 3
v3 19 2 3
*****
c1 11 1 .03p
c2 12 1 .03p
c3 18 1 2.1p
c4 16 17 .6p
*****
r1 10 11 2000
r2 12 13 2000
r3 10 1 30e6
r4 16 2 1000
r5 17 2 1000
r6 18 1 1.27e6
r7 23 21 20
r8 21 8 100
*****
11 21 8 50n
*****
d1 11 14 diode
d2 12 14 diode
d3 18 15 diode
d4 19 18 diode
.model diode d(tt=120n)
*****
q1 16 3 10 1 pnp
q2 17 4 11 1 pnp
q3 16 5 12 1 pnp
q4 17 6 13 1 pnp
.model pnp pnp (bf=90 va=44 tr=50n)
*****
g1 18 1 17 16 .0005
e1 20 1 18 1.0
t1 22 1 20 1 z0=50 td=1.5n
r1t1 22 1 50
c2 23 1 22 1.0
*****
.ENDS
```
Features
- Complete variable-gain amplifier with output amplifier, requires no extra components
- Excellent linearity of 0.2%
- 70 MHz signal bandwidth
- Operates on ±5V to ±15V supplies
- All inputs are differential
- 400V/μs slew rate
- >70dB attenuation @ 4 MHz

Applications
- Leveling of varying inputs
- Variable filters
- Fading
- Text insertion into video

General Description
The EL4451C is a complete variable gain circuit. It offers wide bandwidth and excellent linearity while including a powerful output voltage amplifier, drawing modest supply current.

The EL4451C operates on ±5V to ±15V supplies and has an analog input range of ±2V, making it ideal for video signal processing. AC characteristics do not change appreciably over the ±5V to ±15V supply range.

The circuit has an operational temperature range of −40°C to +85°C and is packaged in plastic 14-pin DIP and 14-lead SO.

The EL4451C is fabricated with Elantec's proprietary complementary bipolar process which provides excellent signal symmetry and is free from latch up.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4451CN</td>
<td>−40°C to +85°C</td>
<td>14-Pin P-DIP</td>
</tr>
<tr>
<td>EL4451CS</td>
<td>−40°C to +85°C</td>
<td>14-Lead SO</td>
</tr>
</tbody>
</table>

Connection Diagram

```
NC 1
GND 2
V- 3
V+ 4
VIN+ 5
VIN- 6
NC 7
Gain+ 8
Gain- 9
FB 10
REF 11
VOUT 12
NC 13
V+ 14
```
## EL4451C
**Wideband Variable-Gain Amplifier, Gain of 2**

### Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+</td>
<td>Positive Supply Voltage</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V+</td>
<td>V+ to V− Supply Voltage</td>
<td>33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>Voltage at any Input or Feedback V+ to V−</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔVIN</td>
<td>Difference between Pairs of Inputs or Feedback</td>
<td>6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIN</td>
<td>Current into any Input, or Feedback Pin</td>
<td>4mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOUT</td>
<td>Continuous Output Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>30mA</td>
</tr>
<tr>
<td>PD</td>
<td>Maximum Power Dissipation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TS</td>
<td>Storage Temperature Range</td>
<td>−60°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Eltec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TJ = TC = TA.

### Test Level Procedure
- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at TA = 25°C and QA sample tested at TA = 25°C, TMAX and TMIN per QA test plan QCX0002.
- **III**: QA sample tested per QA test plan QCX0002.
- **IV**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at TA = 25°C for information purposes only.

### Open-Loop DC Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDIFF</td>
<td>Signal input differential input voltage - Clipping</td>
<td>1.8</td>
<td>2.0</td>
<td>2.8</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>0.2% nonlinearity</td>
<td>1.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>VCM</td>
<td>Common-mode range of VIN: VDIFF = 0, V± = ±5V V± = ±15V</td>
<td>±2.0</td>
<td>±2.8</td>
<td>±12.8</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V± = ±15V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>VOS</td>
<td>Input offset voltage</td>
<td>7</td>
<td>25</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>VOS, FB</td>
<td>Output offset voltage</td>
<td>8</td>
<td>25</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>VG,100%</td>
<td>Extrapolated voltage for 100% gain</td>
<td>1.9</td>
<td>2.1</td>
<td>2.2</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>VG,0%</td>
<td>Extrapolated voltage for 0% gain</td>
<td>−0.16</td>
<td>−0.06</td>
<td>0.06</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>VG,1V</td>
<td>Gain at VGAIN = 1V</td>
<td>0.95</td>
<td>1.05</td>
<td>1.15</td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td>IB</td>
<td>Input bias current (all inputs)</td>
<td>−20</td>
<td>−9</td>
<td>0</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>IOS</td>
<td>Input offset current between VIN + and VIN−, Gain + and Gain −, FB and Ref</td>
<td>0.2</td>
<td>4</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>NL</td>
<td>Non-linearity, VIN between −1V and +1V, VG = 1V</td>
<td>0.2</td>
<td>0.5</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>FT</td>
<td>Signal feedthrough, VG = −1V</td>
<td>−100</td>
<td>−70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>RIN, VIN</td>
<td>Input resistance, VIN</td>
<td>100</td>
<td>230</td>
<td></td>
<td>I</td>
<td>KΩ</td>
</tr>
<tr>
<td>RIN, FB</td>
<td>Input resistance, FB</td>
<td>200</td>
<td>460</td>
<td></td>
<td>V</td>
<td>KΩ</td>
</tr>
<tr>
<td>RIN, RGAIN</td>
<td>Input resistance, gain input</td>
<td>50</td>
<td>100</td>
<td></td>
<td>I</td>
<td>KΩ</td>
</tr>
</tbody>
</table>

---

2-512
Open-Loop DC Electrical Characteristics — Contd.
Power Supplies at ±5V, T_A = 25°C, R_L = 500Ω.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio of V_IN</td>
<td>70</td>
<td>90</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio of V_OS, FB, V_S = ±5V to ±15V</td>
<td>50</td>
<td>60</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>V_O</td>
<td>Output voltage swing V_S = ±5V</td>
<td>±2.5</td>
<td>6.0</td>
<td>±2.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_IN = 0, V_REF varied) V_S = ±15V</td>
<td>±12.5</td>
<td>12.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_SC</td>
<td>Output short-circuit current</td>
<td>40</td>
<td>85</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_S</td>
<td>Supply current, V_S = ±15V</td>
<td>15.5</td>
<td>18</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

Closed-Loop AC Electrical Characteristics
Power supplies at ±12V, T_A = 25°C. R_L = 500Ω, C_L = 15pF, V_O = 1V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW, -3dB</td>
<td>-3dB small-signal bandwidth, signal input</td>
<td>70</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>BW, ±0.1dB</td>
<td>0.1dB flatness bandwidth, signal input</td>
<td>10</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Peaking</td>
<td>Frequency response peaking</td>
<td>0.6</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>BW, gain</td>
<td>-3dB small-signal bandwidth, gain input</td>
<td>70</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate, V_OUT between -2V and +2V, R_F = R_G = 500Ω</td>
<td>400</td>
<td></td>
<td>V</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>V_N</td>
<td>Input referred noise voltage density</td>
<td>110</td>
<td></td>
<td>V</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential gain error, V_offset between -0.7V and +0.7V</td>
<td>0.9</td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>dθ</td>
<td>Differential phase error, V_offset between -0.7V and +0.7V</td>
<td>0.2</td>
<td></td>
<td>V</td>
<td>*</td>
<td></td>
</tr>
</tbody>
</table>

Test Circuit

Note: For typical performance curves, R_F = 0, R_G = ∞, V_GAIN = 1V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.
Typical Performance Curves

Frequency Response for Various Feedback Divider Ratios

Gain, -3 dB Bandwidth, and Peaking vs Load Resistance

Frequency Response for Various $R_L$, $C_L$

$V_S = \pm 5V$

$V_S = \pm 15V$

-3 dB Bandwidth and Peaking vs Supply Voltage

-3 dB Bandwidth and Peaking vs Die Temperature

Frequency Response for Various Gain Settings

Slew Rate vs Supply Voltage

Slew Rate vs Die Temperature

$R_f = R_o = 500\Omega$

$V_S = \pm 12V$
Typical Performance Curves — Contd.

**Common-Mode Rejection Ratio vs Frequency**

**Input Voltage Noise vs Frequency**

**Nonlinearity vs Input Signal**

**Differential Gain Error vs Input Offset Voltage \( V_S = \pm 5V \) or \( \pm 12V \)**

**Differential Phase Error vs Input Offset Voltage \( V_S = \pm 5V \)**

**Differential Phase Error vs Input Offset Voltage \( V_S = \pm 12V \)**

**Differential Gain and Phase Errors vs Gain Setting**

**Differential Gain and Phase Errors vs Load Resistance**

---

*EL4451C*

Wideband Variable-Gain Amplifier, Gain of 2

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Typical Performance Curves — Contd.

Gain vs \( V_{\text{GAIN}} \)

Offset Voltage vs Die Temperature

Bias Current vs Die Temperature

Change in \( V_{G,100\%} \) and \( V_{G,0\%} \) vs Die Temperature

Common Mode Input Range vs Supply Voltage

Supply Current vs Die Temperature

Supply Current vs Supply Voltage

14-Pin Package Power Dissipation vs Ambient Temperature
Applications Information
The EL4451 is a complete two-quadrant multiplier/gain control with 70 MHz bandwidth. It has three sets of inputs; a differential signal input $V_{IN}$, a differential gain-controlling input $V_{GAIN}$, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:

The gain of the feedback divider is

$$H = \frac{R_G}{R_G + R_F}$$

The transfer function of the part is

$$V_{OUT} = A_0 \times ((V_{IN}^+) - (V_{IN}^-)) \times ((V_{GAIN}^+) - (V_{GAIN}^-)) + (V_{REF} - V_{FB})$$

$V_{FB}$ is connected to $V_{OUT}$ through a feedback network, so $V_{FB} = H \times V_{OUT}$. $A_0$ is the open-loop gain of the amplifier, and is approximately 600. The large value of $A_0$ drives $((V_{IN}^+) - (V_{IN}^-)) \times ((V_{GAIN}^+) - (V_{GAIN}^-)) + (V_{REF} - V_{FB}) \to 0$.

Rearranging and substituting for $V_{FB}$

$$V_{OUT} = \frac{((V_{IN}^+) - (V_{IN}^-)) \times ((V_{GAIN}^+) - (V_{GAIN}^-)) + (V_{REF} - V_{FB})}{H}$$

or

$$V_{OUT} = \frac{(V_{IN} \times V_{GAIN} + V_{REF})}{H}$$

Thus the output is equal to the difference of the $V_{IN}$'s times the difference of $V_{GAIN}$'s and offset by $V_{REF}$, all gained up by the feedback divider ratio. The EL4451 is stable for a direct connection between $V_{OUT}$ and $FB$, and the divider may be used for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the $FB$ terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less. Alternatively, a small capacitor across $R_F$ can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the $FB$ input. It is also practical to place small capacitors across both the feedback and the gain resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10pF capacitors across equal divider resistors for a maximum gain of 4 will dominate parasitic effects and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, for DC offsetting of the output, or it can be used to sum in another signal.

Gain-Control Characteristics
The quantity $V_{GAIN}$ in the above equations is bounded as $0 \leq V_{GAIN} \leq 2$, even though the externally applied voltages exceed this range. Actually, the gain transfer function around 0 and 2V is "soft"; that is, the gain does not clip abruptly below the 0%- $V_{GAIN}$ voltage nor above the 100%- $V_{GAIN}$ level. An overdrive of 0.3V must be applied to $V_{GAIN}$ to obtain truly 0% or 100%.

Because the 0%- or 100%- $V_{GAIN}$ levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied $V_{GAIN}$ range of $-0.5V$ to $+2.5V$ will assure the full numerical span of $0 \leq V_{GAIN} \leq 2$.

The gain control has a small-signal bandwidth equal to the $V_{IN}$ channel bandwidth, and overload recovery resolves in about 20 nsec.

Input Connections
The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or 6" of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.
Applications Information — Contd.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 3V and (V+) − 3V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4451. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6μA maximum DC current, and may be biased anywhere between (V−) + 2.5V and (V+) − 3.5V. The ground pin is connected to the IC’s substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and feedthrough over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4451 works with any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the ground pin are observed (see the Ground Pin section). The supplies should be bypassed close to the device with short leads. 4.7μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4451 increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

\[ P_D = 2 \times V_S \times I_{S,\text{max}} + (V_S - V_O) \times V_O/R_{\text{PAR}} \]

where \( I_{S,\text{max}} \) is the maximum supply current

\( V_S \) is the ± supply voltage (assumed equal)

\( V_O \) is the output voltage

\( R_{\text{PAR}} \) is the parallel of all resistors loading the output

For instance, the EL4451 draws a maximum of 18mA. With light loading, \( R_{\text{PAR}} \rightarrow \infty \) and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given \( P_D \) and other parameters is

\[ V_S,\text{max} = (P_D + V_O^2/R_{\text{PAR}}) / (2I_S + V_O/R_{\text{PAR}}) \]

The maximum dissipation a package can offer is

\[ P_D,\text{max} = (T_J,\text{max} - T_A,\text{max}) / \theta_JA \]

Where \( T_J,\text{max} \) is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

\( T_A,\text{max} \) is the ambient temperature, 70°C for commercial and 85°C for industrial range

\( \theta_JA \) is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded.

Output Loading

The output stage of the EL4451 is very powerful. It typically can source 80mA and sink 120mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads <100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220pF load.
Applications Information — Contd.

Leveling Circuits

Often a variable-gain control is used to normalize an input signal to a standard amplitude from a modest range of possible input amplitude. A good example is in video systems, where an unterminated cable will yield a twice-sized standard video amplitude, and an erroneously twice-terminated cable gives a 2/3-sized input.

Here is a ±6 dB range preamplifier:

**Linearized Leveling Amplifier**

![Diagram of Linearized Leveling Amplifier](image)

In this arrangement, the EL4451 outputs a mixture of the signal routed through the multiplier and the REF terminal. The multiplier port produces the most distortion and needs to handle a fraction of an oversized video input, whereas the REF port is just like an op-amp input summing into the output. Thus, for oversized inputs the gain will be decreased and the majority of the signal is routed through the linear REF terminal. For undersized inputs, the gain is increased and the multiplier's contribution added to the output.

Here are some component values for two designs:

<table>
<thead>
<tr>
<th>Attenuation Ratio</th>
<th>R_F</th>
<th>R_G</th>
<th>R_1</th>
<th>R_2</th>
<th>R_3</th>
<th>-3 dB Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>200Ω</td>
<td>400Ω</td>
<td>300Ω</td>
<td>100Ω</td>
<td>200Ω</td>
<td>47 MHz</td>
</tr>
<tr>
<td>2</td>
<td>400Ω</td>
<td>400Ω</td>
<td>500Ω</td>
<td>100Ω</td>
<td>200Ω</td>
<td>28 MHz</td>
</tr>
</tbody>
</table>

With the higher attenuation ratio, the multiplier sees a smaller input amplitude and distorts less, however the higher output gain reduces circuit bandwidth. As seen in the next curves, the peak differential gain error is 0.47% for the attenuation ratio of 1.5, but only 0.27% with the gain of 2 constants. To maintain bandwidth, an external op amp can be used instead of the R_F - R_G divider to boost the EL4451's output by the attenuation ratio.

Sinewave Oscillators

Generating a stable, low distortion sinewave has long been a difficult task. Because a linear oscillator's output tends to grow or diminish continuously, either a clipping circuit or automatic gain control (AGC) is needed. Clipping circuits generate severe distortion which needs subsequent filtering, and AGC's can be complicated.
Applications Information — Contd.

Here is the EL4451 used as an oscillator with simple AGC:

Low-Distortion Sinewave Oscillator

The oscillation frequency is set by the resonance of a series-tuned circuit, which may be an L-C combination or a crystal. At resonance, the series impedance of the tuned circuit drops and its phase lag is 0°, so the EL4451 needs a gain just over unity to sustain oscillation. The $V_{\text{GAIN}}^-$ terminal is initially at $-0.7V$ and the $V_{\text{GAIN}}^+$ terminal at about $+2.1V$, setting the maximum gain in the EL4451. At such high gain, the loop oscillates and output amplitude grows until $D_1$ rectifies more positive voltage at $V_{\text{GAIN}}^-$, ultimately reducing gain until a stable 0.5Vrms output is produced.

Using a 2 MHz crystal, output distortion was $-53\,\text{dBc}$, or 0.22%. Sideband modulation was only 14 Hz wide at $-90\,\text{dBc}$, limited by the filter of the spectrum analyzer used.

The circuit works up to 30 MHz. A parallel-tuned circuit can replace the 510Ω resistor and the 510Ω resistor moved in place of the series-tuned element to allow grounding of the tuned components.

Filters

The EL4451 can be connected to act as a voltage-variable integrator as shown:

EL4451 Connected As Variable Integrator

The input RC cancels a zero produced by the output op-amp feedback connection at $\omega = 1/RC$. With the input RC connected $V_{\text{OUT}}/V_{\text{IN}} = 1/sRC$; without it $V_{\text{OUT}}/V_{\text{IN}} = (1 + sRC)/sRC$. This variable integrator may be used in networks such as the Bi-quad. In some applications the input RC may be omitted. If a negative gain is required, the $V_{\text{IN}}^+$ and $V_{\text{IN}}^-$ terminals can be exchanged.
Applications Information — Contd.
A voltage-controlled equalizer and cable driver can be constructed so:

Equalization and Line Driver Amplifier

The main signal path is via the REF pin. This ensures maximum signal linearity, while the multiplier input is used to allow a variable amount of frequency-shaped input from \( R_1 \), \( R_2 \), and \( C \). For optimum linearity, the multiplier input is attenuated by \( R_1 \) and \( R_2 \). This may not be necessary, depending on input signal amplitude, and \( R_1 \) might be set to 0. \( R_1 \) and \( R_2 \) should be set to provide sufficient peaking, depending on cable high-frequency losses, at maximum gain. \( R_F \) and \( R_G \) are chosen to provide the desired circuit gain, including backmatch resistor loss.
**Features**
- Complete variable-gain amplifier complete with output amplifier
- Compensated for Gain ≥ 10
- 50 MHz signal bandwidth
- 50 MHz gain-control bandwidth
- Low 29 nV/√Hz input noise
- Operates on ±5V to ±15V supplies
- All inputs are differential
- >70 dB attenuation @ 5 MHz

**Applications**
- AGC variable-gain amplifier
- IF amplifier
- Transducer amplifier

**General Description**
The EL4452 is a complete variable-gain circuit. It offers wide bandwidth and excellent linearity, while including a powerful output voltage amplifier, drawing modest current. The higher gain and lower input noise makes the EL4452 ideal for use in AGC systems.

The EL4452 operates on ±5V to ±15V and has an analog input range of ±0.5V. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of −40°C to +85°C and is packaged in 14-pin P-DIP and SO-14.

The EL4452 is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

**Connection Diagram**
**Absolute Maximum Ratings** \( (T_A = 25°C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_+ )</td>
<td>Positive Supply Voltage</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_S )</td>
<td>( V_+ ) to ( V_- ) -- Supply Voltage</td>
<td>33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Voltage at any Input or Feedback</td>
<td>( V_+ ) to ( V_- )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{IN} )</td>
<td>Difference between Pairs of Inputs or Feedback</td>
<td>6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

**Test Procedure**
- I: 100% production tested and QA sample tested per QA test plan QCX0002.
- II: 100% production tested at \( T_A = 25°C \) and QA sample tested at \( T_A = 25°C \), \( T_{MAX} \) and \( T_{MIN} \) per QA test plan QCX0002.
- III: QA sample tested per QA test plan QCX0002.
- IV: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- V: Parameter is typical value at \( T_A = 25°C \) for information purposes only.

**Open-Loop DC Electrical Characteristics**

Power supplies at \( \pm 5V, T_A = 25°C, R_F = 910\Omega, R_G = 100\Omega, R_L = 500\Omega \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DIFF} )</td>
<td>Signal Input Differential Input Voltage - Clipping ( 0.6% ) Nonlinearity</td>
<td>0.4</td>
<td>0.5</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Common-Mode Range (All Inputs; ( V_{DIFF} = 0 ))</td>
<td>( V_S = \pm 5V )</td>
<td>( V_S = \pm 15V )</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>10</td>
<td></td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OS, FB} )</td>
<td>Output Offset Voltage</td>
<td>10</td>
<td></td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( V_G, 100% )</td>
<td>Extrapolated Voltage for 100% Gain</td>
<td>1.8</td>
<td>2.1</td>
<td>2.2</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_G, 0% )</td>
<td>Extrapolated Voltage for 0% Gain</td>
<td>0.16</td>
<td>0.06</td>
<td>0.04</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{G, 1V} )</td>
<td>Gain at ( V_{GAIN} = 1 ) ( (R_F = 910\Omega, R_G = 100\Omega) )</td>
<td>4.9</td>
<td>5.35</td>
<td>5.9</td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current (All Inputs)</td>
<td>0.5</td>
<td></td>
<td></td>
<td>I</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current Between ( V_{IN+, V_{IN-}, V_{GAIN+, V_{GAIN-}} } )</td>
<td>0.5</td>
<td>4</td>
<td></td>
<td>I</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( F_T )</td>
<td>Signal Feedthrough, ( V_G = -1V )</td>
<td>0</td>
<td>-100</td>
<td>-70</td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>( R_{IN, Signal} )</td>
<td>Input Resistance, Signal Input</td>
<td>25</td>
<td>60</td>
<td></td>
<td>I</td>
<td>k( \Omega )</td>
</tr>
<tr>
<td>( R_{IN, Gain} )</td>
<td>Input Resistance, Gain Input</td>
<td>50</td>
<td>120</td>
<td></td>
<td>I</td>
<td>k( \Omega )</td>
</tr>
<tr>
<td>( R_{IN, FB} )</td>
<td>Input Resistance, Feedback</td>
<td>25</td>
<td>60</td>
<td></td>
<td>V</td>
<td>k( \Omega )</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio, ( V_{IN} )</td>
<td>70</td>
<td>90</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
</tbody>
</table>
Open-Loop DC Electrical Characteristics — Contd.
Power supplies at ±5V, T_A = 25°C, R_P = 910Ω, R_G = 100Ω, R_L = 500Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSRR</td>
<td>Power-Supply Rejection Ratio, V_OS, FB; Supplies from ±5V to ±15V</td>
<td>65</td>
<td>83</td>
<td></td>
<td>1</td>
<td>dB</td>
</tr>
<tr>
<td>E_G</td>
<td>Gain Error, Excluding Feedback Resistors, V_GAIN = 2.5V</td>
<td>-7</td>
<td>+7</td>
<td></td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>NL</td>
<td>Nonlinearity, V_IN from -0.25V to +0.25, V_GAIN = 1V</td>
<td>0.3</td>
<td>0.6</td>
<td></td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>V_O</td>
<td>Output Voltage Swing</td>
<td>V_S = ±5V</td>
<td>±2.5</td>
<td>±2.8</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_IN = 0, V_REF Varied)</td>
<td>V_S = ±15V</td>
<td>±12.5</td>
<td>±12.8</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>I_SC</td>
<td>Output Short-Circuit Current</td>
<td>40</td>
<td>85</td>
<td></td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>I_S</td>
<td>Supply Current, V_S = ±15V</td>
<td>15.5</td>
<td>18</td>
<td></td>
<td>1</td>
<td>mA</td>
</tr>
</tbody>
</table>

Closed-Loop AC Electrical Characteristics
Power supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15pF

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW, -3dB</td>
<td>-3dB Small-Signal Bandwidth, Signal Input</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>BW, ±0.1dB</td>
<td>0.1dB Flatness Bandwidth, Signal Input</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>Peaking</td>
<td>Frequency Response Peaking</td>
<td>0.1</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>BW, Gain</td>
<td>-3dB Small-Signal Bandwidth, Gain Input</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate, V_OUT between -2V and +2V</td>
<td>350</td>
<td>400</td>
<td>550</td>
<td>I</td>
<td>V/μs</td>
</tr>
<tr>
<td>V_N</td>
<td>Input-Referred Noise Voltage Density</td>
<td>29</td>
<td></td>
<td></td>
<td>V</td>
<td>nV/rt-Hz</td>
</tr>
</tbody>
</table>

Test Circuit

Note: For typical performance curves, R_P = 910Ω, R_G = 100Ω, V_GAIN = 1V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.
Typical Performance Curves

Frequency Response for Various Feedback Divider Ratios

- $A_V = 10$, $V_S = \pm 15V$, $V_S = \pm 5V$
- $A_V = 50$
- $A_V = 20$
- $R_L = 500\Omega$
- $C_L = 8\ pF$

Frequency Response for Various Gains

- $R_L$, $C_L$, $V_S = \pm 15V$
- $R_L = 150\Omega$
- $C_L = 8\ pF$
- $R_L = 500\Omega$
- $C_L = 86\ pF$

Frequency Response for Various $R_L$, $C_L$, $V_S = \pm 5V$

- $R_L = 500\Omega$
- $C_L = 41\ pF$
- $R_L = 150\Omega$
- $C_L = 8\ pF$

-3 dB Bandwidth vs Supply Voltage

- $R_L = 500\Omega$
- $C_L = 8\ pF$

-3 dB Bandwidth vs Die Temperature

- $V_S = \pm 5V$
- $V_S = \pm 15V$

- $R_L = 500\Omega$
- $C_L = 8\ pF$
Typical Performance Curves — Contd.

Gain and -3 dB Bandwidth vs Load Resistance

Input Common-Mode Rejection Ratio vs Frequency

Slew Rate vs Supply Voltage

Slew Rate vs Die Temperature

Input Voltage Noise vs Frequency

Nonlinearity vs Input Signal
Typical Performance Curves — Contd.

**Bias Current vs Die Temperature**

- $V_S = \pm 5V$
- $V_S = \pm 15V$

**Gain vs $V_{GAIN}$**

**Change in $V_{G,100\%}$ and $V_{G,0\%}$ vs Die Temperature**

**$V_{G,0\%}$ and $V_{G,100\%}$ vs Supply Voltage**

**Common Mode Input Range vs Supply Voltage**

- $-V_{CM}$
- $+V_{CM}$

**Supply Current vs Supply Voltage**

- $T_A = 25^\circ C$
- Die Temperature = $150^\circ C$
Applications Information

The EL4452 is a complete two-quadrant multiplier/gain control with 50 MHz bandwidth. It has three sets of inputs; a differential signal input \( V_{IN} \), a differential gain-controlling input \( V_{GAIN} \), and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:

The gain of the feedback divider is \( H \). The transfer function of the part is

\[
V_{OUT} = A_0 \times ((V_{IN}^+) - (V_{IN}^-)) \times ((V_{GAIN}^+) - (V_{GAIN}^-)) + (V_{REF} - V_{FB})
\]

\( V_{FB} \) is connected to \( V_{OUT} \) through a feedback network, so \( V_{FB} = H \times V_{OUT} \). \( A_0 \) is the open-loop gain of the amplifier, and is approximately 3300. The large value of \( A_0 \) drives

\[
(V_{IN}^+) - (V_{IN}^-) \times \frac{1}{2} (V_{GAIN}^+) - (V_{GAIN}^-) + (V_{REF} - V_{FB}) \to 0.
\]

Rearranging and substituting for \( V_{FB} \)

\[
V_{OUT} = \frac{(V_{IN}^+) - (V_{IN}^-) \times \frac{1}{2} (V_{GAIN}^+) - (V_{GAIN}^-) + V_{REF}}{H}
\]

or

\[
V_{OUT} = (V_{IN} \times \frac{1}{2} V_{GAIN} + V_{REF})/H
\]
Applications Information — Contd.

Thus the output is equal to the difference of the VIN's times the difference of VGAIN's and offset by VREF, all gained up by the feedback divider ratio. The EL4452 is stable for a divider ratio of \( Y \leq 10 \) and the divider may be set for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 130 MHz; typical strays of 3 pF thus require a feedback impedance of 400Ω or less. Alternatively, a small capacitor across RF can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. For instance, a 3 pF capacitor across RF and 27 pF to ground will dominate parasitic effects in a \( \frac{1}{10} \) divider and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, for DC offsetting of the output, or it can be used to sum in another signal.

Gain-Control Characteristics

The quantity VGAIN in the above equations is bounded as \( 0 \leq VGAIN \leq 2 \), even though the externally applied voltages exceed this range. Actually, the gain transfer function around 0 and 2V is "soft"; that is, the gain does not clip abruptly below the 0%-VGAIN voltage nor above the 100%-VGAIN level. An overdrive of 0.3V must be applied to VGAIN to obtain truly 0% or 100%. Because the 0%- or 100%- VGAIN levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied VGAIN range of −0.5V to +2.5V will assure the full numerical span of \( 0 \leq VGAIN \leq 2 \).

The gain control has a small-signal bandwidth equal to the VIN channel bandwidth, and overload recovery resolves in about 20 nsec.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or 6" of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between \( (V-) + 2.5V \) and \( (V+) - 2.5V \) to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±0.5V in the EL4452. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 µA maximum DC current, and may be biased anywhere between \( (V-) + 2.5V \) and \( (V+) - 3.5V \). The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and feedthrough over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4452 operates with power supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the ground pin are observed (see the Ground Pin section). The supplies should be bypassed close to the device with short leads. 4.7 µF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 µF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V- to ground. The inputs...
Applications Information — Contd.
and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4452 increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

\[ P_D = 2 \times V_S \times I_S \text{ max} + (V_S - V_O) \times V_O / R_{PAR} \]

where \( I_S \text{ max} \) is the maximum supply current
\( V_S \) is the ± supply voltage (assumed equal)
\( V_O \) is the output voltage
\( R_{PAR} \) is the parallel of all resistors loading the output

For instance, the EL4452 draws a maximum of 18mA. With light loading, \( R_{PAR} \rightarrow \infty \) and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given \( P_D \) and other parameters is

\[ V_S \text{ max} = (P_D + V_O^2 / R_{PAR}) / (2I_S + V_O / R_{PAR}) \]

The maximum dissipation a package can offer is

\[ P_D \text{ max} = (T_J \text{ max} - T_A \text{ max}) / \theta_{JA} \]

Where \( T_J \text{ max} \) is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance
\( T_A \text{ max} \) is the ambient temperature, 70°C for commercial and 85°C for industrial range
\( \theta_{JA} \) is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded.

Output Loading
The output stage of the EL4452 is very powerful. It can typically source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to a 100Ω load. Heavy resistive loading will degrade frequency response and distortion for loads <100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 1 dB with even a 220 pF load.

AGC Circuits
The basic AGC (automatic gain control) loop is this:

A multiplier scales the input signal and provides necessary gain and buffers the signal presented to the output load, a level detector (shown schematically here as a diode) converts some measure of the output signal amplitude to a DC level, a low-pass filter attenuates any signal ripple present on that DC level, and an amplifier compares that level to a reference and amplifies the error to create a gain-control voltage for the multiplier. The circuitry is a servo that attempts to keep the output amplitude constant by continuously adjusting the multiplier's gain control input.
**Applications Information — Contd.**

Most AGC’s deal with repetitive input signals that are capacitively coupled. It is generally desirable to keep DC offsets from mixing with AC signals and fooling the level detector into maintaining the DC output offset level constant, rather than a smaller AC component. To that end, either the level detector is AC-coupled, or the reference voltage must be made greater than the maximum multiplier gain times the input offset. For instance, if the level detector output equaled the reference voltage at 1V of EL4452 output, the 8 mV of input offset would require a maximum gain of 125 through the EL4452. Bias current-induced offsets could increase this further.

Depending on the nature of the signal, different level detector strategies will be employed. If the system goal is to prevent overload of subsequent stages, peak detectors are preferred. Other strategies use an RMS detector to maintain constant output power. Here is a simple AGC using peak detection:

---

![Diagram of AGC circuit using peak detection]
Applications Information — Contd.

The output of the EL4452 drives a diode detector which is compared to V\_REF by an offset integrator. Its output feeds the gain-control input of the EL4452. The integrator's output is attenuated by the 2 k\(\Omega\) and 2.7 k\(\Omega\) resistors to prevent the op-amp from overloading the gain-control pin during zero input conditions. The 510 k\(\Omega\) resistor provides a pull-down current to the peak level storage capacitor C\textsubscript{1} to allow it to drift negative when output amplitude reduces. Thus the detector is of fast attack and slow decay design, able to reduce AGC gain rapidly when signal amplitude suddenly increases, and increases gain slowly when the input drops out momentarily. The value of C\textsubscript{1} determines drop-out reaction rates, and the value of C\textsubscript{F} affects overall loop time constant as well as the amount of ripple on the gain-control line. C\textsubscript{2} can be used to reduce this ripple further, although it contributes to loop overshoot when input amplitude changes suddenly. The op-amp can be any inexpensive low-frequency type.

The major problem with diode detectors is their large and variable forward voltage. They require at least a 2 V\textsubscript{P-P} peak output signal to function reliably, and the forward voltage should be compensated by including a negative V\textsubscript{D} added to V\_REF. Even this is only moderately successful. At the expense of bandwidth, op-amp circuits can greatly improve diode rectifiers (see "An Improved Peak Detector", an Elantec application note). Fortunately, the detector will see a constant amplitude of signal if the AGC is operating correctly.

A better-calibrated method is to use a four-quadrant multiplier as a square-law detector. Here is a circuit employing the EL4450:
Applications Information — Contd.
In this circuit, the EL4450 not only calculates the square of the input, but also provides the offset integrator function. The product of the two multiplier inputs adds to the \(-\text{Reference} \) input and are passed to the output amplifier, which through \( C_F \) behaves as a pseudo-integrator. The “integrator” gain does not pass through zero at high frequencies but has a zero at \( 1/(2\pi C_F \times 1 \text{ k}\Omega) \). This zero is cancelled by the pole caused by the second capacitor of value \( C_F \) connected at the EL4452 \(-V_{\text{GAIN}} \) input. The \(-\text{Reference} \) can be exchanged for a positive reference by connecting it to the ground return of the 1 kΩ resistor at the FB terminal and grounding REF.

As a general consideration, the input signal applied to an EL4452 should be kept below about 250 mV peak for good linearity. If the AGC were designed to produce a 1V peak output, the input range would be 100 mV–250 mV peak when the EL4452 has a feedback network that establishes a maximum gain of 10. This is an input range of only 2.5:1 for precise output regulation. Raising the maximum gain to 25 allows a 40 mV–250 mV input range with the output still regulated, better than 6:1. Unfortunately, the bandwidth will be reduced. Bandwidth can be maintained by adding a high frequency op-amp cascaded with the output to make up gain beyond the 10 of the EL4452, current feedback devices being the most flexible. The op-amp’s input should be capacitor coupled to prevent gained-up offsets from confusing the level detector during AGC control line variations.
Application Specific Video

Élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
### Video Fader/Variable Gain Amplifiers

Listed by decreasing bandwidth. All use supplies up to ±16V.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Bandwidth</th>
<th>Diff Gain</th>
<th>Diff Phase</th>
<th>Is at 15V</th>
<th>Input Volts Full Scale</th>
<th>Slew Rate</th>
<th>Input Bias IB</th>
<th>VOS</th>
<th>Supply Volts Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>-3 dB</td>
<td>Typ</td>
<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td></td>
</tr>
<tr>
<td>EL4453C</td>
<td>Diff Inputs</td>
<td>80 MHz</td>
<td>0.05%</td>
<td>0.05°</td>
<td>21 mA</td>
<td>±2V</td>
<td>380V/μs</td>
<td>20 μA</td>
<td>25 mV</td>
<td>±4.5V ±16V</td>
<td>14P-N-S</td>
</tr>
<tr>
<td>EL4094C</td>
<td>Only ±In's</td>
<td>60 MHz</td>
<td>0.02%</td>
<td>0.04°</td>
<td>19 mA</td>
<td>±2V</td>
<td>500V/μs</td>
<td>10 μA</td>
<td>20 mV</td>
<td>±4.5V ±16V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL4095C</td>
<td>Logic/Diff In</td>
<td>60 MHz</td>
<td>0.02%</td>
<td>0.02°</td>
<td>21 mA</td>
<td>±2V</td>
<td>330V/μs</td>
<td>10 μA/30 μA</td>
<td>5 mV</td>
<td>±4.5V ±16V</td>
<td>14P-N-S</td>
</tr>
</tbody>
</table>

### Video/RGB DC-Restored Sample and Hold Amplifiers

**Current Mode Feedback Amplifiers**

Listed by decreasing bandwidth. Specs at 25°C and at bold $V_S$.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Includes</th>
<th>Bandwidth</th>
<th>Diff Gain</th>
<th>Diff Phase</th>
<th>Is at $V_S$</th>
<th>AVOL*</th>
<th>Slew Rate</th>
<th>Sample to Hold Delay</th>
<th>IOUT 100Ω Load</th>
<th>VOS</th>
<th>Supply Volts Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>-3 dB</td>
<td>Typ</td>
<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td></td>
</tr>
<tr>
<td>EL4093C</td>
<td>Wide BW</td>
<td>Video S and H</td>
<td>300 MHz</td>
<td>0.04%</td>
<td>0.02°</td>
<td>11.5 mA</td>
<td>533V/V</td>
<td>1500V/μs</td>
<td>15 ns</td>
<td>60 mA</td>
<td>1.5 mV</td>
<td>±4V ±6V</td>
<td>16P-N-S</td>
</tr>
<tr>
<td>EL2090C</td>
<td>High Performance</td>
<td>Video S and H</td>
<td>100 MHz</td>
<td>0.01%</td>
<td>0.02°</td>
<td>17 mA</td>
<td>1000V/V</td>
<td>600V/μs</td>
<td>20 ns</td>
<td>50 mA</td>
<td>10 mV</td>
<td>±4V ±15V</td>
<td>14P-N-S</td>
</tr>
<tr>
<td>EL4089C</td>
<td>Low Cost + In Clamp</td>
<td>Video Clamp</td>
<td>60 MHz</td>
<td>0.02%</td>
<td>0.05°</td>
<td>11 mA</td>
<td>2667V/V</td>
<td>500V/μs</td>
<td>25 ns</td>
<td>54 mA</td>
<td>7 mV</td>
<td>±4V ±15V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL4390C</td>
<td>3 Amps + In Clamp</td>
<td>RGB Clamp</td>
<td>95 MHz</td>
<td>0.02%</td>
<td>0.03°</td>
<td>32 mA</td>
<td>169V/V</td>
<td>800V/μs</td>
<td>35 ns</td>
<td>45 mA</td>
<td>35 mV</td>
<td>±4V ±15V</td>
<td>16P-N-M</td>
</tr>
</tbody>
</table>

*Derived from: $AVOL \approx R_{OL}/(R_F + (-R_{IN} \ast AV))$
## Video Horizontal Genlock

<table>
<thead>
<tr>
<th>Part #</th>
<th>Pal Frequency Divisors</th>
<th>NTSC Frequency Divisors</th>
<th>Logic Levels</th>
<th>Vco Control</th>
<th>IDD</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Clocks per Horizontal Line</td>
<td>Clocks per Horizontal Line</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL4584C</td>
<td>3 Fsc</td>
<td>CCIR 601</td>
<td>Square Pixels</td>
<td>4 Fsc</td>
<td>3 Fsc</td>
<td>CCIR 601</td>
</tr>
<tr>
<td></td>
<td>851</td>
<td>864</td>
<td>944</td>
<td>1135</td>
<td>682</td>
<td>858</td>
</tr>
<tr>
<td>6 Fsc</td>
<td>851</td>
<td>864</td>
<td>944</td>
<td>1135</td>
<td>682</td>
<td>858</td>
</tr>
<tr>
<td>EL4585C</td>
<td>1702</td>
<td>1728</td>
<td>1888</td>
<td>2270</td>
<td>1364</td>
<td>1716</td>
</tr>
</tbody>
</table>

## Video Sync Separators

- NTSC, PAL, SECAM and Non Standard Video Sync Separation.
- External Resistor Sets Internal Timing for Scan Rate.
- Composite Video Input with Video Sync Tip Reference Clamp.
- Input Levels from 0.5 Vp-p to 2 Vp-p.
- Single 5V Supply Low Power.
- Default Vertical Sync.
- Composite Sync Output.
- Vertical Sync Output.
- Odd/Even Field Output.
- Burst/Back Porch Output.
- Outputs TTL/CMOS Levels.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Sync Slicing Point from Sync Ref Tip</th>
<th>Color Burst Filter</th>
<th>Prop Delay In to CSync</th>
<th>IDD at 5V</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Typ</td>
<td>Max</td>
<td>P = Pins</td>
</tr>
<tr>
<td>EL1881C</td>
<td>Low Cost</td>
<td>70 mV</td>
<td>External</td>
<td>45 ns</td>
<td>3 mA</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL1882C</td>
<td>50% Slicing</td>
<td>50% w/AGC</td>
<td>External</td>
<td>25 ns</td>
<td>3 mA</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL4581C</td>
<td>50% + Video Filter</td>
<td>50% w/S and H</td>
<td>3 Pole Internal</td>
<td>260 ns</td>
<td>3 mA</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL4583C</td>
<td>Multi Featured</td>
<td>50% w/S and H</td>
<td>3 Pole Internal</td>
<td>250 ns</td>
<td>4 mA</td>
<td>16P-N-S</td>
</tr>
</tbody>
</table>

*Filter input, filter output, resistor set color burst filter frequency, horizontal sync output, no sync pulse detected output, sync pulse level output, resistor sets no sync pulse detect level.
Multipliers/Variable Gain Amps, Voltage Mode Input

Wide Bandwidth/Video with Voltage Mode Feedback
Listed by decreasing bandwidth. Up to ±15V supplies.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Bandwidth -3 dB</th>
<th>Input Volts Full Scale</th>
<th>Linearity</th>
<th>Linear</th>
<th>Diff. Gain</th>
<th>Diff. Phase</th>
<th>Slew Rate</th>
<th>Input Vos</th>
<th>Input Bias</th>
<th>I_B</th>
<th>Supply Volts Range</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typ Typ Typ Typ Typ Typ Typ Max Max Max Min Max</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL4450C</td>
<td>4 Quadrant</td>
<td>90 MHz ±2V 0.3% 0.2% — —</td>
<td>400V/μs 35 mV 20 μA 18 mA ±4.5V ±16V 14P-N-S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL4451C</td>
<td>2 Quad Leveler</td>
<td>70 MHz ±2V 0.2% 2% 0.9% 0.2°</td>
<td>400V/μs 25 mV 20 μA 18 mA ±4.5V ±16V 14P-N-S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL4452C</td>
<td>2 Quad High Gain</td>
<td>50 MHz ±0.5V 0.3% 2% — —</td>
<td>400V/μs 10 mV 20 μA 18 mA ±4.5V ±16V 14P-N-S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Multipliers/Variable Gain Amps, Current Mode Input

Wide Bandwidth/Video
Listed by decreasing bandwidth. Up to ±15V supplies.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Bandwidth -3 dB</th>
<th>Linearity, Signal Port</th>
<th>Linearity, Gain Port</th>
<th>Diff. Gain</th>
<th>Diff. Phase</th>
<th>I_B</th>
<th>Supply Volts Range</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typ Typ Typ Typ Typ Typ Max Max</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL4083C</td>
<td>4 Quadrant</td>
<td>225 MHz 0.1% 0.1% 0.1% 0.05°</td>
<td>48 mA ±4.5V ±16V 8P-N-S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2082C</td>
<td>2 Quadrant</td>
<td>150 MHz 0.1% 2% 0.25% 0.05°</td>
<td>16 mA ±4.5V ±16V 8P-N-S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Features

- NTSC, PAL, SECAM, non-standard video sync separation
- Fixed 70 mV slicing of video input levels from 0.5 V_p_p to 2 V_p_p
- Low supply current - 1.5 mA typ.
- Single +5V supply
- Composite, vertical sync output
- Odd/Even field output
- Burst/Back porch output
- Plug-in compatible with industry standard LM1881 in 5V applications
- Available in 8-pin DIP and SO package

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

General Description

The EL1881C video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input. It provides composite sync, vertical sync, burst/back porch timing and odd/even field detection. Fixed 70 mV sync tip slicing provides sync edge detection when the video input level is between 0.5 V_p_p and 2 V_p_p (sync tip amplitude 143 mV to 572 mV). A single external resistor sets all internal timing to adjust for various video standards. The composite sync output follows video in sync pulses, and a vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The odd/even output indicates field polarity detected during the vertical blanking interval. The EL1881C is plug-in compatible with the industry standard LM1881 and can be substituted for that part in 5V applications with lower required supply current.

Connection Diagram

![Connection Diagram](image-url)
### Absolute Maximum Ratings \((T_A = 25\degree C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Supply</td>
<td>7V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65\degree C to +150\degree C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (5 sec)</td>
<td>260\degree C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin Voltages</td>
<td>-0.5V to VCC + 0.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Operating Ambient Temperature Range** \(-40\degree C to +85\degree C\)

**Operating Junction Temperature** 125\degree C

**Power Dissipation** 400 mW

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series System. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

### Test Level

<table>
<thead>
<tr>
<th>Test Procedure</th>
<th>Test Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>I 100% production tested and QA sample tested per QA test plan QCX0002.</td>
<td>I</td>
</tr>
<tr>
<td>II 100% production tested at (T_A = 25\degree C) and QA sample tested at (T_A = 25\degree C), (T_{MAX}) and (T_{MIN}) per QA test plan QCX0002.</td>
<td>I</td>
</tr>
<tr>
<td>III QA sample tested per QA test plan QCX0002.</td>
<td>I</td>
</tr>
<tr>
<td>IV Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
<td>IV</td>
</tr>
<tr>
<td>V Parameter is typical value at (T_A = 25\degree C) for information purposes only.</td>
<td>I</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics

Unless otherwise stated, \(V_{DD} = 5V, T_A = 25\degree C, R_{SET} = 681 \text{ k}\Omega\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{DD}), Quiescent</td>
<td>(V_{DD} = 5V)</td>
<td>0.75</td>
<td>1.5</td>
<td>3.0</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Clamp Voltage</td>
<td>Pin 2, Unloaded</td>
<td>1.35</td>
<td>1.5</td>
<td>1.65</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Clamp Discharge Current</td>
<td>Pin 2 = 2V</td>
<td>3.2</td>
<td>12</td>
<td>16</td>
<td>I</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>Clamp Charge Current</td>
<td>Pin 2 = 1V</td>
<td>-2.0</td>
<td>-1.5</td>
<td>-0.8</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(R_{SET}) Pin Reference Voltage</td>
<td>Pin 6</td>
<td>1.20</td>
<td>1.31</td>
<td>1.44</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OL}), Output Low Voltage</td>
<td>(I_{OL} = 1.6 \text{ mA})</td>
<td>0.4</td>
<td>0.8</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OH}), Output High Voltage</td>
<td>(I_{OH} = -40 \mu)A</td>
<td>4</td>
<td>4.8</td>
<td></td>
<td>IV</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(I_{OH} = -1.6 \text{ mA})</td>
<td>2.4</td>
<td>3.5</td>
<td></td>
<td>I</td>
<td></td>
</tr>
</tbody>
</table>

### Dynamic Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comp Sync Prop Delay, (t_{CS})</td>
<td>See Figure 2</td>
<td>20</td>
<td>45</td>
<td>90</td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>Vertical Sync Width, (t_{VS})</td>
<td>Normal or Default trigger, 50%-50%</td>
<td>190</td>
<td>270</td>
<td>350</td>
<td>I</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>Vertical Sync Delay, (t_{VSD})</td>
<td>See Figure 3</td>
<td>35</td>
<td>65</td>
<td>85</td>
<td>I</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>Burst/Back Porch Delay, (t_{BD})</td>
<td>See Figure 2</td>
<td>250</td>
<td>450</td>
<td>650</td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>Burst/Back Porch Width, (t_{B})</td>
<td>See Figure 2</td>
<td>2.5</td>
<td>3.6</td>
<td>4.5</td>
<td>I</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>Input Dynamic Range</td>
<td>Video input amplitude to maintain 50% slice spec</td>
<td>0.5</td>
<td>2</td>
<td></td>
<td>I</td>
<td>(V_{P-P})</td>
</tr>
<tr>
<td>Slice Level</td>
<td>(V_{SLICE}/V_{CLAMP})</td>
<td>55</td>
<td>70</td>
<td>85</td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>
Pin Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Composite Sync Out</td>
<td>Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.</td>
</tr>
<tr>
<td>2</td>
<td>Composite Video In</td>
<td>AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).</td>
</tr>
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<td>3</td>
<td>Vertical Sync Out</td>
<td>Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.</td>
</tr>
<tr>
<td>4</td>
<td>Gnd</td>
<td>Supply ground.</td>
</tr>
<tr>
<td>5</td>
<td>Burst/Back Porch Output</td>
<td>Burst/Back porch output. Low during burst portion of composite video.</td>
</tr>
<tr>
<td>6</td>
<td>RSET</td>
<td>An external resistor to ground sets all internal timing. A 681k 1% resistor will provide correct timing for NTSC signals.</td>
</tr>
<tr>
<td>7</td>
<td>Odd/Even Output</td>
<td>Odd/Even field output. High during odd fields, low during even fields. Transitions occur at start of Vert Sync pulse.</td>
</tr>
<tr>
<td>8</td>
<td>VDD 5V</td>
<td>Positive supply. (5V)</td>
</tr>
</tbody>
</table>

Note: RSET must be a 1% resistor.
Typical Performance Curves

Supply Current, Quiescent
\[ R_{SET} = 681k \]

\[ I_D \] vs \[ V_{DD} \]
\[ R_{SET} = 681k \]

\[ V_{CLAMP} \] Voltage
\[ R_{SET} = 681k \]

\[ V_{RSET} \]
\[ R_{SET} = 681k \]

\[ I_{CHARGE} \] vs \[ V_{DD} \]
\[ R_{SET} = 681k \]
Typical Performance Curves — Contd.

**RSET vs Horizontal Frequency**

- **Burst/Back Porch Width vs RSET**
  - $V_{DD} = 5V$, $T = 25^\circ C$

- **Burst/Back Porch Delay vs RSET**
  - $V_{DD} = 5V$, $T = 25^\circ C$

- **Vertical Sync Width vs RSET**
  - $V_{DD} = 5V$, $T = 25^\circ C$

- **Vertical Default Delay vs RSET**
  - $V_{DD} = 5V$, $T = 25^\circ C$
Typical Performance Curves — Contd.

- **Composite Sync Prop Delay**
  - $R_{SET} = 681k$, $V_{DD} = 5V$

- **Burst/Back Porch Width**
  - $R_{SET} = 681k$

- **Burst/Back Porch Delay Time**
  - $R_{SET} = 681k$

- **Vertical Sync Pulse Width**
  - $R_{SET} = 681k$

- **Vertical Sync Default Delay Time**
  - $R_{SET} = 681k$

- **Composite Sync to Vertical Sync Delay Time**
  - $R_{SET} = 681k$

- **Composite Sync to Odd/Even Delay Time**
  - $R_{SET} = 681k$
Timing Diagrams

**Figure 1. Standard (NTSC Input) Timing**

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.
Expanded Timing Diagrams

**Figure 2. Standard Vertical Timing**

**Figure 3. Non-Standard Vertical Timing**

Figure 4. Standard (NTSC Input) H. Sync Detail
Applications Information

Video In
A simplified block diagram is shown following page.

An AC coupled video signal is input to Video In pin 2 via C1, nominally 0.1 μF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1 mA. A clamp discharge current of about 10 μA is always attempting to discharge C1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from \( I = CV \), where \( V \) is the droop voltage, \( I \) is the discharge current, \( T \) is the time between sync pulses (sync period − sync tip width), and \( C \) is C1.

An NTSC video signal has a horizontal frequency of 15.73 kHz, and a sync tip width of 4.7 μs. This gives a period of 63.6 μs and a time \( T = 58.9 \mu s \). The droop voltage will then be \( V = 5.9 \) mV. This is less than 2% of a nominal sync tip amplitude of 286 mV. The charge represented by this droop is replaced in a time given by \( T = CV/I \), where \( I = \) clamp charge current = 1 mA. Here \( T = 590 \) ns, about 12% of the sync pulse width of 4.7 μs. It is important to choose C1 large enough so that the droop voltage does not approach the switching threshold of the internal comparator.

Fixed Gain Buffer
The clamped video signal then passes to the fixed gain buffer which places the sync slice level at the equivalent level of 70 mV above sync tip. The output of this buffer is presented to the comparator, along with the slice reference. The comparator output is level shifted and buffered to TTL levels, and sent out as Composite Sync to pin 1.

Burst
A low-going Burst pulse follows each rising edge of sync, and lasts approximately 3.5 μs for an \( R_{SET} \) of 681 kΩ.

Vertical Sync
A low-going Vertical Sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1881C on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60 μs after the last falling edge of the vertical equalizing phase for \( R_{SET} = 681 \) kΩ.

Odd/Even
Because a typical television picture is composed of two interlaced fields, there is an odd field that includes all the odd lines, and an even field that consists of the even lines. This odd/even field information is decoded by the EL1881C during the end of picture information and the beginning of vertical information. The odd/even circuit includes a T-flip-flop that is reset during full horizontal lines, but not during half lines or vertical equalization pulses. The T-flip-flop is clocked during each falling edge of these half h-period pulses. Even fields will toggle until a low state is clocked to the odd/even pin 7 at the beginning of vertical sync, and odd fields will cause a high state to be clocked to the odd/even pin at the start of the next vertical sync pulse. Odd/even can be ignored if using non-interlaced video, as there is no change in timing from one field to the next.

\( R_{SET} \)
An external \( R_{SET} \) resistor, connected from \( R_{SET} \) pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of \( R_{SET} \) increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower \( R_{SET} \) value.
Applications Information — Contd.

Chroma Filter
A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in Figure 5. It can be implemented very simply and inexpensively with a series resistor of 620Ω and a parallel capacitor of 500 pF, which gives a single pole roll-off frequency of about 500 kHz. This sufficiently attenuates the 3.58 MHz (NTSC) or 4.43 MHz (PAL) color burst signal, yet passes the approximately 15 kHz sync signals without appreciable attenuation. A chroma filter will increase the propagation delay from the composite input to the outputs.

![Figure 5](image)

**Figure 5**

Simplified Block Diagram

![Figure 6](image)

**Figure 6**

* Note: $R_{\text{SET}}$ must be a 1% resistor.
Features
- NTSC, PAL, SECAM, non-standard video sync separation
- Precision 50% slicing of video input levels from 0.5 Vp-p to 2 Vp-p
- Low supply current - 1.5 mA typ.
- Single +5V supply
- Composite, vertical sync output
- Odd/Even field output
- Burst/Back porch output
- Plug-in compatible with industry standard LM1881 in 5V applications
- Available in 8-pin DIP and SO package

Applications
- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

General Description
The EL1882C video sync separator is manufactured using Elantec’s high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input. It provides composite sync, vertical sync, burst/back porch timing and odd/even field detection. 50% sync tip slicing provides precise sync edge detection when the video input level is between 0.5 Vp-p and 2 Vp-p (sync tip amplitude 143 mV to 572 mV). A single external resistor sets all internal timing to adjust for various video standards. The composite sync output follows video in sync pulses, and a vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The odd/even output indicates field polarity detected during the vertical blanking interval. The EL1882C is plug-in compatible with the industry standard LM1881 and can be substituted for that part in 5V applications with improved 50% slicing and lower required supply current.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL1882CN</td>
<td>-40°C to +85°C</td>
<td>8-pin DIP MDP0031</td>
</tr>
<tr>
<td>EL1882CS</td>
<td>-40°C to +85°C</td>
<td>8-lead SO MDP0027</td>
</tr>
</tbody>
</table>

Demo Board
A dedicated demo board is not available. However, this device can be placed on the EL4584/5 demo board.
### Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Supply</td>
<td>7V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (5 sec)</td>
<td>260°C</td>
</tr>
<tr>
<td>Pin Voltages</td>
<td>-0.5V to VCC + 0.5V</td>
</tr>
</tbody>
</table>

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Tj = TC = TA.

Test Level | Test Procedure |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at TA = 25°C and QA sample tested at TA = 25°C.</td>
</tr>
<tr>
<td>III</td>
<td>TMAX and TMIN per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at TA = 25°C for information purposes only.</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics

Unless otherwise stated, VDD = 5V, TA = 25°C, RSET = 680 kΩ

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD, Quiescent</td>
<td>VDD = 5V</td>
<td>0.75</td>
<td>1.5</td>
<td>3.0</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Clamp Voltage</td>
<td>Pin 2, Unloaded</td>
<td>1.35</td>
<td>1.5</td>
<td>1.65</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Clamp Discharge Current</td>
<td>Pin 2 = 2V</td>
<td>3.2</td>
<td>12</td>
<td>16</td>
<td>I</td>
<td>µA</td>
</tr>
<tr>
<td>Clamp Charge Current</td>
<td>Pin 2 = 1V</td>
<td>-2.0</td>
<td>-1.5</td>
<td>-0.8</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>RSET Pin Reference Voltage</td>
<td>Pin 6</td>
<td>1.20</td>
<td>1.31</td>
<td>1.40</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>VIL, Output Low Voltage</td>
<td>IOL = 1.6 mA</td>
<td>0.4</td>
<td>0.8</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>VOH Output High Voltage</td>
<td>IOH = -40 µA</td>
<td>4</td>
<td>4.8</td>
<td></td>
<td>IV</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>IOH = -1.6 mA</td>
<td>2.4</td>
<td>3.5</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>

### Dynamic Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comp Sync Prop Delay, tCS</td>
<td>See Figure 2</td>
<td>10</td>
<td>25</td>
<td>40</td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>Vertical Sync Width, tVS</td>
<td>Normal or Default trigger, 50%−50%</td>
<td>190</td>
<td>270</td>
<td>350</td>
<td>I</td>
<td>µs</td>
</tr>
<tr>
<td>Vertical Sync Default Delay, tVSD</td>
<td>See Figure 3</td>
<td>35</td>
<td>65</td>
<td>85</td>
<td>I</td>
<td>µs</td>
</tr>
<tr>
<td>Burst/Back Porch Delay, tBD</td>
<td>See Figure 2</td>
<td>250</td>
<td>450</td>
<td>650</td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>Burst/Back Porch Width, tB</td>
<td>See Figure 2</td>
<td>2.5</td>
<td>3.6</td>
<td>4.5</td>
<td>I</td>
<td>µs</td>
</tr>
<tr>
<td>Input Dynamic Range</td>
<td>Video input amplitude to maintain 50% slice spec</td>
<td>0.5</td>
<td>2</td>
<td></td>
<td>I</td>
<td>Vp,p</td>
</tr>
<tr>
<td>Slice Level</td>
<td>VSLICE/VCLAMP</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>I</td>
<td>%</td>
</tr>
</tbody>
</table>
## Pin Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Composite Sync Out</td>
<td>Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.</td>
</tr>
<tr>
<td>2</td>
<td>Composite Video In</td>
<td>AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).</td>
</tr>
<tr>
<td>3</td>
<td>Vertical Sync Out</td>
<td>Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.</td>
</tr>
<tr>
<td>4</td>
<td>Gnd</td>
<td>Supply ground.</td>
</tr>
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<td>5</td>
<td>Burst/Back Porch Output</td>
<td>Burst/Back porch output. Low during burst portion of composite video.</td>
</tr>
<tr>
<td>6</td>
<td>$R_{SET}$</td>
<td>An external resistor to ground sets all internal timing. A 681k 1% resistor will provide correct timing for NTSC signals.</td>
</tr>
<tr>
<td>7</td>
<td>Odd/Even Output</td>
<td>Odd/Even field output. High during odd fields, low during even fields. Transitions occur at start of Vert Sync pulse.</td>
</tr>
<tr>
<td>8</td>
<td>$V_{DD,5V}$</td>
<td>Positive supply. (5V)</td>
</tr>
</tbody>
</table>

Note: $R_{SET}$ must be a 1% resistor.
Typical Performance Curves

**Supply Current, Quiescent**

\[ I_{DD} \text{ vs } V_{DD} \]

\[ R_{SET} = 681k \]

\[ I_{DD} (mA) \]

\[ 4.5V \]

\[ 5V \]

\[ 5.5V \]

\[ -50 -25 0 25 50 75 100 \]

\[ \text{Temperature (°C)} \]

**V\text{CLAMP Voltage}**

\[ V_{\text{CLAMP}} (V) \]

\[ R_{SET} = 681k \]

\[ 1.49 \]

\[ 1.5 \]

\[ 1.51 \]

\[ 1.52 \]

\[ 1.53 \]

\[ 1.54 \]

\[ 1.55 \]

\[ -50 -25 0 25 50 75 100 \]

\[ \text{Temperature (°C)} \]

**V\text{SET}**

\[ V_{\text{SET}} (V) \]

\[ R_{SET} = 681k \]

\[ 1.290 \]

\[ 1.295 \]

\[ 1.300 \]

\[ 1.305 \]

\[ 1.310 \]

\[ 1.315 \]

\[ 1.320 \]

\[ -50 -25 0 25 50 75 100 \]

\[ \text{Temperature (°C)} \]

**I\text{DD vs V\text{DD}}**

\[ I_{DD} (mA) \]

\[ 4.5V \]

\[ 5V \]

\[ 5.5V \]

\[ -50 -25 0 25 50 75 100 \]

\[ \text{Temperature (°C)} \]

**Clamp Discharge Current**

\[ I_{DS} (\mu A) \]

\[ 4.5V \]

\[ 5V \]

\[ 5.5V \]

\[ 85°C \]

\[ 40°C \]

\[ 25°C \]

\[ -25 -5 25 50 75 100 \]

\[ \text{Temperature (°C)} \]

**Clamp Charge Current**

\[ I_{CH} (mA) \]

\[ 4.5V \]

\[ 5V \]

\[ 5.5V \]

\[ -50 -25 0 25 50 75 100 \]

\[ \text{Temperature (°C)} \]
Typical Performance Curves — Contd.

- **R\(_\text{SET}\) vs Horizontal Frequency**
  - Frequency (kHz) vs \(R\(_\text{SET}\) (kΩ)

- **Burst/Back Porch Width vs \(R\(_\text{SET}\)**
  - V\(_\text{DD}\) = 5V, \(T = 25°C\)
  - Burst Width (μs) vs \(R\(_\text{SET}\) (kΩ)

- **Burst/Back Porch Delay vs \(R\(_\text{SET}\)**
  - V\(_\text{DD}\) = 5V, \(T = 25°C\)
  - Burst Delay (μs) vs \(R\(_\text{SET}\) (kΩ)

- **Vertical Sync Width vs \(R\(_\text{SET}\)**
  - V\(_\text{DD}\) = 5V, \(T = 25°C\)
  - Vertical Sync Width (μs) vs \(R\(_\text{SET}\) (kΩ)

- **Vertical Default Delay vs \(R\(_\text{SET}\)**
  - V\(_\text{DD}\) = 5V, \(T = 25°C\)
  - Vertical Sync Default Delay (μs) vs \(R\(_\text{SET}\) (kΩ)
Typical Performance Curves — Contd.

Composite Sync Prop Delay
$R_{SET} = 681k$, $V_{DD} = 5V$

Burst/Back Porch Width,
$R_{SET} = 681k$

Burst/Back Porch Delay Time,
$R_{SET} = 681k$

Vertical Sync Pulse Width
$R_{SET} = 681k$

Vertical Sync Default Delay Time,
$R_{SET} = 681k$

Composite Sync vs Delay Time
$R_{SET} = 681k$

Composite Sync to Odd/Even Delay Time
$R_{SET} = 681k$
Timing Diagrams

**Figure 1. Standard (NTSC Input) Timing**

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.
Expanded Timing Diagrams

Figure 2. Standard Vertical Timing

Figure 3. Non-Standard Vertical Timing
Figure 4. Standard (NTSC Input) H. Sync Detail
Applications Information

Video In
A simplified block diagram is shown following page.

An AC coupled video signal is input to Video In pin 2 via C1, nominally 0.1 μF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1 mA. A clamp discharge current of about 10 μA is always attempting to discharge C1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period - sync tip width), and C is C1.

An NTSC video signal has a horizontal frequency of 15.73 kHz, and a sync tip width of 4.7 μs. This gives a period of 63.6 μs and a time T = 58.9 μs. The droop voltage will then be V = 5.9 mV. This is less than 2% of a nominal sync tip amplitude of 286 mV. The charge represented by this droop is replaced in a time given by T = CV/I, where I = clamp charge current = 1 mA. Here T = 590 ns, about 12% of the sync pulse width of 4.7 μs. It is important to choose C1 large enough so that the droop voltage does not approach the 50% switching threshold of the internal comparator.

AGC and Composite Sync
The clamped video signal then passes to the AGC, which will maintain the blanking level of its output (sensed during burst) at the blanking reference level. The AGC should therefore present a constant amplitude signal to the comparator, if the input is within the AGC's dynamic range. A 50% slicing reference is compared with the AGC's output at the comp circuit. Comp's output is level shifted and buffered to TTL levels, and sent out as Comp Sync on pin 1.

Burst
A low-going Burst pulse follows each rising edge of sync, and lasts approximately 3.5 μs for an RSET of 681 kΩ. This signal is used internally to gate the AGC feedback for determining blanking level.

Vertical Sync
A low-going Vertical Sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1882C on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60 μs after the last falling edge of the vertical equalizing phase for RSET = 681 kΩ.

Odd/Even
Because a typical television picture is composed of two interlaced fields, there is an odd field that includes all the odd lines, and an even field that consists of the even lines. This odd/even field information is decoded by the EL1882C during the end of picture information and the beginning of vertical information. The odd/even circuit includes a T-flip-flop that is reset during full horizontal lines, but not during half lines or vertical equalization pulses. The T-flip-flop is clocked during each falling edge of these half h-period pulses. Even fields will toggle until a low state is clocked to the odd/even pin 7 at the beginning of vertical sync, and odd fields will cause a high state to be clocked to the odd/even pin at the start of the next vertical sync pulse. Odd/even can be ignored if using non-interlaced video, as there is no change in timing from one field to the next.

RSET
An external RSET resistor, connected from RSET pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of RSET increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower RSET value.
Applications Information — Contd.

Chroma Filter
When the EL1882 is used in composite color systems, a chroma filter is required at the video input. This is so because the color burst signal extends to the 50% point of the sync pulse (−20 IRE). Since the EL1882 slices at the 50% level, a chroma filter is required to attenuate the color burst signal to a point above the 50% level. Without this filter false sync triggering may occur during color burst. An example chroma filter is shown in Figure 5. It can be implemented very simply and inexpensively with a series resistor of 620Ω and a parallel capacitor of 500 pF, which gives a single pole roll-off frequency of about 500 kHz. This sufficiently attenuates the 3.58 MHz (NTSC) or 4.43 MHz (PAL) color burst signal, yet passes the approximately 15 kHz sync signals without appreciable attenuation. A chroma filter will increase the propagation delay from composite sync to outputs.

Simplified Block Diagram

* Note: $R_{SET}$ must be a 1% resistor.
Features

- Flexible inputs and outputs, all ground referred
- 150 MHz large and small-signal bandwidth
- 46 dB of calibrated gain control range
- 70 dB isolation in disable mode @ 10 MHz
- 0.15% diff gain and 0.05° diff phase performance at NTSC using application circuit
- Operates on ±5V to ±15V power supplies
- Outputs may be paralleled to function as a multiplexer

Applications

- Level adjust for video signals
- Video faders and mixers
- Signal routing multiplexers
- Variable active filters
- Video monitor contrast control
- AGC
- Receiver IF gain control
- Modulation/demodulation
- General "cold" front-panel control of AC signals

General Description

The EL2082 is a general purpose variable gain control building block, built using an advanced proprietary complementary bipolar process. It is a two-quadrant multiplier, so that zero or negative control voltages do not allow signal feedthrough and very high attenuation is possible. The EL2082 works in current mode rather than voltage mode, so that the input impedance is low and the output impedance is high. This allows very wide bandwidth for both large and small signals.

The I_in pin replicates the voltage present on the V_IN pin; therefore, the V_IN pin can be used to reject common-mode noise and establish an input ground reference. The gain control input is calibrated to 1 mA/μA signal gain for 1V of control voltage. The disable pin (E) is TTL-compatible, and the output current can comply with a wide range of output voltages.

Because current signals rather than voltages are employed, multiple inputs can be summed and many outputs wire-or'ed or mixed.

The EL2082 operates from a wide range of supplies and is available in standard 8-pin plastic DIP or 8-lead SO.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2082CN</td>
<td>0°C to +75°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2082CS</td>
<td>0°C to +75°C</td>
<td>8-Pin SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagram
## Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>PD</th>
<th>Maximum Power Dissipation</th>
<th>TA</th>
<th>Operating Temperature Range</th>
<th>TJ</th>
<th>Operating Junction Temperature</th>
<th>TSST</th>
<th>Storage Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS</td>
<td>Voltage between VS+ and VS-</td>
<td>+33V</td>
<td>TLOAD</td>
<td>0°C to +75°C</td>
<td>150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN, IOUT</td>
<td>Voltage</td>
<td>± VS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VE, VGAIN</td>
<td>Input Voltage</td>
<td>-1 to +7V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIN</td>
<td>Input Current</td>
<td>± 5 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TD = TC = TA.

### Test Level

| I  | 100% production tested and QA sample tested per QA test plan QCX0002. |
| II | 100% production tested at TA = 25°C and QA sample tested at TA = 25°C. |
| III | QA sample tested per QA test plan QCX0002. |
| IV | Parameter is guaranteed (but not tested) by Design and Characterization Data. |
| V  | Parameter is typical value at TA = 25°C for information purposes only. |

## DC Electrical Characteristics

(VS = ±15V, VG = 1V, VE = 0.8V, VOUT = 0, VIN = 0, IIN = 0)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIO</td>
<td>Input Offset Voltage</td>
<td>Full</td>
<td>-20</td>
<td>20</td>
<td>II</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>IIOO</td>
<td>Output Offset Current</td>
<td>Full</td>
<td>-100</td>
<td>100</td>
<td>II</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>RIN</td>
<td>Input Impedance; IIN = 0, 0.35 mA</td>
<td>Full</td>
<td>75</td>
<td>95</td>
<td>115</td>
<td>II</td>
<td>Ω</td>
</tr>
<tr>
<td>VCMRR</td>
<td>Voltage Common-Mode Rejection Ratio VIN = -10V, +10V</td>
<td>Full</td>
<td>45</td>
<td>55</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>ICMRR</td>
<td>Offset Current Common-Mode Rejection Ratio, VIN = -10V, +10V</td>
<td>Full</td>
<td>0.5</td>
<td>5</td>
<td>II</td>
<td>μA/V</td>
<td></td>
</tr>
<tr>
<td>VPSRR</td>
<td>Offset Voltage Power Supply Rejection Ratio, VS = ±5V to ±15V</td>
<td>Full</td>
<td>60</td>
<td>80</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>IPSRR</td>
<td>Offset Current Power Supply Rejection Ratio, VS = ±5V to ±15V</td>
<td>Full</td>
<td>1</td>
<td>10</td>
<td>II</td>
<td>μA/V</td>
<td></td>
</tr>
<tr>
<td>IBVIN</td>
<td>VIN Bias Current</td>
<td>Full</td>
<td>-10</td>
<td>10</td>
<td>II</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>RINV</td>
<td>VIN Input Impedance; VIN = -10V, +10V</td>
<td>Full</td>
<td>0.5</td>
<td>1.0</td>
<td>II</td>
<td>MΩ</td>
<td></td>
</tr>
<tr>
<td>NLini</td>
<td>Signal Nonlinearity; IIN = -0.7 mA, -0.35 mA, 0 mA, +0.35 mA, +0.7 mA</td>
<td>Full</td>
<td>0.10</td>
<td>0.4</td>
<td>II</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>ROUT</td>
<td>Output Impedance VOUT = -10V, +10V</td>
<td>Full</td>
<td>0.25</td>
<td>0.5</td>
<td>II</td>
<td>MΩ</td>
<td></td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics — Contd.

\( (V_S = \pm 15V, V_G = 1V, V_E = 0.8V, V_{OUT} = 0, V_{IN} = 0, I_{IN} = 0) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OUT} )</td>
<td>Output Swing; ( V_{GAIN} = 2V, I_{IN} \pm 2 mA, R_L = 4.0K )</td>
<td>Full</td>
<td>-11</td>
<td>11</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{IOG} )</td>
<td>( V_{OS}, ) Gain Control, Extrapolated from ( V_{GAIN} = 0.1V, 1V )</td>
<td>Full</td>
<td>-15</td>
<td>15</td>
<td>II</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( A_1 )</td>
<td>Current Gain, ( I_{IN} \pm 350 \mu A )</td>
<td>Full</td>
<td>0.9</td>
<td>1.1</td>
<td>II</td>
<td>mA/mA</td>
<td></td>
</tr>
<tr>
<td>( N_{ling} )</td>
<td>Nonlinearity of Gain Control, ( V_{GAIN} = 0.1V, 0.5V, 1V )</td>
<td>Full</td>
<td>2</td>
<td>5</td>
<td>II</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( I_{SO} )</td>
<td>Input Isolation with ( V_{GAIN} = -0.1V )</td>
<td>Full</td>
<td>-80</td>
<td>-96</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( V_{INH} )</td>
<td>( \bar{E} ) Logic High Level</td>
<td>Full</td>
<td>2.0</td>
<td></td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{INL} )</td>
<td>( \bar{E} ) Logic Low Level</td>
<td>Full</td>
<td>0.8</td>
<td></td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{LH} )</td>
<td>Input Current of ( \bar{E}, V_E = 5V )</td>
<td>Full</td>
<td>-50</td>
<td>50</td>
<td>II</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{LL} )</td>
<td>Input Current of ( \bar{E}, V_E = 0 )</td>
<td>Full</td>
<td>-50</td>
<td>50</td>
<td>II</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{ODIS} )</td>
<td>( I_{OUT}, ) Disabled ( \bar{E} = 2.0V )</td>
<td>Full</td>
<td>±1</td>
<td></td>
<td>II</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>Full</td>
<td>13</td>
<td>16</td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

\( (R_L = 25\Omega, C_L = 4 \text{ pF}, C_{IH} = 2 \text{ pF}, T_A = 25^\circ C, V_G = 1V, V_S = \pm 15V) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( BW_1 )</td>
<td>Current Mode Bandwidth (-3 \text{ dB})</td>
<td>150</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>( BW_2 )</td>
<td>Current Mode Bandwidth (\pm 0.1 \text{ dB})</td>
<td>30</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>( BW_p )</td>
<td>Power, ( I_{IN} = 1 \text{ mA p-p})</td>
<td>150</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>( BW_g )</td>
<td>Gain Control Bandwidth</td>
<td>20</td>
<td>V</td>
<td></td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>( SRG )</td>
<td>Gain Control Slew Rate ( V_G ) from 0.2V to 2V</td>
<td>12</td>
<td>V</td>
<td></td>
<td>(mA/mA)/( \mu )s</td>
<td></td>
</tr>
<tr>
<td>( T_{REC} )</td>
<td>Recovery Time from ( V_G &lt; 0 )</td>
<td>250</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( T_{EN} )</td>
<td>Enable Time from ( \bar{E} ) Pin</td>
<td>200</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( T_{DIS} )</td>
<td>Disable Time from ( \bar{E} ) Pin</td>
<td>30</td>
<td>V</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( D_G )</td>
<td>Differential Gain, NTSC with ( I_{IN} = -0.35 \text{ mA to } +0.35 \text{ mA} )</td>
<td>0.25</td>
<td>V</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( D_p )</td>
<td>Differential Phase, NTSC with ( I_{IN} = -0.35 \text{ mA to } +0.35 \text{ mA} )</td>
<td>0.05</td>
<td>V</td>
<td></td>
<td>Degree</td>
<td></td>
</tr>
</tbody>
</table>
Typical Performance Curves

**Current Gain vs Frequency for Different Gains**

- $A_g = -12\, \text{dB}$, $A_g = -6\, \text{dB}$
- $A_g = -24\, \text{dB}$, $A_g = -18\, \text{dB}$
- $A_g = -12\, \text{dB}$, $A_g = 0\, \text{dB}$

**Current Gain Flatness**

- $V_s = \pm 15\, \text{V}$
- $R_s = 25\, \Omega$

**Harmonic Distortion vs Input Amplitude**

- 2nd Harmonic $f_0 = 40\, \text{MHz}$
- 3rd Harmonic $f_0 = 40\, \text{MHz}$
- 3rd Harmonic $f_0 = 1\, \text{MHz}$
- 2nd Harmonic $f_0 = 1\, \text{MHz}$

**Output Current Noise vs Frequency**

- $V_s = \pm 15\, \text{V}$
- $V_s = 2\, \text{V}$
- $V_s = 1\, \text{V}$
- $V_s = 0.5\, \text{V}$
- $V_s = 0.25\, \text{V}$
Typical Performance Curves — Contd.

Differential Gain Error vs DC Offset Current

Differential Phase Error vs DC Offset Current

Gain Pin Transient Response

Gain Control Recovery From $V_g = -0.1V$

Gain Control Pin Frequency Response

$\text{I}_\text{OUT} \text{ vs } \text{I}_\text{IN}$

Normalized Gain Error vs $V_{\text{GAIN}}$ Voltage
Typical Performance Curves — Contd.

- **Current Gain vs Supply Voltage**
  - $V_G = 1V$
  - $I_H = \pm 350 \mu A$

- **Current Gain vs Temperature**
  - $V_G = 2V$
  - $V_G = 1V$

- **Output Capacitance vs Output Voltage**
  - $V_S = \pm 5V$
  - $V_S = \pm 15V$

- **Enable Pin Response**

- **Supply Current vs Supply Voltage**
  - $V_G = 2V$
  - $V_G = 1V$

- **Supply Current vs Die Temperature**
  - $V_G = 2V$
  - $V_G = 1V$
Applications Information

The EL2082 is best thought of as a current-conveyor with variable current gain. A current input to the I\textsubscript{IN} pin will be replicated as a current driven out the I\textsubscript{OUT} pin, with a gain controlled by V\textsubscript{GAIN}. Thus, an input of 1 mA will produce an output current of 1 mA for V\textsubscript{GAIN} = 1V. An input of 1 mA will produce an output of 2 mA for V\textsubscript{GAIN} = 2V. The useable V\textsubscript{GAIN} range is zero to +2V. A negative level on V\textsubscript{GAIN}, even only −20 mV, will yield very high signal attenuation.

The EL2082 in Conjunction with Op-Amps

This resistor-load circuit shows a simple method of converting voltage signals to currents and vice versa:

\[
\text{Gain} = \frac{V\text{GAIN}}{1V} \left( \frac{R_L}{R_{IN} + 95\Omega} \right) \left( \frac{R_F + R_G}{R_G} \right)
\]

R\textsubscript{IN} would typically be 1 kΩ for video level inputs, or 10 kΩ for ±10V instrumentation signals. The higher the value of R\textsubscript{IN} (the lower the input current), the lower the distortion levels of the EL2082 will be. An approximate expression of the nonlinearity of the EL2082 is:

\[
\text{Nonlinearity} \% = 0.3 \times I_{IN} (\text{mA})^2
\]

Optimum input current level is a tradeoff between distortion and signal-to-noise-ratio. The distortion and input range do not change appreciably with V\textsubscript{GAIN} levels; distortion is set by input currents alone.
Applications Information — Contd.

The output current could be terminated with a 1 kΩ load resistor to achieve a nominal voltage gain of 1 at the EL2082, but the $I_{OUT}$, load, and stray capacitances would limit bandwidth greatly. The lowest practical total capacitance at $I_{OUT}$ is about 12 pF, and this gives a 13 MHz bandwidth with a 1 kΩ load. In the above example a 100Ω load is used for an upper limit of 130 MHz. The operational amplifier gives a gain of +10 to bring the overall gain to unity. Wider bandwidth yet can be had by installing $C_{IN}$. This is a very small capacitor, typically 1 pf–2 pF, and it bolsters the gain above 100 MHz. Here is a table of results for this circuit used with various amplifiers:

<table>
<thead>
<tr>
<th>Operational Amplifier</th>
<th>Power Supplies</th>
<th>$R_f$</th>
<th>$R_g$</th>
<th>$C_{IN}$</th>
<th>$-3\ dB$ Bandwidth</th>
<th>$0.1\ dB$ Bandwidth</th>
<th>Peaking</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2020</td>
<td>± 5V</td>
<td>620</td>
<td>68</td>
<td>—</td>
<td>34 MHz</td>
<td>5.6 MHz</td>
<td>0</td>
</tr>
<tr>
<td>EL2020</td>
<td>± 15V</td>
<td>620</td>
<td>68</td>
<td>—</td>
<td>40 MHz</td>
<td>7.4 MHz</td>
<td>0</td>
</tr>
<tr>
<td>EL2130</td>
<td>± 5V</td>
<td>620</td>
<td>68</td>
<td>—</td>
<td>73 MHz</td>
<td>11 MHz</td>
<td>1.0 dB</td>
</tr>
<tr>
<td>EL2030</td>
<td>± 15V</td>
<td>620</td>
<td>68</td>
<td>—</td>
<td>93 MHz</td>
<td>12 MHz</td>
<td>1.3 dB</td>
</tr>
<tr>
<td>EL2090</td>
<td>± 15V</td>
<td>240</td>
<td>27</td>
<td>—</td>
<td>60 MHz</td>
<td>10 MHz</td>
<td>0.5 dB</td>
</tr>
<tr>
<td>EL2120</td>
<td>± 5V</td>
<td>220</td>
<td>24</td>
<td>—</td>
<td>57 MHz</td>
<td>10 MHz</td>
<td>0.4 dB</td>
</tr>
<tr>
<td>EL2120</td>
<td>± 15V</td>
<td>220</td>
<td>24</td>
<td>—</td>
<td>65 MHz</td>
<td>11 MHz</td>
<td>0.3 dB</td>
</tr>
<tr>
<td>EL2070</td>
<td>± 5V</td>
<td>200</td>
<td>22</td>
<td>2 pF</td>
<td>150 MHz</td>
<td>30 MHz</td>
<td>0.4 dB</td>
</tr>
<tr>
<td>EL2071</td>
<td>± 5V</td>
<td>1.5K</td>
<td>240</td>
<td>2 pF</td>
<td>200 MHz</td>
<td>30 MHz</td>
<td>0</td>
</tr>
<tr>
<td>EL2075</td>
<td>± 5V</td>
<td>620</td>
<td>68</td>
<td>2 pF</td>
<td>270 MHz</td>
<td>30 MHz</td>
<td>1.5 dB</td>
</tr>
</tbody>
</table>

Maximum bandwidth is maintained over a gain range of +6 to −16 dB; bandwidth drops at lower gains. If wider gain range with full bandwidth is required, two or more EL2082's can be cascaded with the $I_{OUT}$ of one directly driving the $I_{IN}$ of the next.

The EL2082 can also be used with an I → V operational circuit:

![Inverting EL2082 Op-Amp](image)

The circuit above gives a negative gain. The main concern of this connection involves the total $I_{OUT}$ and stray capacitances at the amplifier's input. When using traditional op-amps, the pole caused by these capacitances can make the amplifier less stable and even cause oscillations in amplifiers whose gain-bandwidth is greater than 5 MHz. A typical cure is to add a capacitor $C_f$ in the 2 pF–10 pF range. This will reduce overall bandwidth, so a capacitor $C_{IN}$ can be added to regain frequency response. The ratio $C_f/C_{IN}$ is made equal to $R_{IN}/R_f$. 

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Applications Information — Contd.

Current-feedback amplifiers eliminate this difficulty. Because their input is a very low impedance, capacitance at the summing point of an inverting operational circuit is far less troublesome. Here is a table of results of various current-feedback circuits used in the inverting circuit:

<table>
<thead>
<tr>
<th>Operational Amplifier</th>
<th>Power Supplies</th>
<th>Rf</th>
<th>RIN</th>
<th>Rg</th>
<th>Bandwidth</th>
<th>Bandwidth</th>
<th>Peaking</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2020</td>
<td>±5V</td>
<td>1k</td>
<td>910</td>
<td>—</td>
<td>29 MHz</td>
<td>4.3 MHz</td>
<td>0</td>
</tr>
<tr>
<td>EL2020</td>
<td>±15V</td>
<td>1k</td>
<td>910</td>
<td>—</td>
<td>34 MHz</td>
<td>5.3 MHz</td>
<td>0</td>
</tr>
<tr>
<td>EL2130</td>
<td>±5V</td>
<td>1k</td>
<td>910</td>
<td>—</td>
<td>61 MHz</td>
<td>9.7 MHz</td>
<td>0</td>
</tr>
<tr>
<td>EL2030</td>
<td>±15V</td>
<td>1k</td>
<td>910</td>
<td>—</td>
<td>82 MHz</td>
<td>12.3 MHz</td>
<td>0</td>
</tr>
<tr>
<td>EL2171</td>
<td>±5V</td>
<td>2k</td>
<td>1.8k</td>
<td>1k</td>
<td>114 MHz</td>
<td>11 MHz</td>
<td>1.2 dB</td>
</tr>
</tbody>
</table>

with the EL2171 the EL2082 had ±15V supplies and the EL2171 required a 150Ω output load.

The EL2120 and EL2090 are suitable in this circuit but they are compensated for 300Ω feedback resistors. RIN would have to be reduced greatly to obtain unity gain and the increased signal currents would cause the EL2082 to display much increased distortion. They could be used if the input resistor were maintained at 910Ω and Rf reduced for a −1/3 gain, or if Rf = 1k and an overall bandwidth of 25 MHz were acceptable.

The EL2082 can also be used within an op-amp’s feedback loop:

![Diagram of EL2082 in feedback inverting gain](image)

Gain = \( \frac{1V}{V_{\text{GAIN}}} \left( \frac{R_f + 95\Omega}{R_{\text{IN}}} \right) \)

With voltage-mode op-amps, the same concern about capacitance at the summing node exists, so Cf and CIN should be used. As before, current-feedback amplifiers tend to solve the problem. However, in this circuit the inherent phase lag of the EL2082 detracts from the phase margin of the op-amp, and some overall bandwidth reduction may result. The EL2082 appears as a 3.0 ns delay, well past 100 MHz. Thus, for a 20 MHz loop bandwidth, the EL2082 will subtract 20 MHz × 3.0 ns × 360 degrees = 21.6 degrees. The loop path should have at least 55 degrees of phase margin for low ringing in this connection. Loop bandwidth is always reduced by the ratio RIN/(RIN + Rf) with voltage mode op-amps.
Applications Information — Contd.

Current-feedback op-amps again solve the summing-junction capacitance problem in this connection. The loop bandwidth here becomes a matter of transimpedance over frequency and its phase characteristics. Unfortunately, this is generally poorly documented in amplifier data sheets. A rule of thumb is that the transimpedance falls to the value of the recommended feedback resistor at a frequency of $F - 3 \, \text{dB}/4$ to $F - 3 \, \text{dB}/2$, where $F - 3 \, \text{dB}$ is the unity-gain closed-loop bandwidth of the amplifier. The phase margin of the op-amp is usually close to 90 degrees at this frequency.

In general, $R_f$ is initially the recommended value for the particular amplifier and is then empirically adjusted for amplifier stability at maximum $V_{\text{GAIN}}$, then $R_{\text{IN}}$ is set for the overall circuit gain required. Sometimes a very small $C_f$ can be used to improve loop stability, but it often must be in series with another resistor of value around $R_f/2$.

A virtue of placing the EL2082 in feedback is that the input-referred noise will drop as gain increases. This is ideal for level controls that are used to set the output to a constant level for a variety of inputs as well as AGC loops. Furthermore, the EL2082 has a relatively constant input signal amplitude for a variety of input levels, and its distortion will be relatively constant and controllable by setting $R_f$. Note that placing the EL2082 in the feedback path causes the circuit bandwidth to vary inversely with gain.

The next circuit shows use of the EL2082 in the feedback path of a non-inverting op-amp:

![Circuit Diagram](https://example.com/circuit.png)

This example has the same virtues with regards to noise and distortion as the preceding circuit; and its bandwidth shrinks with increasing gain as well. The typical 12 pF sum of EL2082 output capacitance in parallel with stray capacitance necessitates the inclusion of $C_f$ to prevent a feedback pole. Because of this 12 pF capacitance at the op-amp -input, current-feedback op-amps will generally not be usable. As before, the loop bandwidth and phase margin must accommodate the extra phase lag of the EL2082.
Applications Information — Contd.

Using the $V_{IN}$ Pin
The $V_{IN}$ pin can be used instead of the $I_{IN}$ pin so:

\[
G_m = \frac{I_{OUT}}{V_{IN}} = -\frac{V_g}{1v} \left( \frac{1}{R_g + 95\Omega} \right)
\]

This connection is useful when a high input impedance is required. There are a few caveats when using the $V_{IN}$ pin. The first is that $V_{IN}$ has a 250 V/µs slew rate limitation. The second is that the inevitable $C_{STRAY}$ across $R_g$ causes a gain zero and gain INCREASES above the $1/(2\pi C_{STRAY} R_g)$ frequency and can peak as much as 20 dB with large $C_{STRAY}$. A graph of gain vs. frequency for several $C_{STRAY}$s is included in the typical performance curves. In general, if wide bandwidth and frequency flatness is desired, the $I_{IN}$ pin should be used.

The $V_{IN}$ pin does make an excellent ground reference pin, for instance when low-frequency noise is to be rejected. The next schematic shows the EL2082 $V_{IN}$ pin rejecting possible 60 Hz hum induced on an RF input cable:

This example shows $V_{IN}$ rejecting low-frequency field-induced noise but not adding peaking since the 0.01 µF bypass capacitor shunts high-frequency signals to local ground.

Reactive Couplings with the EL2082
The following sketch is an excerpt of a receiver IF amplifier showing methods of connecting the EL2082 to reactive networks:
Applications Information — Contd.
The $I_{IN}$ pin of the EL2082 looks like 95$\Omega$ well past 100 MHz, and the output looks like a simple current-source in parallel with about 5 pF. There is no particular problem with any resistance or reactance connected to $I_{IN}$ or $I_{OUT}$. The mixer output is generally sent to a crystal filter, which required a few hundred ohm terminating impedance. The impedance of the $I_{IN}$ pin of the first EL2082 is transformed to about 400$\Omega$ by the 2:1 transformer $T1$. The two EL2082's are used as variable-gain IF amplifiers, with small gains offered by each. The output of the first EL2082 is coupled to the second by the resonant matching network $L1-C1$. For a $Q$ of 5, $Xc1 = x11 = 5 \times 95\Omega$, approximately. The impedance seen at the first EL2082's $I_{OUT}$ will be about $Q^2 \times 95\Omega$, or 2.5k, and by impedance transformation alone the first gain cell delivers 28 dB of gain at $V_g = 1$V. More gain cells can be used for a wider range of (calibrated) AGC compliance.

The $E$ input can be used as a high-speed noise blanker gate.

Linearized Fader/Gain Control
The following circuit is an example of placing two EL2082's in the feedback network of an op-amp to significantly reduce their distortions:

\[
V_{OUT} = K \cdot V_A + (1-K) \cdot V_B
\]

where $0 \leq K \leq 1$

![Linearized Gain Control/Fader](image)
Applications Information — Contd.

The circuit sums two inputs A and B, such that the sum of their respective path gains is unity, as controlled by the potentiometer. When the potentiometer's wiper is fully down, the slightly negative voltage at the Vg of the B-side EL2082 cuts off the B signal to better than 70 dB attenuation at 3.58 MHz. The A-side EL2082 is at unity gain, so the only (error) signal presented to the op-amp's input is the same (error) signal at the IIN of the A-side EL2082. The circuit thus outputs -AIN. Since the error signal required by the op-amp is very small, even at video frequencies, the current through the A-side EL2082 is small and distortion is minimized.

At 50% potentiometer setting, equal error output signals flow from the EL2082's, since the op-amp still requires little net -input current. The EL2082's essentially buck each other to establish an output, and 50% gain occurs for both the A and B inputs. The EL2082's now contribute distortion, but less than in previous connections. The op-amp sees a constant 1k feedback resistor regardless of potentiometer setting, so frequency response is stable for all gain settings.

A single-input gain control is implemented by simply grounding B_IN.

Distortion can be improved by increasing the input resistors to lower signal currents. This will lower the overall gain accordingly, but will not affect bandwidth, which is dependent upon the feedback resistors. Reducing the signal input amplitude is an analogous tactic, but the noise floor will effectively rise.

Another strategy to reduce distortion in video systems is to use DC restoration circuitry, such as the EL2090 ahead of the fader inputs to reduce the range of signals to be dealt with; the -0.7V to +0.7V possible range of inputs (due to capacitor coupling) would be changed to a stabilized -0.35V to +0.35V span.

The EL2020, EL2030, and EL2120 (at reduced bandwidth since it is compensated for 300Ω feedback resistors) all give the same video performance at NTSC operation.

Variable Filters

This circuit is the familiar state-variable configuration, similar to the bi-quad:

Voltage Tuneable Bi-Quad Filter

\[ F_0 = \frac{V_g}{1V} \left( \frac{1}{2\pi (R + 95\Omega)C} \right) \]
**Applications Information — Contd.**

Frequency-setting resistors R are each effectively adjusted in value by an EL2082 to effect voltage-variable tuning. Two gain controls yield a linear frequency adjustment; using one gives a square-root-of-control voltage tuning. The EL2082's could be placed in series with the integrator capacitors instead to yield a tuning proportional to $1/V_g$.

The next circuit is one of a new class of "CCII" filters that use the current-conveyor element. Basic information is available in the April 1991, volume 38, number 4 edition of the IEEE Transactions on Circuits and Systems journal, pages 456 through 461 of the article "The Single CCII Biquads with High-Input Impedance", by Shen-Iuan Liu and Hen-Wai Tsao.

![Image](image.png)

This interesting filter uses the current output of the EL2082 to generate a bandpass voltage output and the intermediate node provides a second-order low-pass filter output. Both outputs should be buffered so as not to warp characteristics, although the $V_{IN}$ of the next EL2082 can be driven directly in the case of cascaded filters. The $V_{GAIN}$ input acts as a $Q$ and peaking adjust point around the nominal 1V value. The resistor at $I_{OUT}$ could serve as the frequency trim, and $Q$ trimmed subsequently with $V_{GAIN}$.

**Negative Components**

The following circuit converts a component or two-terminal network to a variable and even negative replica of that impedance:

![Image](image.png)

$$Z_{IN} = \frac{(Z + 95\Omega)}{(1 - Vg/1V)}$$
Applications Information — Contd.

A negative impedance is simply an impedance whose current flows reverse to the normal sense. In the above circuit, the current through Z is replicated by the EL2082 and inverted (\(I_{\text{OUT}}\) flows inverted to the sense of \(I_{\text{IN}}\) in the EL2082) and summed back to the input. When \(V_g = 0\) or \(V_g < 0\), the input impedance is simply \(Z + 95\Omega\). When \(V_g = 1\)V, the negative of the current through Z is summed with the input and the input impedance is "infinite". When \(V_g = 2\)V, twice the negative of the current through Z is summed with the input resulting in an input impedance of \(-Z - 95\Omega\).

Thus variable capacitors can be simulated by substituting the capacitor as Z. "Negative" capacitors result for \(V_g > 1\)V, and capacitance needs to be present in parallel with the input to prevent oscillations. Inductors or complicated networks also work for Z, but a net negative impedance will result in oscillations.

**EL2082 Macromodel**

This macromodel has been designed to work with PSPICE (copyrighted by the Microsim Corporation). E500 buffers in the \(V_{\text{IN}}\) voltage and presents it to the \(R_{\text{IN}}\) resistor to emulate the \(I_{\text{IN}}\) pin. E501 supplies the non-linearity of the current channel and replicates the \(I_{\text{IN}}\) current to a ground referenced voltage. R500 and C500 provide the bandwidth limitation on the current signal. E502 supplies the \(V_{\text{GAIN}}\) non-linearity and drives the L501/R501/C501 to shape the gain control frequency response. E503 does the actual gain-control multiplication, and drives delay line T500 to better simulate the actual phase characteristics of the part. G500 creates the current output, and \(R_{\text{OUT}}\) with \(C_{\text{OUT}}\) provide proper output parasitics.

The model is good at frequency and linearity estimates around \(V_g = 1\)V and nominal temperatures, but has several limitations:

- The \(V_g\) channel does not give zero gain for \(V_g < 0\); the output gain reverses—don’t use \(V_g < 0\).
- The \(V_g\) channel is not slew limited.
- Frequency response does not vary with supply voltage.
- The \(V_{\text{IN}}\) channel is not slew limited.

Unfortunately, the polynomial expressions and two-input multiplication may not be available on every simulator. Results have been confirmed by laboratory results in many situations with this macromodel, within its capabilities.
EL2082 Macromodel

*: Vgain
*: In
*: Vin
*: Iout

.SUBCKT EL2082macro (1 2 3 4 5 6 7 8)

*** I-to-I gain cell macromodel ***

******
Cini 2 0 2P
C500 502 0.9845P
C501 505 0 1000P
Cout 6 0 5P
L501 503 504 0.1U
Rsilly1 1 0 1E9
Rsilly2 505 0 1E9
Rini 2 500 95
Rinv 3 0 2Meg
Rout 6 0 1Meg
R500 501 502 1000
R501 504 505 5
R502 506 507 50
R503 508 0 50
E500 500 3 0 1
E501 501 0 POLY(1) (2,500) 0 2 0 -.8
E502 503 0 POLY(1) (1,0) 0 1.05 -.05
E503 506 0 POLY(2) (505,0) (502,0) 0 0 0 0 1
G500 6 0 508 0 -0.0105
T500 508 0 507 0 Z0=50 TD=1.95N

.ENDS
### Features
- Complete video level restoration system
- 0.01% differential gain and 0.02° differential phase accuracy at NTSC
- 100 MHz bandwidth
- 0.1 dB flatness to 20 MHz
- Sample-and-hold has 15 nA typical leakage and 1.5 pC charge injection
- System can acquire DC correction level in 10 μs, or 5 scan lines of 2 μs each, to $\frac{1}{2}$ IRE
- $V_S = \pm 5V$ to $\pm 15V$
- TTL/CMOS hold signal

### Applications
- Input amplifier in video equipment
- Restoration amplifier in video mixers

### Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2090CN</td>
<td>0°C to + 75°C</td>
<td>14-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2090CM</td>
<td>0°C to + 75°C</td>
<td>16-Lead SOL</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

### General Description

The EL2090C is the first complete DC-restored monolithic video amplifier sub-system. It contains a very high-quality video amplifier and a nulling sample-and-hold amplifier specifically designed to stabilize video performance. When the HOLD logic input is set to a logic 0 during a horizontal sync, the sample-and-hold amplifier may be used as a general-purpose op-amp to null the DC offset of the video amplifier. When the HOLD input goes to a logic 1 the sample-and-hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent scan line.

The video amplifier is optimized for video characteristics, and performance at NTSC is nearly perfect. It is a current-feedback amplifier, so that $-3$ dB bandwidth changes little at various closed-loop gains. The amplifier easily drives video signal levels into 75Ω loads. With 100 MHz bandwidth, the EL2090 is also useful in HDTV applications.

The sample-and-hold is optimized for fast sync pulse response. The application circuit shown will restore the video DC level in five scan lines, even if the HOLD pulse is only 2 μs long. The output impedance of the sample-and-hold is low and constant over frequency and load current so that the performance of the video amplifier is not compromised by connections to the DC restore circuitry.

The EL2090C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL2090C is specified for operation over the 0°C to 75°C temperature range.

### Connection Diagrams

- **14-Pin DIP Package**
  - Video In: 1, N.C.: 2, Video Out: 3, 5
  - Gnd: 4
  - S/H In: 5, S/H Out: 6
  - Hold Control: 8, N.C.: 9, Child: 10
  - 2090-1

- **16-Pin SOL Package**
  - Video In: 1, N.C.: 2, Video Out: 3, 5
  - Gnd: 4
  - S/H In: 5, S/H Out: 6
  - Hold Control: 8, N.C.: 9, Child: 10
  - 2090-2
**Absolute Maximum Ratings (TA = 25°C)**

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage between V+ and V-</td>
<td>36V</td>
</tr>
<tr>
<td>Voltage between VIN+, S/HIN+, S/HIN-, C_HOLD, and GND pins</td>
<td>(V+) + 0.5V to (V-) - 0.5V</td>
</tr>
<tr>
<td>VOOUT Current</td>
<td>60 mA</td>
</tr>
<tr>
<td>Current into VIN- and HOLD Pins</td>
<td>5 mA</td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elanec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TA=Tj=Tc=TA.

**Open Loop DC Electrical Characteristics**

VS = ±15V; RL = 150Ω, TA = 25°C unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I TOTAL</td>
<td>Total Supply Current</td>
<td>Full</td>
<td>14</td>
<td>17</td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Video Amplifier Section (Not Restored)**

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOOS</td>
<td>Input Offset Voltage</td>
<td>Full</td>
<td>8</td>
<td>70</td>
<td>II</td>
<td>mV</td>
</tr>
<tr>
<td>IIB+</td>
<td>+VIN Input Bias Current</td>
<td>Full</td>
<td>2</td>
<td>15</td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>IIB-</td>
<td>-VIN Input Bias Current</td>
<td>Full</td>
<td>30</td>
<td>150</td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>ROL</td>
<td>Transimpedance</td>
<td>25°C</td>
<td>300</td>
<td>V</td>
<td>V/mA</td>
<td></td>
</tr>
<tr>
<td>AVOL</td>
<td>Open-Loop Voltage Gain; VOOUT = ±2V</td>
<td>Full</td>
<td>56</td>
<td>65</td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VS = ±15V; RL = 2 kΩ</td>
<td>Full</td>
<td>±12</td>
<td>±13</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VS = ±5V; RL = 150Ω</td>
<td>Full</td>
<td>±3.0</td>
<td>±3.5</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>ISC</td>
<td>Short-Circuit Current; +VIN Set to ±2V; -VIN to Ground through 1 kΩ</td>
<td>25°C</td>
<td>±50</td>
<td>±90</td>
<td>±160</td>
<td>II</td>
</tr>
</tbody>
</table>

**Sample-And-Hold Section**

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>Full</td>
<td>2</td>
<td>10</td>
<td>II</td>
<td>mV</td>
</tr>
<tr>
<td>IB</td>
<td>Input Bias Current</td>
<td>Full</td>
<td>0.5</td>
<td>2.5</td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>IOS</td>
<td>Input Offset Current</td>
<td>Full</td>
<td>0.05</td>
<td>0.5</td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>RN, DIFF</td>
<td>Input Differential Resistance</td>
<td>25°C</td>
<td>200</td>
<td>V</td>
<td>kΩ</td>
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<tr>
<td>RN, COMM</td>
<td>Input Common-Mode Resistance</td>
<td>25°C</td>
<td>100</td>
<td>V</td>
<td>MΩ</td>
<td></td>
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<tr>
<td>VCM</td>
<td>Common-Mode Input Range</td>
<td>Full</td>
<td>±11</td>
<td>±12.5</td>
<td>II</td>
<td>V</td>
</tr>
</tbody>
</table>
**Open Loop DC Electrical Characteristics**

\( V_S = \pm 15V; R_L = 1500; T_A = 25°C \) unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp.</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>Sample-And-Hold Section</td>
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<td></td>
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<tr>
<td>( AVOL )</td>
<td>Large Signal Voltage Gain</td>
<td>Full</td>
<td>15k</td>
<td>50k</td>
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<td>II</td>
<td>V/V</td>
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<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>Full</td>
<td>75</td>
<td>95</td>
<td></td>
<td>II</td>
<td>dB</td>
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<td>PSRR</td>
<td>Power-Supply Rejection Ratio</td>
<td>Full</td>
<td>75</td>
<td>95</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>( V_{\text{thresh}} )</td>
<td>HOLD Pin Logic Threshold</td>
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<td>1.4</td>
<td>2.0</td>
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<td>V</td>
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<tr>
<td>( I_{\text{droop}} )</td>
<td>Hold Mode Droop Current</td>
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<td>10</td>
<td>50</td>
<td></td>
<td>II</td>
<td>nA</td>
</tr>
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<td>( I_{\text{charge}} )</td>
<td>Charge Current Available to</td>
<td>Full</td>
<td>±90</td>
<td>±135</td>
<td></td>
<td>II</td>
<td>( \mu )A</td>
</tr>
<tr>
<td></td>
<td>Chold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>( V_O )</td>
<td>Output Swing; ( R_L = 2k )</td>
<td>Full</td>
<td>±10</td>
<td>±13</td>
<td>±40</td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( I_{SC} )</td>
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<td>25°C</td>
<td>±10</td>
<td>±17</td>
<td>±40</td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Closed Loop AC Electrical Characteristics**

\( V_S = \pm 15V; C_L = 15 \text{ pF}; C_{\text{stray}} (\sim - V_{\text{IN}}) = 2.5 \text{ pF}; R_F = R_G = 3000; R_L = 1500; C_{\text{hold}} = 100 \text{ pF}; T_A = 25°C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Video Amplifier Section</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>SlewRate; ( V_{\text{OUT}} ) from (-2 ) to (+2)V</td>
<td>600</td>
<td></td>
<td></td>
<td>III</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth; (-3 ) dB</td>
<td>75</td>
<td>100</td>
<td></td>
<td>III</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>( \pm 1 ) dB</td>
<td>35</td>
<td>60</td>
<td></td>
<td>III</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>( \pm 0.1 ) dB</td>
<td>10</td>
<td>20</td>
<td></td>
<td>III</td>
<td>MHz</td>
</tr>
<tr>
<td>Peaking</td>
<td>Differential Gain; ( V_{\text{IN}} ) from (-0.7 ) to (+0.7)V; ( F = 3.58 ) MHz</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
<td>V/%</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Phase; ( V_{\text{IN}} ) from (-0.7 ) to (+0.7)V; ( F = 3.58 ) MHz</td>
<td>0.02</td>
<td></td>
<td></td>
<td></td>
<td>V/°</td>
</tr>
<tr>
<td>Sample-And-Hold Section</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>BW</td>
<td>Gain-Bandwidth Product</td>
<td>1.3</td>
<td></td>
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<td>V/MHz</td>
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<tr>
<td>( \Delta Q )</td>
<td>Sample to Hold Charge</td>
<td>1.5</td>
<td>5</td>
<td></td>
<td>III</td>
<td>pC</td>
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<tr>
<td></td>
<td>Injection (Note 1)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta T )</td>
<td>Sample to Hold or Hold to</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td></td>
<td>Sample Delay Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_s )</td>
<td>Sample to Hold Settling</td>
<td>200</td>
<td></td>
<td></td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td></td>
<td>Time to 2 \text{ mV}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: The logic input is between 0V and 5V, with a 220\Omega resistor in series with the HOLD pin and 39 pF capacitor from HOLD pin to ground.
Figure 1. Typical Application (AV = +2)

Typical Performance Curves

Relative Frequency Response for Various Gains

Frequency Response with Different Loads (AV = +2)

Frequency Response Flatness for Various Load and Supply Conditions

Frequency Response Flatness vs CIN, AV = +2
Typical Performance Curves — Contd.

Differential Gain and Phase vs Supply Voltage; $A_V = +2$, $R_L = 150\Omega$, $V_{IN}$ from 0 to $+0.7\ V_{DC}$

Deviation from Linear Phase vs Frequency

Differential Gain vs DC Input Offset; $A_V = +2$, $F_O = 3.58\ MHz$, $R_L = 150\Omega$

Differential Phase vs DC Input Offset; $A_V = +2$, $F_O = 3.58\ MHz$, $R_L = 150\Omega$
Typical Performance Curves — Contd.

- **S/H Available Charge Current vs Temperature**
- **Sample-to-Hold Change Injection vs Temperature**
- **Typical Droop Current vs Temperature, $V_S = \pm 15V$**
- **Supply Current vs Supply Voltage**
- **Supply Current vs Temperature; $V_S = \pm 15V$**
Applications Information

The EL2090C is a general purpose component and thus the video amplifier and sample-and-hold pins are uncommitted. Therefore much of the ultimate performance as a DC-restored video amplifier will be set by external component values and parasitics. Some application considerations will be offered here.

The DC feedback from the sample-and-hold can be applied to either positive or negative inputs of the video amplifier (with appropriate phasing of the sample-and-hold amplifier inputs). We will consider feedback to the inverting video input. During a sample mode (the HOLD input at a logic low), the sample-and-hold acts as a simple nulling op-amp.

Ideally, the DC feedback resistor Raz is a high value so as not to couple a large amount of the AC signal on the video input back to the sample-and-hold amplifier output. The sample-and-hold output is a low impedance at high frequencies, but variations of the DC operating point will change the output impedance somewhat. No more than a few ohms output impedance change will occur, but this can cause gain variations in the 0.01% realm. This DC-dependent gain change is in fact a differential gain effect. Some small differential phase error will also be added.

The best approach is to maximize the DC feedback resistor value so as to isolate the sample-and-hold from the video path as much as possible. Values of 1 kΩ or above for Raz will cause little to no video degradation.

This suggests that the largest applicable power supply voltages be used so that the output swing of the sample-and-hold can still correct for the variations of DC offset in the video input with large values of Raz. The typical application circuit shown will allow correction of ±1V inputs with good isolation of the sample-and-hold output. Good isolation is defined as no video degradation due to the insertion of the sample-and-hold loop. Lower supply voltages will require a smaller value of DC feedback resistor to retain correction of the full input DC variation. The EL2090 differential phase performance is optimum at ±9V supplies, and differential gain only marginally improves above this voltage. Since all video characteristics mildly degrade with increasing die temperature, the ±9V levels are somewhat better than ±15V supplies. However, ±15V supplies are quite usable.

Ultimate video performance, especially in HDTV applications, can also be optimized by setting the black-level reference such that the signal span at the video amplifier's output is set to its optimum range. For instance, setting the span to ±1V of output is preferable to a span of 0V to +2V. The curves of differential gain and phase versus input DC offset will serve as guides.

The DC feedback resistor may be split so that a bypass capacitor is added to reduce the initially small sample-and-hold transients to even smaller levels. The corruption can be reduced to as low as 1 mV peak seen at the video amplifier output. The size of the capacitor should not be so large as to de-stabilize the sample-and-hold feedback loop, nor so small as to reduce the video amplifier's gain flatness. A resistor or some other video isolation network should be inserted between the video amplifier output and the sample-and-hold input to prevent excessive video from bleeding through the autozero section, as well as preventing spurious DC correction due to video signals confusing the sample-and-hold during autozero events. Figure 1 shows convenient component values. A full 3.58 MHz trap is not necessary for suppressing NTSC chroma burst interaction with the sample-and-hold input; the simple R-C network suggested in Figure 1 suffices.
Applications Information — Contd.

The HOLD input to the sample-and-hold has a 1.4V threshold and is clamped to a diode below ground and 6V above ground. The hold step characteristics are not sensitive to logic high nor low levels (within TTL or CMOS swings), but logic slewrates greater than 1000V/μs can couple noise and hold step into the sample-to-hold output waveforms. The logic slewrates should be greater than 50V/μs to avoid hold jitter. To avoid artificially high droop in hold mode, the Chold pin and Chold itself should be guarded with circuit board traces connected to the output of the sample-and-hold. Low-leakage hold capacitors should be used, such as mica or mylar, but not ceramic. The excellent properties of more expensive polystyrene, polypropylene, or teflon capacitors are not needed.

The user should be aware of a combination of conditions that may make the EL2090 operate incorrectly upon power-up. The fault condition can be described by noticing that the sample-and-hold output (pin 11) appears locked at a voltage close to VCC. This voltage is maintained regardless of changes at the inputs to the sample-and-hold (pins 5 and 6) or to the HOLD control input (pin 7). Two conditions must occur to bring this about:

1. A large value of Chold—usually values of 1000 pF or more. This is not an unusual situation. Many users want to reduce the size of the hold step and increasing Chold is the most direct way to do this. Increasing Chold also reduces the slew rate of the sample and hold section but because of the limited size of the video signal, this is usually not a limitation.

2. A sampling interval (dictated by the HOLD pin) that is too small. By small, we mean less than 2 μs.

For a sampling interval that is wide enough, there is enough time for the loop to close and for the amplifier to discharge whatever charge was dumped onto Chold it during the initial power spike and to then ramp up (or down) to the voltage that is proper for a balanced loop. When the sampling interval is too small, there is insufficient time for internal devices to recover from their initial saturated state from power-up because the feedback is not closed long enough. Therefore, typical recovery times for the loop are 2 μs or greater. Summarizing, the two things that could prevent proper saturation recovery are (as mentioned above) too large a capacitor which slows the charge and discharge rate of the stored voltage at Chold and too small a sampling interval in which the entire feedback loop is closed.

The circuit shown below prevents the fault condition from occurring by preventing the node from ever saturating. By clamping the value of Chold to some value lower than the supply voltage less
Applications Information — Contd.

A saturation voltage, we prevent this node from approaching the positive rail. The maximum voltage is set by the resistive voltage divider (between V+ and GND) R1 and R2 plus a diode. This value can be adjusted if the maximum size of the input signal is known. The diode used is an off-the-shelf 1N914 or 1N916.

As is true of all 100 MHz amplifiers, good bypassing of the supplies to ground is mandatory. 1 μF tantalums are sufficient, and 0.01 μF leaded chip capacitors in parallel with medium value electrolytics are also good. Leads longer than 1/2 can induce a characteristic 150 MHz resonance and ringing.

The VIN- of the video amplifier should have the absolute minimum of parasitic capacitance. Stray capacitance of more than 3 pF will cause peaking and compromise the gain flatness. The bandwidth of the amplifier is fundamentally set by the value of Rf. As demonstrated by the frequency response versus gain graph, the peaking and bandwidth is a weak function of gain. The EL2090 was designed for Rf = 300Ω giving optimum gain flatness at Av = +2. Unity-gain response is flattest for Rf = 360Ω; gains of +5 can use Rf = 270Ω. In situations where the peaking is accentuated by load capacitance or input capacitance the value of Rf will have to be increased, and some bandwidth will be sacrificed.

The VIN+ of the video amplifier should not look into an inductive source impedance. If the source is physically remote and a terminated input line is not provided, it may be necessary to connect an input "snubber" to ground. A snubber is a resistor in series with a capacitor which de-Q's the input resonance. Typical values are 100Ω and 30 pF.

The output of the video amplifier is sensitive to capacitive loads greater than 25 pF, and a snubber to ground or a resistor in series with the output is useful to isolate reactive loads.
EL2090 Macromodel

* Revision A, October 1992

.param vclamp = \{-0.002 \cdot (\text{TEMP} - 25)\}

* Connections:

<table>
<thead>
<tr>
<th>Vidin+</th>
<th>Vidin-</th>
<th>+ Vsupply</th>
<th>- Vsupply</th>
<th>Vid Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/H In+</td>
<td>S/H In-</td>
<td>Hold Control</td>
<td>Chold</td>
<td></td>
</tr>
</tbody>
</table>

.subckt EL2090/EL 3 1 14 12

********** Video Amplifier ***************

e1 20 0 3 0 1.0
via 20 34 0V
h2 34 38 vxx 1.0
r10 1 36 25
l1 36 38 20nH
iinp 3 0 10µA
iinn 1 0 5µA
h1 21 0 vis 600
r2 21 22 1K
d1 22 0 dclamp
d2 0 22 dclamp
e2 23 0 22 0.00166666666666666
l5 23 24 0.7µH
c5 24 0 0.5pF
r5 24 0 600
g1 0 25 24 0 1.0
rol 25 0 400K
cdp 25 0 7.7pF
q1 12 25 26 qp
c2 14 25 27 qn
c3 14 26 28 qn
c4 12 27 29 qp
r7 28 13 4
r8 29 13 4
ios1 14 26 2.5mA
ios2 27 12 2.5mA
ipe 14 12 7.2mA
ivos 0 33 5mA
vxx 33 0 0V
r11 33 0 1K

g4 0 49 0 5 6 1e-3
vcur 49 42 0v
r43 6 0 100Meg
r44 5 0 100Meg
r40 42 0 4K
d41 50 42 diode
d42 42 51 diode
v41 50 0 {vclamp}
v42 0 51 {vclamp}
g41 44 0 42 0 200e-6
r42 44 0 31Meg
d45 9 14 diode
d46 12 9 diode
s1 44 9 48 0 swa
e40 46 0 9 0.95
i40 0 9 10nA
r45 46 47 70
l40 47 11 70nH
c40 7 9 0.32pF
r47 7 48 10K
c41 48 0 3pF

* Models

* .model qn npn(is = 5e-15 bf = 500 tf = 0.1nS)
   .model qp pnp(is = 5e-15 bf = 500 tf = 0.1nS)
   .model dclamp d(is = 1e-30 ibv = 0.02 bv = 2.75 n = 4)
   .model diode d
   .model swa vs witch(von = 1.2v voff = 1.6v roff = 1e12 ron = 100)
   .ends
EL2090 Macromodel — Contd.

Sample and Hold Amplifier
EL2090C
100 MHz DC-Restored Video Amplifier

EL2090 Macromodel — Contd.

Video Amplifier
Features

- Novel current mode design
- Virtual ground current summing inputs
- Differential ground referenced current outputs
- High speed (both inputs)
  - 200 MHz bandwidth
  - 12 ns 1% settling time
- Low distortion
  - THD < 0.03% @ 1 MHz
  - THD < 0.1% @ 10 MHz
- Low noise (R_L = 50Ω)
  - 100 dB dynamic range
  - 10 Hz to 20 kHz
  - 73 dB dynamic range
  - 10 Hz to 10 MHz
- Wide supply conditions
  - ± 5 to ±15V operation
  - Programmable bias current
- 0.2 dB gain tolerance to 25 MHz

Applications

- Four quadrant multiplication
- Gain control
- Controlled signal summing and multiplexing
- HDTV video fading and switching
- Mixing/modulating/demodulating (phase detection)
- Frequency doubling
- Division
- Squaring
- Square rooting
- RMS and power measurement
- Vector addition-RMS summing
- CRT focus and geometry correction
- Polynomial function generation
- AGC circuits

General Description

The 4083C makes use of an Elantec fully complimentary oxide isolated bipolar process to produce a patent pending current in, current out four quadrant multiplier. Input and output signal summing and direct interface to other current mode devices can be accomplished by simple connection to reduce component count and preserve bandwidth. The selection of an appropriate series resistor value allows an input to accept a voltage signal of any size and optimize dynamic range. The differential outputs offer significant performance improvements which greatly extend the usable gain control range at high frequencies. The bias current is programmable to accommodate the voltage and power dissipation constraints of the package and available systems supplies.

The devices can implement all the classic four quadrant multiplier applications and are uniquely well suited to gain control and signal summing of broadband signals.

Connection Diagram

Manufactured under U.S. Patent No. 5,389,840
## Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Voltage between Vs+ and Vs-</th>
<th>Operating Junction Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vs</td>
<td>+33V</td>
<td>Tj EL4083 150°C</td>
</tr>
<tr>
<td>I(BIAS)</td>
<td>+2.4 mA</td>
<td>TST Storage Temperature -65°C to +150°C</td>
</tr>
<tr>
<td>IX</td>
<td>±2.4 mA</td>
<td></td>
</tr>
<tr>
<td>IY</td>
<td>±2.4 mA</td>
<td></td>
</tr>
<tr>
<td>Pd</td>
<td>Maximum Power Dissipation</td>
<td>See Curves</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
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<tr>
<td></td>
<td>EL4083 -40°C to +85°C</td>
<td></td>
</tr>
</tbody>
</table>

### Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_j = T_C = T_A \).

### Test Level

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
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<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QC00002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at ( T_A = 25°C ) and QA sample tested at ( T_A = 25°C ), ( T_{MAX} ) and ( T_{MIN} ) per QA test plan QC00002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QC00002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at ( T_A = 25°C ) for information purposes only.</td>
</tr>
</tbody>
</table>

## Electrical Characteristics (TA = 25°C, Vs = ±5, Iz = 1.6 mA) unless otherwise specified

### Power Supplies

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
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<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vs</td>
<td>( +15 )V, ( +5 )V</td>
<td>7.2</td>
<td>8.5</td>
<td>9.5</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Icc</td>
<td>( +15 )V, ( +5 )V</td>
<td>42.0</td>
<td>44.0</td>
<td>45</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Iee</td>
<td>( +15 )V, ( +5 )V</td>
<td>9.5</td>
<td>10.0</td>
<td>12</td>
<td>I</td>
<td>mA</td>
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<tr>
<td>V</td>
<td>( +15 )V, ( +5 )V</td>
<td>4.5</td>
<td>47</td>
<td>48</td>
<td>I</td>
<td>mA</td>
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### Multiplier Performance

<table>
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<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer Function (Note 5)</td>
<td>( (I_{XY} - I_{XV}) = K(I_X \times I_Y)/I_Z )</td>
<td>0.92</td>
<td>0.965</td>
<td>1.01</td>
<td>I</td>
<td>%FS</td>
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<tr>
<td>K Value</td>
<td></td>
<td>±0.5</td>
<td>±2</td>
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<td>I</td>
<td>%FS</td>
</tr>
<tr>
<td>Total Error (Note 1)</td>
<td>( -2 ) mA &lt; ( I_X, I_Y &lt; 2 ) mA</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>±1.5</td>
<td>±3</td>
<td>IV</td>
<td>%FS</td>
</tr>
<tr>
<td>Linearity (Note 2)</td>
<td></td>
<td>±25</td>
<td>±0.5</td>
<td></td>
<td>I</td>
<td>%FS</td>
</tr>
<tr>
<td>Bandwidth (Note 3)</td>
<td>( -3 ) dB (See Figure 2)</td>
<td>200</td>
<td>225</td>
<td></td>
<td>III</td>
<td>MHz</td>
</tr>
<tr>
<td>X Feedthrough DC to ( I_{XY} ) or ( I_{XV} ) (Note 5)</td>
<td>( I_X = \pm 2 ) mA, ( I_Y = 0 ) (unnulled)</td>
<td>0.15</td>
<td>1.6</td>
<td></td>
<td>I</td>
<td>%FS</td>
</tr>
<tr>
<td>Y Feedthrough DC to ( I_{XY} ) or ( I_{XV} ) (Note 5)</td>
<td>( I_X = \pm 2 ) mA, ( I_Y = 0 ) (unnulled)</td>
<td>0.15</td>
<td>1.6</td>
<td></td>
<td>I</td>
<td>%FS</td>
</tr>
<tr>
<td>AC Feedthrough, ( X ) to ( I_{XY} ) or ( I_{XV} ) (Note 4)</td>
<td>( f = 3.58 ) MHz</td>
<td>80</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
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<tr>
<td>AC Feedthrough, ( X ) to ( I_{XY} - I_{XV} ) (Note 4)</td>
<td>( f = 100 ) MHz</td>
<td>28</td>
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<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>AC Feedthrough, ( Y ) to ( I_{XY} ) or ( I_{XV} ) (Note 4)</td>
<td>( f = 3.58 ) MHz</td>
<td>64</td>
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<td></td>
<td>V</td>
<td>dB</td>
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<tr>
<td>AC Feedthrough, ( Y ) to ( I_{XY} - I_{XV} ) (Note 4)</td>
<td>( f = 100 ) MHz</td>
<td>26</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
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</table>

3-56
## Electrical Characteristics — Contd. \( (T_A = 25^\circ C, V_S = \pm 5, I_X = 1.6 \text{ mA}) \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs ((I_X, I_Y))</td>
<td>FRS = (1.25 \times I_Z) (Nominal)</td>
<td>\pm 2</td>
<td>I</td>
<td>mA</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Clipping Level (C_L = 2 \times I_Z)</td>
<td>2.85</td>
<td>3.2</td>
<td>I</td>
<td>mA</td>
<td>Ω</td>
<td>Ω</td>
</tr>
<tr>
<td>(Z_{IN}(I_X))</td>
<td>30</td>
<td>40</td>
<td>48</td>
<td>I</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>(Z_{IN}(I_Y))</td>
<td>30</td>
<td>36</td>
<td>48</td>
<td>I</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltages at Input Pins, (I_Z = 1.6 \text{ mA})</td>
<td>-4</td>
<td>+4</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>((V_{OSX}, V_{OSY}))</td>
<td>-12</td>
<td>+12</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Currents (I_{XO} - I_{YO}) (T_{MIN} \text{ to } T_{MAX})</td>
<td>±10</td>
<td>±40</td>
<td>I</td>
<td>μA</td>
<td>V</td>
<td>nA/°C</td>
</tr>
<tr>
<td>Nonlinearity</td>
<td>(I_X) (I_Y = 2 \text{ mA}, -2 \text{ mA} &lt; I_X &lt; 2 \text{ mA})</td>
<td>0.1</td>
<td>0.6</td>
<td>I</td>
<td>%FS</td>
<td></td>
</tr>
<tr>
<td>Distortion, (I_X) ((I_{XY} - I_X))</td>
<td>(f = 3.58 \text{ MHz})</td>
<td>-55</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distortion, (I_Y) ((I_{XY} - I_Y))</td>
<td>(f = 100 \text{ MHz})</td>
<td>-25</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distortion, (I_X) ((I_{XY} - I_X))</td>
<td>(f = 3.58 \text{ MHz})</td>
<td>-56</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distortion, (I_Y) ((I_{XY} - I_Y))</td>
<td>(f = 100 \text{ MHz})</td>
<td>-26</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distortion, (I_X) ((I_{XY} - I_X))</td>
<td>(f = 3.58 \text{ MHz})</td>
<td>-66</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distortion, (I_Y) ((I_{XY} - I_Y))</td>
<td>(f = 100 \text{ MHz})</td>
<td>-35</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diff Gain @3.58 MHz</td>
<td>(I_Z = 0.2 \text{ mA}, I_Y = 0.25 \text{ mA})</td>
<td>0.2</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_X) (I_Y = 0.2 \text{ mA}, I_Y = 0.25 \text{ mA})</td>
<td>0.17</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_Y) (I_X = 0.2 \text{ mA}, I_Y = 0.25 \text{ mA})</td>
<td>0.1</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_X) (I_Y = 1.6 \text{ mA}, I_Y = 2 \text{ mA})</td>
<td>0.05</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_Y) (I_X = 1.6 \text{ mA}, I_Y = 2 \text{ mA})</td>
<td>0.05</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diff Phase @3.58 MHz</td>
<td>(I_Z = 0.2 \text{ mA}, I_Y = 0.25 \text{ mA})</td>
<td>0.5</td>
<td>V</td>
<td>deg²</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_X) (I_Y = 0.2 \text{ mA}, I_Y = 0.25 \text{ mA})</td>
<td>0.5</td>
<td>V</td>
<td>deg²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_Y) (I_X = 0.2 \text{ mA}, I_Y = 0.25 \text{ mA})</td>
<td>0.5</td>
<td>V</td>
<td>deg²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_X) (I_Y = 1.6 \text{ mA}, I_Y = 2 \text{ mA})</td>
<td>0.05</td>
<td>V</td>
<td>deg²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_Y) (I_X = 1.6 \text{ mA}, I_Y = 2 \text{ mA})</td>
<td>0.05</td>
<td>V</td>
<td>deg²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outputs ((I_{XY}, I_{YX}))</td>
<td>(I_X = I_Y = 0)</td>
<td>-15</td>
<td>I</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diff Output (I_{DY} = (I_{XY} - I_{YX}))</td>
<td>±15</td>
<td>±120</td>
<td>I</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Compliance</td>
<td>±0.1</td>
<td>±80</td>
<td>I</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max Output Current Swing</td>
<td>±1.5</td>
<td>±2.0</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise Spectral Density</td>
<td>±2.85</td>
<td>±3.2</td>
<td>I</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Hz &lt; (f) &lt; 10 MHz</td>
<td>(R_L = 500 \Omega)</td>
<td>125</td>
<td>V</td>
<td>pA/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_S) (Bias)</td>
<td>Current Range</td>
<td>Tested</td>
<td>0.2</td>
<td>1.6</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>(I_Z = 0.2 \text{ mA})</td>
<td>±25</td>
<td>I</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>(I_Z = 1.6 \text{ mA})</td>
<td>±25</td>
<td>I</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Error is defined as the maximum deviation from the ideal transfer function expressed as a percentage of the full scale output.

Note 2: Linearity is defined as the error remaining after compensating for scale factor (gain) variation and input and output referred offset errors.

Note 3: Bandwidth is guaranteed using the squaring mode test circuit of Figure 4.

Note 4: Relative to full scale output with full scale sinewave on signal input and zero port input nulled. Specification represents feedthrough of the fundamental.

Note 5: Specifications are provisional for the EL4083.
AC Test Fixture

![AC Test Fixture Diagram]

Figure 2. AC Bandwidth Test Fixture

Burn-In Circuit

![Burn-In Circuit Diagram]

Figure 3. Burn-In Circuit P-DIP
**Figure 4**

8-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

\[ T_{j_{\text{max}}} = 150^\circ \text{C} \]
\[ \theta_{JA} = 103^\circ \text{C/W} \]

**Figure 5**

8-Lead SO
Maximum Power Dissipation vs Ambient Temperature

\[ T_{j_{\text{max}}} = 150^\circ \text{C} \]
\[ \theta_{JA} = 175^\circ \text{C/W} \]

**Figure 6.** (I_x, I_y Bandwidth vs I_z)

**Figure 7.** (I_x, I_y 1% Settling Time vs I_z)
Figure 8. Output Noise Density vs I_z Bias

Input Offset Trim(s)

```
+V_s
50k
-V_s
```

Output Offset Trim

```
+V_s
10k
-V_s
```

\[ R_{TI} = \frac{(V_s \times 1.6 \text{ mA})}{(16 \mu A \times I_z)} \]

\[ R_{TO} = \frac{(V_s \times 1.6 \text{ mA})}{(30 \mu A \times I_z)} \]

Figure 9. Optional External Trim Networks

Figure 10. V_{ZIN} vs I_z (Typical)

Figure 11. I_{ZIN} Bandwidth vs I_z
General Operating Information

**Iz Input (Bias, Divisor) and Power Supplies**

The Iz pin is a low impedance (<20Ω) virtual ground current input. It can accept positive current from a resistor connected to a positive voltage source or the positive supply. The instantaneous bias for the multiplier gain core is proportional to this current value. Negative applied current will put the multiplier portion of the circuit in a zero bias state and the voltage at the pin will be clamped at a diode drop below ground. The part will respond in a similar manner to currents from a current source such as the output of a transconductance amplifier or one of its own outputs. The overall transfer equation for the EL4083 is:

\[ K(IX \times IY)/IZ = (IXY-IXY), K \sim 1 \]

As can be seen from the equation, the Z input can serve as a divisor input. However, it is different from the other two inputs in that the value of its current determines the supply current of the part and the bandwidth and compliance range of the outputs and other two inputs. Table 1 gives the equations describing these and other important relationships. These dependencies can complicate and/or limit the usefulness of this pin as a computational input. The Iz dependence of the impedance of the multiplying inputs can be particularly troublesome. See the Iz divider and the RMS #2 circuit sections of the application note for some ways of dealing with this.

The primary intended use for the Z input is as a programming pin similar in function to those on programmable op amps. This enables one to trade off power consumption against bandwidth and settling time and allow the part to function within its power dissipation rating over its full operational supply range (±4.5V - ±16.5V). The E4083 has been designed to function well for Iz values in the range of 200 μA < Iz < 1.6 mA which corresponds to IX and IY signal bandwidths of about 50 MHz to over 200 MHz. Higher values of Iz may cause problems at temperature extremes while lower values down to zero will progressively degrade the input referred D.C. offsets and reduce speed. Below about 50 μA of bias current the internal servo amplifier loop which maintains the Iz pin at ground will lose regulation and the voltage at the pin will start to move negative (see Figure 10). This is accompanied by a significant increase in input impedance of the pin. Figure 11 shows the A.C. bandwidth of the Iz input as a function of the D.C. value of Iz. Figures 6 and 7 show the bandwidth and 1% settling time of the multiplying inputs, IX and IY, as functions of Iz.

**IX and IY (Multiplier) Inputs and Offset Trimming**

The IX and IY pins are low impedance (Iz dependent) virtual ground current inputs that accept bipolar signals. The input referred clip value is equal to Iz × 2 while the full scale value has been chosen to be 1.25 × Iz to maintain excellent distortion and linearity performance. Operating at higher full scale values will degrade these two pa-

<table>
<thead>
<tr>
<th>Table 1. Basic Design Equations and Relationships</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive Supply Current</td>
</tr>
<tr>
<td>Negative Supply Current</td>
</tr>
<tr>
<td>Power Dissipation (See Figures 4 and 5)</td>
</tr>
<tr>
<td>Multiplying Input(s) Impedance</td>
</tr>
<tr>
<td>Multiplying Input(s) Clip Point</td>
</tr>
<tr>
<td>Multiplying Input(s) Full Scale Value</td>
</tr>
<tr>
<td>Multiplying Input Resistor Values (In Terms of Peak Input Signal)</td>
</tr>
<tr>
<td>Full Scale Output (Single Ended)</td>
</tr>
<tr>
<td>Full Scale Output (Differential)</td>
</tr>
<tr>
<td>Iz (Bias) Input Voltage vs Iz</td>
</tr>
<tr>
<td>Iz Signal Bandwidth vs Iz</td>
</tr>
<tr>
<td>IX, IY Signal Bandwidth vs Iz</td>
</tr>
<tr>
<td>IX, IY 1% Settling Time vs Iz</td>
</tr>
<tr>
<td>IX+, IX- = 3.4 mA + Iz × 26</td>
</tr>
<tr>
<td>IX-, IX- = 4.5 mA + Iz × 27</td>
</tr>
<tr>
<td>PWR = (+VS - (-VS)) × (4 mA + Iz × 26.5)</td>
</tr>
<tr>
<td>RZX = RZY = (32fl) × 1.6 mA/Iz</td>
</tr>
<tr>
<td>IX (clip) = IY (clip) = Iz × 2</td>
</tr>
<tr>
<td>IX (fs) = IY (fs) = Iz × 1.25 (nominal)</td>
</tr>
<tr>
<td>Rx = VX (peak)/IX (fs)</td>
</tr>
<tr>
<td>Ry = VY (peak)/IY (fs)</td>
</tr>
<tr>
<td>IXV = IXV = IX (fs) × IY (fs)/(Ix × 2)</td>
</tr>
<tr>
<td>(IXY - IXY) = IX (fs) × IY (fs)/Iz</td>
</tr>
<tr>
<td>(See Figure 10)</td>
</tr>
<tr>
<td>(See Figure 11)</td>
</tr>
<tr>
<td>(See Figure 6)</td>
</tr>
<tr>
<td>(See Figure 7)</td>
</tr>
</tbody>
</table>
As mentioned, the output referred offset only affects D.C. accuracy which may not be an issue in A.C. applications. In gain control applications one may only need to null feedthrough with respect to the gain control input.

In gain control (VCA) applications the X input should be used as the control input and the signal applied to the Y input since it has slightly higher bandwidth and better linearity and distortion performance.

**Current Outputs (Iₓᵧ, Iₓᵧ), Feedthrough and Distortion**

Another unique feature of the EL4083 is the differential ground referenced current output structure. These outputs can drive 50Ω terminated lines and reactive loads such as transformers, baluns, and LC tank and filter circuits directly.* Unlike low impedance follower buffers, these outputs do not interact with the load to produce ringing or instability. If a high level low impedance output is required, the outputs can be recovered differentially and converted to a single ended output with a fast op amp such as the EL2075 (see Figure 19). The outputs can also drive current input devices such as CMF amps, current conveyors and its own inputs directly by simple connection.

Figures 12 and 14 show the nulled gain and feedthrough characteristics of the Iₓᵧ and Iₓᵧ outputs which are virtually identical and differ only in phase. Figure 12 is with the A.C. signal applied to the X input with Y used as the gain control and in Figure 14 these signals are reversed. Note that in both cases the signal feedthrough rolls up and peaks near the cutoff frequency. This is quite typical of the performance of all previous four quadrant multipliers. Figures 13 and 15 show the corresponding gain/feedthrough characteristics for the differentially recovered output signal Iₓᵧ-Iₓᵧ. Note that in this case the peak feedthrough at high frequencies is lower by more than 40 dB.

* See EL2082 Data Sheet—Receiver IF Amplifier (Figure 19). The EL2082 also has a current output.
General Operating Information
— Contd.
Figures 16 and 17 show the total harmonic distortion for the single-ended and differential recovered outputs for a full scale A.C. input signal on one input and a full scale D.C. control signal on the other. Note that above about one megahertz to the cutoff frequency the THD of the differentially recovered signal is as much as 10 dB lower than the single-ended signals.
General Operating Information — Contd.

Figure 12. Nulled $I_{XY}$ and $I_{XY}$ Frequency Response (Signal on XIN, Gain Controlled by YIN)

Figure 13. Nulled ($I_{XY}$-$I_{XY}$) Frequency Response (Signal on XIN, Gain Controlled by YIN)

Figure 14. Nulled $I_{XY}$ and $I_{XY}$ Frequency Response (Signal on YIN, Gain Controlled by XIN)

Figure 15. Nulled ($I_{XY}$-$I_{XY}$) Frequency Response (Signal on YIN, Gain Controlled by XIN)

Figure 16. (Full Level XIN THD vs Frequency)

Figure 17. (Full Level YIN THD vs Frequency)
Applications

Basic Product Functions
Figures 18 and 19 are the basic schematics for many of the applications of the EL4083. These can perform signal mixing, frequency doubling, modulation, demodulation, gain control/voltage-controlled amplification, multiplication and squaring. Figure 18 has resistively terminated differential outputs and has the widest bandwidth. The figure also shows the option of using the EL2260 dual CMF amplifier to recover the outputs differentially at very low impedance. This has a maximum 3 dB bandwidth of 130 MHz and settles to 1% in 25 ns. Figure 19 uses an EL2075 at the outputs as a differential to single ended converter with gain to take advantage of the performance enhancements of the differentially recovered output mentioned above and to provide a high level low impedance drive. The -3 dB bandwidth of this circuit is over 150 MHz using good layout techniques. However, to achieve this bandwidth one must restrict the output swing to little more than 1 Vpp to avoid running into the 500V/μs minimum slew rate of the EL2075. Table 2 shows the input signal assignments for the applications listed above.

<table>
<thead>
<tr>
<th>Application</th>
<th>VX</th>
<th>VY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mixer</td>
<td>Signal 1</td>
<td>Signal 2</td>
</tr>
<tr>
<td>Frequency Doubler</td>
<td>Signal</td>
<td>Signal</td>
</tr>
<tr>
<td>Modulator</td>
<td>Modulating Signal</td>
<td>Carrier</td>
</tr>
<tr>
<td>Demodulator</td>
<td>Local Oscillator</td>
<td>Modulated Signal</td>
</tr>
<tr>
<td>Gain Control/VCA</td>
<td>Gain Control</td>
<td>Signal</td>
</tr>
<tr>
<td>Multiplier</td>
<td>Signal 1</td>
<td>Signal 2</td>
</tr>
<tr>
<td>Squarer</td>
<td>Signal</td>
<td>Signal</td>
</tr>
</tbody>
</table>

*X means not connected if function is not used.
Applications — Contd.

\[ I_Z = \frac{V_{CC}}{R_Z} \]
\[ R_X = V_X (\text{MAX}) / (1.25 \times I_Z) \]
\[ R_Y = V_Y (\text{MAX}) / (1.25 \times I_Z) \]

*1. 51Ω Resistors omitted when using EL2260

*2. Optimum value of RF determined by supplies and amount or tolerable peaking

\((-3\, \text{dB BW} \sim 90\, \text{MHz} \at \pm 5V, \, \text{BW} \sim 150\, \text{MHz} @ \pm 15V)\)

**Figure 18. Basic Schematic (Dual Diff Outs)**

\[ I_Z = \frac{V_{CC}}{R_Z} \]
\[ R_X = V_X (\text{MAX}) / (1.25 \times I_Z) \]
\[ R_Y = V_Y (\text{MAX}) / (1.25 \times I_Z) \]

*Optimized for Wide Bandwidth

**Figure 19. Basic Schematic (Single Ended Converted)**

(150 MHz VCA)
**Other Applications**

Elantec has also published an applications note covering other applications of the EL4083. These include dividers, squaring and square rooting circuits, several RMS and power measurement circuits, and a wideband AGC circuit. Also presented are two polynomial computation examples for video and some HDTV quality fader and summing circuits. The EL4083 has been found flexible enough to easily implement all of the classic four quadrant multiplier applications and also offer interesting new applications possibilities.

### EL4083 Macromodel

This macromodel is compatible with PSPICE (copywritten by Microsim Corporation). It has been designed to work accurately for fixed values of $I_Z$ (bias) in the range of 200 $\mu$A to 1.6 mA. The additional simulation burden imposed by including provision for a time varying $I_Z$ was thought not worthwhile. The value of $I_Z$ is specified to the model by the parameter $NS$. The relation between $I_Z$ and $NS$ is: $I_Z = 200 \mu$A $\times$ NS. All other inputs can accept time varying signals.

The model will provide good transient and frequency response and settling time estimates as well as time domain switching results. Input and output impedance and overload responses are correctly modeled. The D.C. current drawn from supplies for a given value of $I_Z$ is also correct.

Noise, PSRR and the temperature dependence of A.C. parameters such as frequency response and settling time are not modeled. Linearity and distortion results from the model will be worse than the real part by about a factor of three and do not show the correct frequency dependence.

The macromodel is constructed from simple controlled sources, passive components and stripped transistor and diode models. As such it should be usable, perhaps with slight modification, on all but student or demonstration simulators where the model’s size may be a problem.

---

**Macromodel**

*EL4083 Macromodel
*Revision A, August 22, 1994

*Connection: IZ(BIAS)
*IX(in)
*IV(in)
*VEE
*VCC
*IXY

.subckt EL4083 ZIN XIN YIN VEE VCC IXY IVX

.MODEL M1MP5DIODE D TT=60p IS=1f CJ=300f VJ=600m XTI=3 EG=1.11 RS=80m

.MODEL M2MDCAP D TT=100n IS=2e-17 CJ=1p VJ=800m RS=300

.MODEL M3MNP1 NPN CJC=1.3p TF=120p IS=1.0f BF=120 CJS=480f

.MODEL M4MNP1 PNP CJC=1.79p TF=50.166666666667 IS=1f BF=90 CJS=480f

C1 N9 N7 9p C2 N7 0 350f C3 N19 N16 9p C4 N16 0 350f
Macromodel — Contd.

EV95 VBP 0 N42 0 1
EV96 N54 0 N21 0 650m
EV97 N55 0 N11 0 650m
EV98 N27 0 N28 0 1
EV99 N29 0 SWIN 0 1
FI10 VN-VEE VF110 1
FI11 VCC VP-VF111 1
FI12 VCC N39 VF112 1
FI13 N37 VEE VF113 1
FI14 VCC N38 VF114 1
FI15 N36 VEE VF115 1
FI16 N45 VEE VF116 1
FI17 VCC N42 VF117 1
FI18 N37 N36 VF118 500m
FI19 N38 N39 VF119 500m
FI20 VN+ VN- VF120 500m
FI21 VP+ VP- VF121 500m
FI22 0 N21 VF122 1
FI23 N21 0 VF123 1
FI24 N24 0 VF124 2
FI25 N14 0 VF125 2
FI26 N11 0 VF126 1
FI27 0 N11 VF127 1
FI28 VCC VEE VF128 21
FI29 N28 ZB1 VF129 1
FI30 N33 0 VF13 1
FI60 N33 VF16 1
FI70 N35 N34 VF17 1
FI80 VN+ VEE VF18 1
FI90 VCC VP+ VF19 1
IIBGN 0 VEE 2.2m
IIBGP VCC 0.246m
IIISWB N32 VEE 629u
IIISWI SWIN VEE 555u
IIZSU N28 VEE 10u
L1 N7 IXA 71n
L2 XIN N7 4n
L3 N16 IYA 71n
L4 YIN N16 4n
L5 N46 IYX 4n
L6 N47 IXY 4n
Q10 N10 VP+ [VEE] M4MNP1 2
Q10 N46 VN+ N36[VEE] M3MNP1 2
Q11 N47 VN+ N37 [VEE] M3MNP1 2
Q12 N46 VN- N37 [VEE] M3MNP1 2
Q13 0 N34 N56 [VEE] M4MNP1 400m
Q14 0 N24 N57 [VEE] M4MNP1 400m
Q15 0 N35 N58 [VEE] M3MNP1 400m
Q16 0 N35 N59 [VEE] M3MNP1 400m
Q2 0 N10 VP- [VEE] M4MNP1 2
Q3 0 N20 VN+ [VEE] M3MNP1 2
Q4 0 N20 VN- [VEE] M3MNP1 2
Q5 N46 VP- N39 [VEE] M4MNP1 2
Q6 N47 VP+ N39 [VEE] M4MNP1 2
Q7 N46 VP+ N38 [VEE] M4MNP1 2
Q8 N47 VP- N38 [VEE] M4MNP1 2
Q9 N47 VN- N36 [VEE] M3MNP1 2
R1 N15 N7 60 TC=824u 7.67u
R10 N16 N17 450 TC=0 0
R11 YIN N16 100 TC=0 0
R12 0 SWIN 500 TC=824u 7.67u
R13 N56 N38 35 TC=0 0
R14 N57 N39 35 TC=0 0
R15 N37 N38 35 TC=0 0
R16 N36 N59 35 TC=0 0
R17 N46 IYX 100 TC=0 0
R18 N47 IXY 100 TC=0 0
R2 N11 IXC 6.25 TC=0 0
R3 N9 IXC 4.5 TC=0 0
R4 N7 IAX 1.5k TC=0 0
R5 XIN N7 100 TC=0 0
R6 N25 N16 156 TC=824u 7.76u
R7 N21 IYC 6.25 TC=0 0
R8 ITC N19 45 TC=0 0
R9 N17 IYA 45 TC=0 0
RSU VEE 0 16K TC=0 0
VF110 N43 N44 0.0
VF111 N40 N41 0.0
VF112 ZB4 ZB5 0.0
VF113 ZB5 ZB6 0.0
VF114 ZB3 ZB4 0.0
VF115 ZB6 ZB7 0.0
VF116 N44 ZB9 0.0
VF117 N41 ZB8 0.0
VF118 IYB IYC 0.0
VF119 IYA IYB 0.0
VF120 IXB IXC 0.0
VF121 IXA IXB 0.0
VF122 N22 N24 0.0
VF123 N23 N24 0.0
VF124 ZB2 ZB3 0.0
VF125 ZB1 ZB2 0.0
VF126 N13 N14 0.0
VF127 N12 N14 0.0
VF128 ZB9 VEE 0.0
VF129 ZIN N26 0.0
VF15 N30 N32 0.0
VF16 N31 N32 0.0
VF17 N33 0 0.0
VF18 ZB8 N43 0.0
VF19 ZB7 N40 0.0
..ENDS

3-69
Features
• Complete video level restoration system
• 0.02% differential gain and 0.05° differential phase accuracy at NTSC
• 60 MHz bandwidth
• 0.1 dB flatness to 10 MHz
• $V_S = \pm 5V$ to $\pm 15V$
• TTL/CMOS hold signal

Applications
• Input amplifier in video equipment
• Restoration amplifier in video mixers

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1A089CN</td>
<td>0°C to +75°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>E1A089CS</td>
<td>0°C to +75°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

General Description

The EL4089C is an 8-pin complete DC-restored monolithic video amplifier sub-system. It contains a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance.

When the HOLD logic input is set to a TTL/CMOS logic 0, the sample- and-hold amplifier can be used to null the DC offset of the video amplifier.

When the HOLD input goes to a TTL/CMOS logic 1, the correcting voltage is stored on the video amplifier's input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.

The video amplifier is optimized for video performance and low power. Its current feedback design allows the user to maintain essentially the same bandwidth over a gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

The EL4089C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089C is specified for operation over 0°C to +75°C temperature range.

Connection Diagram

DC restoring amplifier with a gain of 2, restoring to ground.
### Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ and V−</td>
<td>Voltage between V+ and V−</td>
<td>33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN+, S/HIN+, and GND pins</td>
<td>Voltage between VIN+, S/HIN+, and GND pins</td>
<td>(V+) + 0.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V−) − 0.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOUT Current</td>
<td>Current into VIN− and HOLD</td>
<td>60 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 mA</td>
<td>Internal Power Dissipation</td>
<td>Sec Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Tj = Tc = TA.

**Test Level**

- **I:** 100% production tested and QA sample tested per QA test plan QCX0002.
- **II:** 100% production tested at TA = 25°C and QA sample tested at TA = 25°C.
- **III:** TMAX and Tmin per QA test plan QCX0002.
- **IV:** QA sample tested per QA test plan QCX0002.
- **V:** Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **VI:** Parameter is typical value at TA = 25°C for information purposes only.

### Open Loop DC Electrical Characteristics

Provisional Supplies at ±15V, Load = 1 kΩ; TA = +25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>+25°C</td>
<td>12</td>
<td>25</td>
<td></td>
<td>II</td>
<td>mV</td>
</tr>
<tr>
<td>IB+</td>
<td>IN+ Input Bias Current</td>
<td>+25°C</td>
<td>1</td>
<td>5</td>
<td></td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>IB−</td>
<td>IN− Input Bias Current</td>
<td>+25°C</td>
<td>18</td>
<td>150</td>
<td></td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>ROL</td>
<td>Transimpedance (Note 1)</td>
<td>+25°C</td>
<td>180</td>
<td>800</td>
<td></td>
<td>II</td>
<td>kΩ</td>
</tr>
<tr>
<td>RIN−</td>
<td>IN− Resistance</td>
<td>+25°C</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>Ω</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>+25°C</td>
<td>44</td>
<td>60</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td>+25°C</td>
<td>±12</td>
<td>±13</td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>ISC</td>
<td>Short Circuit Current</td>
<td>+25°C</td>
<td>45</td>
<td>100</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Restoration Section**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS, Comp</td>
<td>Composite Input Offset Voltage (Note 3)</td>
<td>+25°C</td>
<td>3</td>
<td>7</td>
<td></td>
<td>II</td>
<td>mV</td>
</tr>
<tr>
<td>IB+,r</td>
<td>Restore In+ Input Bias Current</td>
<td>+25°C</td>
<td>3</td>
<td>12</td>
<td></td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>IOUT</td>
<td>Restoring Current Available</td>
<td>+25°C</td>
<td>180</td>
<td>300</td>
<td></td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio (Note 2)</td>
<td>+25°C</td>
<td>60</td>
<td>70</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
</tbody>
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---

3-71
Open Loop DC Electrical Characteristics — Contd.
Provisional Supplies at ±15V, Load = 1 kΩ; T_A = +25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test</th>
<th>Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Restore Section</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Note 4)</td>
<td>+25°C</td>
<td>60</td>
<td>90</td>
<td>II</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_THRESHOLD</td>
<td>HOLD Logic Threshold</td>
<td>+25°C</td>
<td>0.8</td>
<td>2.0</td>
<td>II</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_HL, Hold</td>
<td>HOLD Input Current @ Logic High</td>
<td>+25°C</td>
<td>1</td>
<td>5</td>
<td>II</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_HL, Hold</td>
<td>HOLD Input Current @ Logic Low</td>
<td>+25°C</td>
<td>5</td>
<td>15</td>
<td>II</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isy, Hold</td>
<td>Supply Current (HOLD = 5V)</td>
<td>+25°C</td>
<td>4.8</td>
<td>6.0</td>
<td>9.0</td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Isy, Sampling</td>
<td>Supply Current (HOLD = 0V)</td>
<td>+25°C</td>
<td>5.0</td>
<td>6.5</td>
<td>11.0</td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

Closed Loop AC Electrical Characteristics
Provisional Supplies at ±15V, Load = 150Ω and 15 pF. R_f and R_g = 300Ω; A_V = 2, T_A = 25°C. (See Note 7 about Test Fixture)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test</th>
<th>Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifier Section</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (Note 5)</td>
<td>500</td>
<td></td>
<td></td>
<td>V</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate with ±5V Supplies (Note 5)</td>
<td>275</td>
<td></td>
<td></td>
<td>V</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth ±3 dB</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth ±0.1 dB</td>
<td>25</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain at 3.58 MHz (Note 6)</td>
<td>V_S = ±15V</td>
<td>0.02</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dPh</td>
<td>Differential Phase at 3.58 MHz (Note 6)</td>
<td>V_S = ±5V</td>
<td>0.03</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Restore Section</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Restore Amplifier Slew Rate (Test Circuit) 20%–80%</td>
<td>25</td>
<td></td>
<td></td>
<td>V</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>T_HE</td>
<td>Time to Enable Hold</td>
<td>25</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>T_HD</td>
<td>Time to Disable Hold</td>
<td>40</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: For current feedback amplifiers, A_VOL = R_OI/R_IN. .
Note 2: V_CM = ±10V for V_S = ±15V.
Note 3: Measured from S/H Input to amplifier output, while restoring.
Note 4: V_OS is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.
Note 5: SR measured at 20% to 80% of a 4V pk-pk square wave.
Note 6: DC offset from ~0.714V through +0.714V, ac amplitude is 286 mVp-p, equivalent to 40 mV.
Note 7: Test fixture was designed to minimize capacitance at the IN – input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.
Typical Performance Curves

Supply Current vs Temperature

Supply Current vs Supply Voltage

Restoring Current vs Temperature

Amplifier Input Current vs Die Temperature

Amplifier Offset Voltage vs Die Temperature

Amplifier Output Voltage vs Die Temperature; $V_S = \pm 15V$
**Typical Performance Curves — Contd.**

- **CMRR for Amplifier and Restore Section vs Die Temperature**
- **Transimpedance ($R_{OL}$) vs Die Temperature**
- **Relative Frequency Response for Various Gains, $R_F = 300\,\Omega$**
- **Frequency Response vs Supply $A_V = 2; R_F = 300$**
- **Frequency Response Flatness vs Supply $A_V = 2; R_F = 300$**
- **Frequency Response Flatness for Various Load and Supply Conditions $A_V = 2; R_F = 300$**
Typical Performance Curves — Contd.

Frequency Response Flatness vs $C_{IN}$: $A_V = 2; R_F = 300$

Differential Gain vs DC Input Offset; $A_V = 2; F_O = 3.58\, MHz; R_L = 150\Omega$

Differential Phase vs DC Input Offset; $A_V = 2; F_O = 3.58\, MHz; R_L = 150\Omega$

8-Pin Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

8-Lead SO
Maximum Power Dissipation vs Ambient Temperature
**Typical Application**

The EL4089 can be used to DC-restore a video waveform (see Fig. 1). The above circuit forces the cable driving video amplifier's output to ground when the HOLD pin is at a logic low.

The "correction voltage" is stored on capacitor CX1, an external ceramic capacitor. The capacitor value is chosen from the system requirements. The typical input bias current to the video amplifier is 1 μA, so for a 62 μs hold time, and a 0.01 μF capacitor, the output voltage drift is 6.2 mV in one line.

The S/H amplifier can provide a typical current of 300 μA to charge capacitor CX1, so with a 1.2 μs sampling time, the output can be corrected by 36 mV in each line.

Using a smaller value of CX1 increases both the voltage that can be corrected, and the drift while being held, likewise, using a larger value of CX1, reduces the voltages.

The RX1 resistor is in the circuit purely to simulate some external source impedance, and is not needed as a real component. Likewise for RX2. The 75Ω back terminating resistor RXT is recommended when driving 75Ω cables.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the VIN- pin, (pin 1). This helps to minimize the stray capacitance on pin 1.

Power supply bypassing is important, and a 0.1 μF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7 μF tantalum bead capacitor, is recommended.

When both digital and Analog grounds are on the same board, the EL4089 should be on the Analog ground. The digital ground can be connected to the Analog ground through a 100Ω–300Ω resistor, near the EL4089. This allows the digital signal a return path, while preventing the digital noise from corrupting the analog ground.
Table of Charge Storage Capacitor vs Droop Charging Rates

<table>
<thead>
<tr>
<th>Cap Value nF</th>
<th>Droop in 60 µs mV</th>
<th>Charge in 1.2 µs mV</th>
<th>Charge in 4 µs mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>6</td>
<td>36</td>
<td>120</td>
</tr>
<tr>
<td>33</td>
<td>1.8</td>
<td>11</td>
<td>36</td>
</tr>
<tr>
<td>100</td>
<td>0.6</td>
<td>3.6</td>
<td>12</td>
</tr>
</tbody>
</table>

Basic formulae are:

\[ V \text{ (droop)} = I_b \times \frac{\text{Line time} - \text{Sample time}}{\text{Capacitor}} \]

\[ V \text{ (charge)} = I_{\text{OUT}} \times \frac{\text{Sample time}}{\text{Capacitor}} \]

For best results the source impedance should be kept low, using a buffer for example.

Because the S/H effectively shorts the input signal during Sample, the input should not be sampled during active video. Typically the sample is made during the back porch period of horizontal blanking. For this reason color composite signals, which have color burst on the back porch, can not be passed. See EL2090 or EL4093 for this application.
**General Description**

The EL4093C is a complete DC-restored video amplifier subsystem, featuring low power consumption and high slew rate. It contains a current feedback amplifier and a sample and hold amplifier designed to stabilize video performance. When the HOLD logic input is low, the sample and hold may be used as a general purpose op amp to null the DC offset of the video amplifier. When the HOLD input goes high, the sample and hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent video scan line.

The sample and hold amplifier contains a current output stage that greatly simplifies its connection to the video amplifier. Its high output impedance also helps to preserve video linearity at low supply voltages. For ease of interfacing, the HOLD input is TTL-compatible. This device has an operational temperature of \(-40°C\) to \(+85°C\) and is packaged in plastic 16-pin DIP and 16-lead SOIC.

**Connection Diagram**

![Connection Diagram](image)

**Features**

- High accuracy DC restoration for video
- Low supply current of 9.5 mA typ.
- 300 MHz bandwidth
- 1500V/μs slew rate
- 0.04% differential gain and 0.02° differential phase into 150Ω for NTSC
- 1.5 mV max. restored DC offset
- Sample and hold amplifier with fast enable and low leakage
- TTL-compatible HOLD logic input

**Applications**

- Input amplifier in video equipment
- Restoration amplifier in video mixers

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4093CN</td>
<td>(-40°C) to (+85°C)</td>
<td>16-pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL4093CS</td>
<td>(-40°C) to (+85°C)</td>
<td>16-Lead SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

**Demo Board**

A demo PCB is available for this product. Request "EL4093 Demo Board."
Absolute Maximum Ratings

- **Vs**: V+ to V− Supply Voltage 12.6V
- **VHOLD**: Voltage at HOLD input $(DGND - 0.7)$ to $(DGND + 5.5V)$
- **VIN**: Voltage at any other input V+ to V− ±8V
- **ΔVIN**: Difference between Sample and Hold inputs ±8V
- **IOUT1**: Video amplifier output current ±30mA
- **IOUT2S/H**: Amplifier output current ±10mA
- **IIN**: Maximum current into other pins ±6mA
- **PD**: Maximum Power Dissipation See Curves
- **TA**: Operating Ambient Temperature Range $-40°C$ to $+85°C$
- **TJ**: Operating Junction Temperature $150°C$
- **TST**: Storage Temperature Range $-65°C$ to $+150°C$

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level
- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$,
- **TMAX** and **TMIN** per QA test plan QCX0002.
- **III**: QA sample tested per QA test plan QCX0002.
- **IV**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open-Loop DC Electrical Characteristics  Power supplies at ±5V, $T_A = 25°C$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;s,HOLD&lt;/sub&gt;</td>
<td>Total Supply current in HOLD mode</td>
<td>9.5</td>
<td>11.5</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;s,SAMPLE&lt;/sub&gt;</td>
<td>Total Supply current in SAMPLE mode</td>
<td>8.5</td>
<td>10.5</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

Video Amplifier Section (Not Restored)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Input Offset Voltage</td>
<td>10</td>
<td>110</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;B+&lt;/sub&gt;</td>
<td>Non-Inverting Input Bias Current</td>
<td>10</td>
<td>25</td>
<td>I</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;B−&lt;/sub&gt;</td>
<td>Inverting Input Bias Current</td>
<td>15</td>
<td>50</td>
<td>I</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Transimpedance</td>
<td>150</td>
<td>400</td>
<td>I</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;O&lt;/sub&gt;</td>
<td>Output Voltage Swing</td>
<td>±3</td>
<td>±3.5</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;SC&lt;/sub&gt;</td>
<td>Output Short-Circuit Current</td>
<td>60</td>
<td>100</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
**Open-Loop DC Electrical Characteristics**

Power supplies at ±5V, T<sub>A</sub> = 25°C — Contd.

### Sample and Hold Section

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Input Offset Voltage</td>
<td>0.5</td>
<td>1.5</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>TCV&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Average Offset Voltage Drift</td>
<td>6</td>
<td></td>
<td>V</td>
<td>μV/°C</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;H&lt;/sub&gt;</td>
<td>Input Bias Current</td>
<td>1</td>
<td>2</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Input Offset Current</td>
<td>10</td>
<td>200</td>
<td>I</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>TCI&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Average Offset Current Drift</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td>nA/°C</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;CM&lt;/sub&gt;</td>
<td>Common Mode Input Range</td>
<td>±2.5</td>
<td>±2.8</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>g&lt;sub&gt;m&lt;/sub&gt;</td>
<td>Transconductance (R&lt;sub&gt;L&lt;/sub&gt; = 500Ω)</td>
<td>5</td>
<td>15</td>
<td>I</td>
<td>A/V</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio (V&lt;sub&gt;CM&lt;/sub&gt; = -2.5V to +2.5V)</td>
<td>70</td>
<td>90</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>HOLD Logic Input Low (referenced to Digital GND)</td>
<td></td>
<td>0.8</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>HOLD Logic Input High (referenced to Digital GND)</td>
<td>2.0</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;GND&lt;/sub&gt;</td>
<td>Digital GND Reference Voltage</td>
<td>(V&lt;sub&gt;−&lt;/sub&gt;)</td>
<td>(V&lt;sub&gt;+&lt;/sub&gt;) - 4.0</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;DROOP&lt;/sub&gt;</td>
<td>Hold Mode Droop Current</td>
<td>10</td>
<td>70</td>
<td>I</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;CHARGE&lt;/sub&gt;</td>
<td>Charge Current Available to C&lt;sub&gt;HOLD&lt;/sub&gt;</td>
<td>±5.5</td>
<td>±8.5</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;O&lt;/sub&gt;</td>
<td>Output Voltage Swing (R&lt;sub&gt;L&lt;/sub&gt; = 10kΩ)</td>
<td>±3</td>
<td>±3.5</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;O&lt;/sub&gt;</td>
<td>Output Current Swing (R&lt;sub&gt;L&lt;/sub&gt; = 0Ω)</td>
<td>±4.5</td>
<td>±5.5</td>
<td>I</td>
<td>mA</td>
<td></td>
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</tbody>
</table>

**Closed-Loop AC Electrical Characteristics**

Power supplies at ±5V, T<sub>A</sub> = 25°C, R<sub>F</sub> = R<sub>G</sub> = 750Ω, R<sub>L</sub> = 150Ω, C<sub>L</sub> = 5 pF, C<sub>IN</sub>−(parasitic) = 1.8 pF

### Video Amplifier Section

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Levels</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW, -3 dB</td>
<td>-3 dB Small-Signal Bandwidth</td>
<td>300</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>BW, ±0.1 dB</td>
<td>0.1 dB Flatness Bandwidth</td>
<td>50</td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Peaking</td>
<td>Frequency Response Peaking</td>
<td>0</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate, V&lt;sub&gt;OUT&lt;/sub&gt; between −2V and +2V</td>
<td>1500</td>
<td></td>
<td>V</td>
<td>V/μs</td>
<td></td>
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<tr>
<td>dG</td>
<td>Differential Gain Error, V&lt;sub&gt;offset&lt;/sub&gt; between −714 mV and +714 mV</td>
<td>0.04</td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
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<tr>
<td>dθ</td>
<td>Differential Phase Error, V&lt;sub&gt;offset&lt;/sub&gt; between −714 mV and +714 mV</td>
<td>0.02</td>
<td></td>
<td>V</td>
<td>°</td>
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</tbody>
</table>
Closed-Loop AC Electrical Characteristics

Power supplies at ±5V, \( T_A = 25^\circ C \), \( R_F = R_G = 750 \Omega \), \( R_L = 1500 \Omega \), \( C_L = 5 \, \text{pF} \), \( C_{\text{HOLD}} = 2.2 \, \text{nF} \)

Sample and Hold Section

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Levels</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Delta I_{\text{STEP}} )</td>
<td>Change in Sample to Hold Output Current Due to Hold Step</td>
<td>0.1</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \Delta T_{\text{SH}} )</td>
<td>Sample to Hold Delay Time</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \Delta T_{\text{HS}} )</td>
<td>Hold to Sample Delay Time</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
| \( T_{\text{AC}} \) | Settling Time to 1% (DC Restored Amplifier Output)  
Video Amplifier Input from 0 to 1V | 2.2 |  |  |  | V | \( \mu s \) |

Typical Application

![Typical Application Diagram](image-url)
Typical Performance Curves

Non-inverting Frequency Response (Gain)

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = +1$
- $A_v = +5$
- $A_v = +2$

Frequency (Hz)

Non-inverting Frequency Response (Phase)

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = +1$
- $A_v = +2$
- $A_v = +5$

Phase (°)

Frequency Response for Various $R_L$

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = +1$
- $A_v = +2$

Frequency (Hz)

Inverting Frequency Response (Gain)

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = -1$
- $A_v = -2$
- $A_v = -5$

Frequency (Hz)

Inverting Frequency Response (Phase)

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = -1$
- $A_v = -2$
- $A_v = -5$

Phase (°)

Frequency Response for Various $R_L$

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = +1$
- $A_v = +2$

Frequency (Hz)

Frequency Response for Various $C_{IN}$

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = +1$
- $A_v = +2$

Frequency (Hz)

Frequency Response for Various $C_L$

- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = +1$
- $A_v = +2$

Frequency (Hz)

3 dB Bandwidth vs Temperature (Video Amp)

- $A_v = +2$
- $R_f = 750\Omega$
- $R_c = 150\Omega$
- $A_v = +2$
- $R_f = 750\Omega$
- $R_c = 150\Omega$

Frequency (MHz)

Die Temperature (°C)
Typical Performance Curves — Contd.

1. **Peaking vs Temperature (Video Amp)**
   - $a_v = +2$
   - $R_f = 750 \Omega$
   - $R_L = 1500 \Omega$

2. **Output Voltage Swing vs Frequency**
   - $a_v = +2$
   - $R_f = 750 \Omega$
   - $R_L = 1500 \Omega$

3. **2nd and 3rd Harmonic Distortion vs Frequency**
   - $a_v = +2$
   - $R_f = 1500 \Omega$
   - $Y_0 = 2 Y_{p-p}$

4. **Voltage and Current Noise vs Frequency**
   - $V_{n,0}$
   - $I_{n,0}$

5. **Supply Current vs Temperature**
   - Hold Mode
   - Sample Mode

6. **Input Offset Voltage vs Die Temperature (Video Amp, 3 Sample)**

7. **Input Bias Current vs Temperature (Video Amp)**

8. **Transimpedance vs Temperature (Video Amp)**

---

44093-13, 44093-14, 44093-15, 44093-16, 44093-17, 44093-18, 44093-19, 44093-20
Typical Performance Curves — Contd.

Input Offset Voltage vs Die Temperature (Sample & Hold, 3 Samples)

Input Bias Current vs Die Temperature (Sample & Hold)

Transconductance vs Die Temperature (Sample & Hold)

Transconductance vs Die Temperature (Sample & Hold)

Transconductance vs Die Temperature (Sample & Hold)

Output Current Swing vs Temperature (Sample & Hold)

Droop Current vs Temperature (Sample & Hold)

Charge Current vs Temperature (Sample & Hold)

Hold Step (ΔIOUT) vs Temperature

Input Offset Voltage

Input Bias Current

Transconductance

Droop Current

Charge Current

Hold Step

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)

Die Temperature (°C)
Typical Performance Curves — Contd.

**Differential Gain and Phase vs DC Input Voltage at 3.58 MHz**

- **Input:** $A_V = +2$, $R_F = R_G = 750\, \Omega$, $R_L = 150\, \Omega$

**Slew Rate vs Die Temperature (Video Amp)**

- **Output:** $A_V = +2$, $R_F = R_G = 750\, \Omega$, $R_L = 150\, \Omega$

**Settling Time vs Settling Accuracy (Video Amp)**

- **Output:** $A_V = +2$, $R_F = R_G = 750\, \Omega$, $R_L = 150\, \Omega$

**Maximum Power Dissipation vs Ambient Temperature, 16-Pin P-DIP Package**

- **Output:** $T_{JAX} = 150^\circ C$, $q_JA = 63^\circ C/W$

**Maximum Power Dissipation vs Ambient Temperature, 16-Pin SO Package**

- **Output:** $T_{JAX} = 150^\circ C$, $q_JA = 120^\circ C/W$
Applications Information

Product Description
The EL4093C is a high speed DC-restore system containing a current feedback amplifier (CFA) and a sample & hold (S/H) amplifier. The CFA offers a wide 3 dB bandwidth of 300 MHz and a slew rate of 1500 V/µs, making it ideal for high speed video applications such as SVGA. The CFA's excellent differential gain and phase at 3.58 MHz also makes it suitable for NTSC applications. Drawing only 9.5 mA on ±5V supplies, the EL4093C serves as an excellent choice for those applications requiring both low power and high bandwidth.

The connection between the CFA and sample & hold (the Autozero interface) has been greatly simplified. The output of the sample & hold is a high impedance current source, allowing direct connection to the CFA inverting input for autozero purposes. In addition, special circuitry within the sample & hold provides a charge current of 8.5 µA in sample mode, resulting in a sample hold current ratio (ratio of charging current to droop current) of approx. 1,000,000.

Theory of Operation
In video applications, DC restoration moves the backporch or black level to a fixed DC reference. The EL4093C uses a CFA in feedback with a sample & hold to provide DC restoration. Figure 1 shows how the two are connected to provide this function; the S/H compares the output of the CFA to a DC reference, and any difference between them causes an output current from the S/H. This "autozero" current is fed to the CFA inverting input, the effect of which is to move the CFA output towards the reference voltage. This autozero mechanism settles when the CFA output is one VOS away from the reference (the VOS here refers to the S/H offset voltage).

The autozero mechanism is typically active for only a short period of each video line. Figure 2 shows a NTSC video signal along with the EL4581C back porch output. The back porch signal is used to drive the HOLD input of the EL4093C, and we see that the EL4093C is in sample mode for only 3.5 µs of each line. It is during this time that the autozero mechanism attempts to drive the CFA output towards the reference voltage, at the same time putting a correction voltage onto the hold capacitor C_HOLD. During the rest of the line (60 µs) the EL4093C is in hold mode, but DC correction is maintained by the voltage on C_HOLD.

Figure 1

Figure 2
Applications Information — Contd.

Power Supply Bypassing and Printed Circuit Board Layout
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. In the EL4093C there are two sets of supply pins: V+1/V−1 provide power for the CFA, and V+2/V−2 are for the S/H amplifier. Good performance can be achieved using only one set of bypass capacitors, although they must be close to the V+1/V−1 pins since that is where the high frequency currents flow. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.01 μF capacitor has been shown to work well. Chip capacitors are recommended for the 0.01 μF bypass to minimize lead inductance.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the CFA inverting input. Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Chip resistors are recommended for RF and RG, and use of sockets should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

If the CFA is configured for non-inverting gain, then one should also pay attention to the trace leading to the + input. The inductance of a long trace (> 3”) can form a resonant network with the amplifier input, resulting in high frequency oscillations around 700 MHz. In such cases a 50Ω−100Ω series resistor placed close to the + input would isolate this inductance and damp out the resonance.

Capacitance at the Inverting Input
Any manufacturer’s high-speed voltage or current feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. Hence it is important to minimize the stray capacitance at this node by removing the nearby ground plane. In addition, since the S/H output connects to this node, it is important to minimize the trace capacitance. Good practice here would be to connect the two pins with a short trace directly underneath the chip.

Feedback Resistor Values
The EL4093C has been optimized for a gain of +2 with RF = 750Ω. This value of feedback resistor gives a 3 dB bandwidth of 300 MHz at a gain of +2 driving a 150Ω load. Since the amplifier inside the EL4093C uses current mode feedback, it is possible to change the value of RF to adjust the bandwidth. Shown in the table below are optimum feedback resistor values for different closed loop gains.

<table>
<thead>
<tr>
<th>Gain</th>
<th>Optimum RF</th>
<th>BW (MHz)</th>
<th>Peaking (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+1</td>
<td>910</td>
<td>314</td>
<td>0.2</td>
</tr>
<tr>
<td>+2</td>
<td>750</td>
<td>300</td>
<td>0</td>
</tr>
<tr>
<td>+5</td>
<td>470</td>
<td>294</td>
<td>0.2</td>
</tr>
<tr>
<td>−1</td>
<td>680</td>
<td>300</td>
<td>0</td>
</tr>
</tbody>
</table>

Autozero Interface
The autozero interface refers to the connection between the S/H output and the CFA inverting input. This interface has been greatly simplified compared to that of the EL2090C, in that the S/H output is a high impedance current source. The S/H output can be connected directly to the inverting input, and its high impedance greatly reduces the interaction between the sample & hold and the gain setting resistors. Another virtue of this interface is better gain linearity as the autozero current changes. For example, at an autozero current of 0 mA the output impedance is about 5 MΩ, dropping to 1 MΩ as the autozero current increases to 3 mA. Using RF = RG = 750Ω, the closed loop gain changes only by 0.025% in this interval.
Applications Information — Contd.

Autozero Range
The autozero range is defined as the difference between the input DC level and the reference voltage to restore to. The size of this range is a function of the gain setting resistors used and the S/H output current swing. For a gain of +2 the optimum feedback resistor is 750Ω, and the available S/H output current is ±5.5 mA minimum. To determine the autozero range for this case, we refer to Figure 3 below.

Suppose that the input DC level is +V_{DC}, and that the reference voltage is 0V. We know that in feedback, the following two conditions will exist on the CFA: first, its output will be equal to 0V (due to autozero), and second, its V_{IN}− voltage is equal to the V_{IN}+ voltage (i.e. V_{IN}− = +V_{DC}). So we have a potential difference of +V_{DC} across both RF and RG, resulting in a current I_{RF} = I_{RG} = V_{DC}/750Ω that must flow into each of them. This current I_{AZ} = (I_{RF} + I_{RG}) must come from the S/H output. Since the maximum that I_{AZ} can be is 5.5 mA, we can solve for V_{DC} using the following:

I_{AZ} = \pm 5.5 \text{ mA} = 2\left(\frac{V_{DC}}{750\Omega}\right)

and see that V_{DC} = \pm 2V. This range can easily accommodate most video signals.

As another example, consider the case where we are restoring to a reference voltage of +0.75V. Using the same reasoning as above, a current I_{RF} = (V_{DC} - 0.75V)/R_{F} and a current I_{RG} = V_{DC}/R_{G} must flow through R_{G}. Again, our boundary condition is that I_{RF} + I_{RG} \leq \pm 5.5 \text{ mA}, and we can solve for the allowable V_{DC} values using the following:

\pm 5.5 \text{ mA} = \frac{V_{DC} - 0.75V}{750\Omega} + \frac{V_{DC}}{750\Omega}

Hence V_{DC} must be between +2.4V to -1.7V. This example illustrates that when the reference changes, the autozero range also changes. In general, the user should determine the autozero range for his/her application, and ensure that the input signal is within this range during the autozero period.

Autozero Loop Bandwidth
The gain-bandwidth product (GBWP) of the autozero loop is determined by the size of the hold capacitor, the value of R_{F}, and the transconductances (gm's) of the S/H amplifier. To begin, the S/H amplifier is modeled as in Figure 4 below. First, the input stage transconductance is represented by gm1, with the compensation capacitor given by C_{HOLD}. This stage's GBWP is thus gm1/(2π \cdot C_{HOLD}) = 1/(2π \cdot (350Ω)(2.2 nF)) = 207 kHz. Next, since the S/H has a current output, its output stage can be modeled as a transconductance gm2, in this case having a value of 1/(500Ω). The current from gm2 then flows through the I to V converter made up of the CFA and R_{F} to produce a voltage gain. Thus the GBWP of the overall loop is given by:

GBWP = \frac{gm1}{2π \cdot C_{HOLD}} (gm2 \cdot R_{F})
Applications Information — Contd.

With $R_F = 750\Omega$, a GBWP of 310 kHz is obtained. Note however that this is the small signal GBWP. As mentioned earlier, the sample and hold has special boost circuits built in which provides ±8.5 mA of charge current during full slew. These boost circuits turn on when the S/H input differential voltage exceeds ±50 mV. When the boosters are turned on, $g_{m1}$ greatly increases and the circuit becomes nonlinear. Thus some stability issues are associated with the boosters, and they will be addressed in a later section.

**Charge Injection and Hold Step**

Charge injection refers to the charge transferred to the hold capacitor when switching to the HOLD mode. The charge should ideally be 0, but due to stray capacitive coupling and other effects, is typically 0.1 pC in the EL4093. This charge changes the hold capacitor voltage by $\Delta V = \Delta Q / C_{\text{HOLD}}$, and this $\Delta V$ is multiplied by the output stage transconductance ($g_{m2}$) to produce a change in S/H output current. This last quantity is listed as the spec $\Delta I_{\text{STEP}}$, and is calculated using the following:

$$\Delta I_{\text{STEP}} = \left(\frac{\Delta Q}{C_{\text{HOLD}}}\right) \cdot g_{m2}$$

For $C_{\text{HOLD}} = 2.2 \text{ nF}$ and $g_{m2} = 1/(500\Omega)$, $\Delta I_{\text{STEP}}$ has a typical value of 100 nA. This change in S/H output current flows through $R_F$, shifting the CFA output voltage. However, as we shall soon see, this shift is negligible. Assuming $R_F = 750\Omega$, $\Delta I_{\text{STEP}}$ is impressed across $R_F$ to give $(750\Omega)(100 \text{ nA}) = 0.08 \text{ mV}$ of change at the CFA output.

**Droop Rate**

When the S/H amplifier is in HOLD mode, there is a small current that leaks from the switch into the hold capacitor. This quantity is termed the droop current, and is typically 10 nA in the EL4093. This droop current produces a ramp in the hold capacitor voltage, which in turn produces a similar effect at the CFA output. The Droop Rate at the CFA output can be found using the equation below:

$$\text{Droop} = \frac{I_{\text{DROOP}}}{C_{\text{HOLD}}} (g_{m2} \cdot R_F)$$

Assuming $R_F = 750\Omega$ and $C_{\text{HOLD}} = 2.2 \text{ nF}$, the drift in the CFA output due to droop current is about 7 $\mu\text{V}/\mu\text{s}$. Recall that in NTSC applications, there is about 60 $\mu\text{s}$ between autozero periods. Thus there is $7 \mu\text{V}/\mu\text{s}(60 \mu\text{s}) = 0.4 \text{ mV}$, or less than 0.1 IRE, of drift over each NTSC scan line. This drift is negligible in most applications.
Applications Information — Contd.

Choice of Hold Capacitor
The EL4093 has been designed to work with a hold capacitor of 2.2 nF. With this value of $C_{\text{HOLD}}$, the droop rate and hold step are negligibly small for most applications. In addition, with the special boost circuits inside the S/H, fast acquisition is possible even using a hold capacitor of this size. Figure 5 below shows the input and output of the DC-restored amplifier while the S/H is in sample mode. Applying a +1V step to the non-inverting input of the CFA, the output of the CFA jumps to +2V. The S/H, however, then tries to autozero the system by driving the CFA output back to the reference voltage. Since the input differential across the S/H is initially +2V, the boost circuits turn on and supply 8.5 mA of charge current to the hold capacitor. The boost circuit remains on until the CFA output has come to within 50 mV of the reference. Note that this event took only 320 ns; settling to within 1% of the final value takes another 2 μs. Thus for a 1V input step, acquisition takes only one to two NTSC scan lines.

A natural question arises as to whether there are other $C_{\text{HOLD}}$ values that can be used. In one direction, increasing $C_{\text{HOLD}}$ will further reduce the droop and hold step, but lengthen the acquisition time. Since the droop and hold step are already small to begin with, there is no apparent advantage to increasing $C_{\text{HOLD}}$.

In the other direction, decreasing $C_{\text{HOLD}}$ would increase the droop and hold step but shorten the acquisition time. There is, however, a caveat to reducing $C_{\text{HOLD}}$: too small a $C_{\text{HOLD}}$ would cause the autozero loop to oscillate. The reason is that when the S/H boost circuit turns on, the input stage gm increases drastically and the circuit becomes nonlinear. A sufficiently large $C_{\text{HOLD}}$ must be used to suppress the non-linearity and force the loop to settle. For example, it has been found that a $C_{\text{HOLD}}$ of 470 pF results in 1 Vp-p oscillation around 10 MHz at the CFA output.

The minimum recommended value for $C_{\text{HOLD}}$ is 2.2 nF. With this value the loop remains stable over the entire operating temperature range ($-40^\circ\text{C}$ to $+85^\circ\text{C}$). The greatest instability occurs at low temperatures, where we observe from the performance curves that the S/H gm's, and hence the GBWP, are at their maximum. If the operating range is restricted to room temperature or above, then 1.5 nF is sufficient to keep the loop stable. At this value of $C_{\text{HOLD}}$ the acquisition time reduces to about 1.5 μs.

Video Performance and Application
Although the EL4093 is intended for high speed video applications such as SVGA, it also offers excellent performance for NTSC, with 0.04% dG and 0.02% dP at 3.58 MHz. Some application considerations, however, are required for handling NTSC signals.

Referring back to Figure 2, recall that typically, the autozero interval lies in the back porch portion of video containing the colorburst pulse. When the S/H compares the video to the reference voltage during this period, the colorburst (40 IREp-p) triggers the S/H boost circuit and prevents the autozero loop from settling.
Applications Information — Contd.
A remedy for this situation is to attenuate the colorburst before applying it to the S/H input. Figure 6 below shows a 3.58 MHz chroma trap which would notch out the colorburst while preserving the video DC level.

![Figure 6. Colorburst Trap for NTSC Applications](image)

One may be tempted to use a RC lowpass filter to suppress the colorburst, as shown in Figure 7 below. This technique, however, poses several problems. First, to obtain enough attenuation, we need to set the pole frequency 10 to 20 times lower than 3.58 MHz. This pole, being close to the auto zero loop pole, would destabilize the system and cause the loop to oscillate.

![Figure 7. Caution: Lowpass Filter Does Not Work in NTSC Applications](image)

Although we can cancel this pole by introducing a zero, the RC network introduces a time delay between the CFA output and the S/H input. This has undesirable effects in some NTSC applications, as Figure 8 below illustrates. There is only 0.6 μs from the rising edge of sync to the colorburst. If we are autozeroing over the back porch, the autozero period would begin somewhere in this 0.6 μs interval. Since the edge of sync is now delayed by the RC network, autozero begins before the video back porch reaches its final value. Consequently, the autozero loop performs a correction on every line and never settles.

![Figure 8. Lowpass Filter Delays Input to Sample and Hold](image)
Applications Information — Contd.

If the video does not contain any AC components during the autozero level (e.g. RGB video), then the above networks are not needed and the CFA output can be connected directly to the S/H input.

Power Dissipation

The EL4093 current feedback amplifier has an absolute maximum of ±30 mA output current drive. This is slightly more than the current required to drive ±2V into 75Ω. To see how much the junction temperature is raised in this worst case, we refer to the equations below:

\[ T_{J\text{MAX}} = T_{\text{MAX}} + (\theta_{JA} \cdot P_{D\text{MAX}}) \]

where:
- \( T_{\text{MAX}} \) = Maximum Ambient Temperature
- \( \theta_{JA} \) = Thermal Resistance of the Package
- \( P_{D\text{MAX}} \) = Maximum Power Dissipation of the CFA and S/H amplifier in the Package

\( P_{D\text{MAX}} \) for either the CFA or the S/H amplifier can be calculated as follows:

\[ P_{D\text{MAX}} = (2 \cdot V_S \cdot I_{S\text{MAX}}) \]

\[ + (V_S - V_{OUT\text{MAX}}) \cdot (V_{OUT\text{MAX}}/R_L) \]

where:
- \( V_S \) = Supply Voltage
- \( I_{S\text{MAX}} \) = Maximum Supply Current of Amplifier
- \( V_{OUT\text{MAX}} \) = Maximum Output Voltage of Application
- \( R_L \) = Load Resistance

For the EL4093, the maximum supply current is 11.5 mA on \( V_S = \pm 5V \). Assume that in the worst case, the CFA output swings ±2V into 75Ω. Since the S/H has a current output, we assume that it is at maximum current swing (±5.5 mA) but at a mid-rail output voltage (0V). With the above assumptions, \( P_{D\text{MAX}} \) for the EL4093 is 223 mW, and using the thermal resistance of a narrow SO package (120°C/W), this yields a temperature increase of 27°C. Since the maximum ambient temperature is 85°C, the resulting junction temperature of 112°C is still below the maximum.

Please note that there is no short-circuit protection on the EL4093 CFA output, and hence the minimum short circuit current (60 mA) is greater than the absolute maximum output current. Maintaining the EL4093 in this state for more than a few seconds may cause the part to exceed \( T_{J\text{MAX}} \), in addition to metal migration problems.
**Features**
- Complete video fader
- 0.02%/0.04° differential gain/phase @100% gain
- Output amplifier included
- Calibrated linear gain control
- ±5V to ±15V operation
- 60 MHz bandwidth
- Low thermal errors

**Applications**
- Video faders/wipers
- Gain control
- Video text insertion
- Level adjust
- Modulation

**Ordering information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4094CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL4094CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

**General Description**

The EL4094C is a complete two-input fader. It combines two inputs according to the equation:

\[ V_{OUT} = V_{INA} (0.5V + V_{g}) + V_{INB} (0.5V - V_{g}), \]

where \( V_{GAIN} \) is the difference between \( V_{GAIN} \) and \( V_{GAIN} \) pin voltages and ranges from \(-0.5V\) to \(+0.5V\). It has a wide 60 MHz bandwidth at \(-3\) dB, and is designed for excellent video distortion performance. The EL4094C is the same circuit as the EL4095, but with feedback resistors included on-chip to implement unity-gain connection. An output buffer is included in both circuits.

The gain-control input is also very fast, with a 20 MHz small-signal bandwidth and 70 ns recovery time from overdrive.

The EL4094C is compatible with power supplies from \(±5V\) to \(±15V\), and is available in both the 8-pin plastic DIP and SO-8.

**Connection Diagram**

![Connection Diagram](image-url)

Manufactured under U.S. Patent No. 5,321,371, 5,374,898
Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{S+})</td>
<td>Voltage between (V_{S+}) and GND</td>
<td>+18V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_S)</td>
<td>Voltage between (V_{S+}) and (V_{S-})</td>
<td>+33V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IN+})</td>
<td>Input Voltage</td>
<td>((V_{S-}) - 0.3V) to ((V_{S+}) + 0.3V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{INB})</td>
<td>Input Voltage</td>
<td>(V_{GAIN} \pm 5V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{GAIN})</td>
<td>Input Voltage</td>
<td>(V_{S-} \text{ to } V_{S+})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{OUT})</td>
<td>Output Current</td>
<td>±35 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{PSR})</td>
<td>Power Supply Rejection Ratio</td>
<td>60</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(EG)</td>
<td>Gain Error, 100% Setting</td>
<td>-0.5</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>(V_{IN}) Range</td>
<td>((V-) + 2.5)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_O)</td>
<td>Output Voltage Swing</td>
<td>((V-) + 2.5)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{SC})</td>
<td>Output Short-Circuit Current</td>
<td>50 95 150</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(V_{GAIN, 100%})</td>
<td>Minimum Voltage at (V_{GAIN}) for 100% Gain</td>
<td>0.45 0.5 0.55</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{GAIN, 0%})</td>
<td>Maximum Voltage at (V_{GAIN}) for 0% Gain</td>
<td>-0.55 -0.5 -0.45</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(NL, \text{Gain})</td>
<td>Gain Control Non-linearity, (V_{IN} = \pm 0.5V)</td>
<td>1.5 4</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>(NL, \text{Av} = 1)</td>
<td>Signal Non-linearity, (V_{IN} = 0 \pm 1V), (V_{GAIN} = 0.55V)</td>
<td>0.01</td>
<td></td>
<td>V %</td>
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<tr>
<td>(Av = 0.5)</td>
<td>Signal Non-linearity, (V_{IN} = 0 \pm 1V), (V_{GAIN} = 0V)</td>
<td>0.05</td>
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<td>V %</td>
</tr>
<tr>
<td>(Av = 0.25)</td>
<td>Signal Non-linearity, (V_{IN} = 0 \pm 1V), (V_{GAIN} = -0.25V)</td>
<td>0.2 0.5</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>(R_{Gain})</td>
<td>Resistance between (V_{GAIN}) and (\overline{V_{GAIN}})</td>
<td>4.6 5.5 6.6</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>(I_{S})</td>
<td>Supply Current</td>
<td>12 14.5 17</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(F_T)</td>
<td>Off-Channel Feedthrough</td>
<td>-75 -50</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Open Loop DC Electrical Characteristics
\(V_S = \pm 5V, T_A = 25°C, V_{GAIN} = +0.6V\) to measure channel A, \(V_{GAIN} = -0.6V\) to measure channel B, \(V_{GAIN} = 0V\), unless otherwise specified.
### Closed Loop AC Electrical Characteristics

$V_S = \pm 15V, C_L = 15\ \text{pF}, T_A = 25^\circ C, A_V = 100\%$ unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate; $V_{OUT}$ from $-3V$ to $+3V$ measured at $-2V$ and $+2V$</td>
<td>370</td>
<td>500</td>
<td>III</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth, $-3\ dB$</td>
<td>45</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$-1\ dB$</td>
<td>35</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>$-0.1\ dB$</td>
<td>6</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>$dG$</td>
<td>Differential Gain, AC amplitude of 286 mV&lt;sub&gt;p-p&lt;/sub&gt; at 3.58 MHz on DC offset of $-0.7$, $0$, and $+0.7V$ $A_V = 100%$</td>
<td>0.02</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>$A_V = 50%$</td>
<td>0.20</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>$A_V = 25%$</td>
<td>0.40</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>$d\theta$</td>
<td>Differential Phase, AC amplitude of 286 mV&lt;sub&gt;p-p&lt;/sub&gt; at 3.58 MHz on DC offset of $-0.7$, $0$, and $+0.7V$ $A_V = 100%$</td>
<td>0.04</td>
<td>V</td>
<td>($)</td>
</tr>
<tr>
<td></td>
<td>$A_V = 50%$</td>
<td>0.20</td>
<td>V</td>
<td>($)</td>
</tr>
<tr>
<td></td>
<td>$A_V = 25%$</td>
<td>0.20</td>
<td>V</td>
<td>($)</td>
</tr>
<tr>
<td>BW, GAIN</td>
<td>$-3\ dB$ Gain Control Bandwidth, $V_{GAIN}$ Amplitude 0.5 V&lt;sub&gt;p-p&lt;/sub&gt;</td>
<td>20</td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>$T_{REC}, GAIN$</td>
<td>Gain Control Recovery from Overload; $V_{GAIN}$ from $-0.6V$ to $0V$</td>
<td>70</td>
<td>V</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Typical Performance Curves

**Small-Signal Step Response for Gain = 100\%, 50\%, 25\%, and 0\%. $V_S \pm 5V$**

![Small-Signal Step Response](image1)

**Large-Signal Step Response for Gain = 100\%, 50\%, 25\%, and 0\%. $V_S \pm 12V$**

![Large-Signal Step Response](image2)
Typical Performance Curves — Contd.

**Frequency Response vs Capacitive Loading**

![Graph showing frequency response vs capacitive loading](image)

**Frequency Response vs Resistive Loading**

![Graph showing frequency response vs resistive loading](image)

**Frequency Response vs Gain**

![Graph showing frequency response vs gain](image)

**Off-Channel Isolation Over Frequency**

![Graph showing off-channel isolation over frequency](image)

**Change in Slewrate and Bandwidth with Supply Voltage**

![Graph showing change in slewrate and bandwidth with supply voltage](image)

**Output Noise Over Frequency**

![Graph showing output noise over frequency](image)
Typical Performance Curves — Contd.

Change in 100% Gain Error, Supply Current, Slewrate and Bandwidth over Temperature

Nonlinearity vs V_{IN} for Gain = 100%, 75%, 50% and 25%

Differential Gain Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz

Differential Phase Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz
Typical Performance Curves — Contd.

Differential Gain and Phase Error vs Gain

Gain vs $V_G$, $1V_{DC}$ at $V_{INA}$

Gain Control Response to a Non-Overloading Step, Constant Sinewave at $V_{INA}$

Cross-Fade Balance. $V_{INA} = V_{INB} = 0V$

$V_{GAIN}$ Overload Recovery Response
Typical Performance Curves — Contd.

- **Gain Control Gain vs Frequency**

- **Change in V(100%) and V(0%) of Gain Control vs Supply Voltage**

- **Change in V(100%) and V(0%) of Gain Control vs Die Temperature**

- **Supply Current vs Supply Voltage**

- **Maximum Dissipation vs Ambient Temperature**

---

*Gain Control Gain vs Frequency:*

- Frequency (Hz) vs Gain (dB)
- Frequency: 100K, 1M, 10M, 100M
- Gain: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10
- \( V_{\text{IN}} = 1V \)

*Change in V(100%) and V(0%) of Gain Control vs Supply Voltage:*

- Supply Voltage (V) vs Change in V(100%) and V(0%) (mV)
- Supply Voltage: 3, 5, 7, 9, 11, 13, 15
- Change in V(100%): 30, 20, 10, 0, -10, -20, -30
- Change in V(0%): 10, 0, -10, -20, -30

*Change in V(100%) and V(0%) of Gain Control vs Die Temperature:*

- Die Temperature (°C) vs Change in V(100%) and V(0%) (mV)
- Die Temperature: -40, -20, 0, 20, 40, 60, 80, 100, 120, 140, 160
- Change in V(100%): 10, 8, 6, 4, 2, 0
- Change in V(0%): 2, 0, -2

*Supply Current vs Supply Voltage:*

- Supply Voltage (V) vs Supply Current (mA)
- Supply Voltage: 0, 3, 6, 9, 12, 15
- Supply Current: 0, 2, 4, 6, 8, 10, 12, 14, 16, 18

*Maximum Dissipation vs Ambient Temperature:*

- Ambient Temperature (°C) vs Maximum Dissipation (W)
- Ambient Temperature: -40, -20, 0, 20, 40, 60, 80, 100
- Maximum Dissipation: 0.8, 0.6, 0.4, 0.2, 0, -0.2, -0.4, -0.6, -0.8, -1.0
Applications Information

The EL4094 is a self-contained and calibrated fader subsystem. When a given channel has 100% gain the circuit behaves as a current-feedback amplifier in unity-gain connection. As such, video and transfer distortions are very low. As the gain of the input is reduced, a 2-quadrant multiplier is gradually introduced into the signal path and distortions increase with reducing gain.

The input impedance also changes with gain setting, from about 1 MΩ at 100% gain down to 16 kΩ at zero gain. To maximize gain accuracy and linearity, the inputs should be driven from source impedances of 500Ω or less.

Linearity
The EL4094 is designed to work linearly with ±2V inputs, but lowest distortion occurs at ±1V levels and below. Errors are closer to those of a good current-feedback amplifier above 90% gain.

Low-frequency linearity is 0.1% or better for gains 25% to 100% and inputs up to 1V. NTSC differential gain and phase errors are better than 0.3% and 0.3° for the 25% to 100% gain range. These distortions are not strongly affected by supply voltage nor output loading, at least down to 150Ω. For settling to 0.1%, however, it is best to not load the output heavily and to run the EL4094 on the lowest practical supply voltages, so that thermal effects are minimized.

Gain Control Inputs
The gain control inputs are differential and may be biased at any voltage as long as \( V_{GAIN} \) is less than 2.5V below \( V^+ \) and 3V above \( V^- \). The differential input impedance is 5.5 kΩ, and the common-mode impedance is more than 500 kΩ. With zero differential voltage on the gain inputs, both signal inputs have a 50% gain factor. Nominal calibration sets the 100% gain of \( V_{INA} \) input at +0.5V of gain control voltage, and 0% at −0.5V of gain control. \( V_{INH} \)'s gain is complementary to that of \( V_{INA} \); +0.5V of gain control sets 0% gain at \( V_{INH} \) and −0.5V gain control sets 100% \( V_{INB} \) gain. The gain control does not have a completely abrupt transition at the 0% and 100% points. There is about 10 mV of “soft” transfer at the gain endpoints. To obtain the most accurate 100% gain factor or best attenuation at 0% gain, it is necessary to overdrive the gain control input by 30 mV or more. This would set the gain control voltage range as −0.565V to +0.565V, or 30 mV beyond the maximum guaranteed 0% to 100% range. In fact, the gain control inputs are very complex. Here is a representation of the terminals:

For gain control inputs between ±0.5V (±90 μA), the diode bridge is a low impedance and all of the current into \( V_g \) flows back out through \( V_g \). When gain control inputs exceed this amount, the bridge becomes a high impedance as some of the diodes shut off, and the \( V_g \) impedance rises sharply from the nominal 5.5kΩ to about 500kΩ. This is the condition of gain control overdrive. The actual circuit produces a much sharper overdrive characteristic than does the simple diode bridge of this representation.

The gain input has a 20 MHz −3 dB bandwidth and 17 ns risetime for inputs to ±0.45V. When the gain control voltage exceeds the 0% or 100% values, a 70 ns overdrive recovery transient will occur when it is brought back to linear range. If quicker gain overdrive response is required, the Force control inputs of the EL4095 can be used.

Output Loading
The EL4094 does not work well with heavy capacitive loads. Like all amplifier outputs, the output impedance becomes inductive over frequency resonating with a capacitive load. The effective output inductance of the EL4094 is about 350 nH. More than 50 pF will cause excessive frequency response peaking and transient ringing. The problem can be solved by inserting a low-value resistor in series with the load, 22Ω or more. If a series resistance cannot be used, then adding a 300Ω or less load resistor to ground or a “snubber” network may help. A snubber is a re-
Applications Information — Contd.

istor in series with a capacitor, 150Ω and 100 pF being typical values. The advantage of a snubber is that it does not draw DC load current.

Unterminated coaxial line loads can also cause resonances, and they should be terminated either at the far end or a series back-match resistor installed between the EL4094 and the cable.

The output stage can deliver up to 140 mA into a short-circuit load, but it is only rated for a continuous 35 mA. More continuous current can cause reliability problems with the on-chip metal interconnect. Video levels and loads cause no problems at all.

Noise

The EL4094 has a very simple noise characteristic: the output noise is constant (40 nV/√Hz wideband) for all gain settings. The input-referred noise is then the output noise divided by the gain. For instance, at a gain of 50% the input noise is 40 nV/√Hz/0.5, or 80 nV/√Hz.

Bypassing

The EL4094 is fairly tolerant of power-supply bypassing, but best multiplier performance is obtained with closely connected 0.1 μF ceramic capacitors. The leaded chip capacitors are good, but neither additional tantalums nor chip components are necessary. The signal inputs can oscillate locally when connected to long lines or unterminated cables.

Power Dissipation

Peak die temperature must not exceed 150°C. At this temperature, the epoxy begins to soften and becomes unstable, chemically and mechanically. This allows 75°C internal temperature rise for a 75°C ambient. The EL4094 in the 8-pin PDIP package has a thermal resistance of 87°C/W, and can thus dissipate 862 mW at a 75°C ambient temperature. The device draws 17 mA maximum supply current, only 510 mW at ±15V supplies, and the circuit has no dissipation problems in this package.

The SO-8 surface-mount package has a 153°C/W thermal resistance with the EL4094, and only 490 mW can be dissipated at 75°C ambient temp-erature. The EL4094 thus cannot be operated with ±15V supplies at 75°C in the surface-mount package; the supplies should be reduced to ±5V to ±12V levels, especially if extra dissipation occurs when driving a load.

The EL4094 as a Level Adjust

A common use for gain controls is as an input signal leveller—a circuit that scales too-large or too-small signals to a standard amplitude. A typical situation would be to scale a variable video input by +6 dB to -6 dB to obtain a standard amplitude. The EL4094 cannot provide more than 0 dB gain, but it can span the range of 0 dB to -12 dB with another amplifier gaining the output up by 6 dB. The simplest way to obtain the range is to simply ground the B input and vary the gain of the signal applied to the A input. The disadvantage of this approach is that linearity degrades at low gains. By connecting the signal to the A input of the EL4094 and the signal attenuated by 12 dB to the B input, the gain control offers the highest linearity possible at 0 dB and -12 dB extremes, and good performance between. The circuit is shown on the following page.

The EL4095 can be used to provide the required gains without the extra amplifier. In practice, the gain control is adjusted to set a standard video level regardless of the input level. The EL4583 sync-separator has a recovered amplitude output that can be used to servo the gain control voltage. Here is the curve of differential gain and phase distortion for varying inputs, with the output set to standard video level:

![Differential Gain and Phase of Linearized Level Control](image-url)
**Applications Information — Contd.**
The differential gain error is kept to 0.3% and the differential phase to 0.15° or better over the entire input range.

The EL4094 as an Adjustable Filter
Equalizers are used to adjust the delay or frequency response of systems. A typical use is to compensate for the high-frequency loss of a cable system ahead of the cable so as to create a flat response at the far end. A generalized scheme with the EL4094 is shown below.

For an adjustable preemphasis filter, for instance, filter A might be an all-pass filter to compensate for the delay of filter B, a peaking filter. Fading the gain from A to B provides a variable amount of peaking, but constant delay.

The EL4094 as a Phase Modulator
To make a phase modulator, filter A might be a leading-phase network, and filter B a lagging network. The wide bandwidth of the gain-control input allows wideband phase modulation of the carrier applied to the main input. Of course, the carrier and gain inputs must not be digital but be reasonably clean sinewaves for the modulation to be accurate.
EL4094C Macromodel

This macromodel is offered to allow simulation of general EL4094 behavior. We have included these characteristics:

- Small-signal frequency response
- Output loading effects
- Input impedance
- Off-channel feedthrough
- Output impedance over frequency
- Signal path DC distortions
- \( \text{V}_G \) gain I-V characteristics
- \( \text{V}_G \) gain overdrive recovery delay
- 100% gain error

These will give a good range of results for various operating conditions, but the macromodel does not behave identically as the circuit in these areas:

- Temperature effects
- Signal overload effects
- Signal and \( \text{V}_G \) operating range
- Current-limit
- Video and high-frequency distortions
- Slewrate limitations
- Noise
- Power supply interactions

The macromodel's netlist is based on the Pspice simulator (copyrighted by the Microsim Company). Other simulators may not support the POLY function, which is used to implement multiplication as well as square-low nonlinearities.

```
.**
.**
*    V_INB    V_OUT  /V_G  V_G  V_INA
*    (1)     (4)     (6)     (7)     (8)
.**
```

```
R_{OL} 810 0 290k
C_{comp} 810 0 3.5p
G_{1} 10 0 810 0 -10
R_{OUT} 10 0 0.1
L_{OUT} 10 4 350.200n
R_{OUT} 10 4 80
r_{1} 10 910 10
c_{1} 910 911 300p
r_{2} 911 0 90
***
*** Input channel A
***
R_{INA} 22 910 16k
r_{a} 11 0 1k
C_{feedthrougha} 23 8 130p
R_{feedthrougha} 8 22 1.0
E_{la} 23 22 1 0.1
R_{spice} 23 22 1E12
G_{1a} 11 0 POLY(1) (22,910) 0.0 0.001 -3E-6
G_{2a} 810 0 POLY(2) (11,0) (13,0) 0.0 0.0 0.0 0.0 0.001
***
*** Input channel B
***
R_{INB} 25 910 16k
r_{b} 20 0 1k
C_{feedthroughb} 24 1 130p
R_{feedthroughb} 1 25 1.0
E_{lb} 24 25 8 0.1
R_{spice} 24 25 1E12
G_{1b} 20 0 POLY(1) (25,910) 0.0 0.001 -3E-6
G_{2b} 810 0 POLY(2) (20,0) (19,0) 0.0 0.0 0.0 0.0 0.001
***
*** Gain control
***
R_{spice} 13 0 1E12
R_{spice} 18 0 1E12
R_{10} 14 0 1E7
C_{10} 14 0 8E-16
D_{1} 14 15 Dclamp
D_{2} 16 14 Dclamp
.model Dclamp D (TT = 200n)
V_{1} 15 0 4999.3
V_{2} 0 16 4999.3
V_{3} 13 17 0.5
V_{4} 19 18 0.5
G_{10} 14 0 7 6 -0.001
G_{11} 7 6 14 0 -2E-8
E_{10} 17 0 14 0 1E-4
E_{11} 18 0 14 0 -1E-4
***
.ends
**
```
EL4094C Macromodel — Contd.

EL4094 Macromodel Schematic
### Features
- Full function video fader
- 0.02% / 0.02° differential gain/phase @ 100% gain
- 25 ns multiplexer included
- Output amplifier included
- Calibrated linear gain control
- ±5V to ±15V operation
- 60 MHz bandwidth
- Low thermal errors

### Applications
- Video faders/wipers
- Gain control
- Graphics overlay
- Video text insertion
- Level adjust
- Modulation

### General Description
The EL4095C is a versatile variable-gain building block. At its core is a fader which can variably blend two inputs together and an output amplifier that can drive heavy loads. Each input appears as the input of a current-feedback amplifier and with external resistors can separately provide any gain desired. The output is defined as:

\[
V_{OUT} = A \cdot V_{INA} (0.5V + V_{GAIN}) + B \cdot V_{INB} (0.5V - V_{GAIN}),
\]

where A and B are the feedback gains of each channel.

Additionally, two logic inputs are provided which each override the analog \(V_{GAIN}\) control and force 100% gain for one input and 0% for the other. The logic inputs switch in only 25 ns and provide high attenuation to the off channel, while generating very small glitches.

Signal bandwidth is 60 MHz, and gain-control bandwidth 20 MHz. The gain control recovers from overdrive in only 70 ns.

The EL4095C operates from ±5V to ±15V power supplies, and is available in both 14-pin DIP and narrow surface mount packages.

### Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4095CN</td>
<td>-40°C to +85°C</td>
<td>14 Pin DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL4095CS</td>
<td>-40°C to +85°C</td>
<td>SO-14</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

### Connection Diagram

[Connection Diagram Image]

**Top View**

Manufactured under U.S. Patent No. 5,321,371, 5,374,898
# Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter (V_S^+)</th>
<th>Description</th>
<th>Limit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V_S^+)</td>
<td>Voltage between (V_S^+) and (V_S^-)</td>
<td>Min</td>
<td>18V</td>
</tr>
<tr>
<td>Voltage (V_S)</td>
<td>((V_S^-) - 0.3V) to ((V_S^+) + 0.3V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (V_{INA})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (V_{INB})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Into (-VINA), (-VINB)</td>
<td></td>
<td>5 mA</td>
<td></td>
</tr>
<tr>
<td>Input Voltage (V_{GAIN})</td>
<td></td>
<td>(V_{GAIN} \pm 5V)</td>
<td></td>
</tr>
<tr>
<td>Input Voltage (V_{GAIN})</td>
<td></td>
<td>(V_S^-) to (V_S^+)</td>
<td></td>
</tr>
<tr>
<td>Input Voltage (V_{FORCE})</td>
<td>Input Voltage</td>
<td>Min</td>
<td>1V to +6V</td>
</tr>
<tr>
<td>Output Current (I_{OUT})</td>
<td></td>
<td></td>
<td>±35 mA</td>
</tr>
<tr>
<td>Operating Temperature Range (T_A)</td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Operating Junction Temperature (T_J)</td>
<td></td>
<td></td>
<td>0°C to +150°C</td>
</tr>
<tr>
<td>Storage Temperature Range (T_{ST})</td>
<td></td>
<td></td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LITX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

## Test Level

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25^\circ C) and QA sample tested at (T_A = 25^\circ C), (T_{MAX}) and (T_{MIN}) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25^\circ C) for information purposes only.</td>
</tr>
</tbody>
</table>

## Open Loop DC Electrical Characteristics

\(V_S = \pm 15V, T_A = 25^\circ C, V_{GAIN} \) ground unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>Min</td>
<td>1.5</td>
<td>I</td>
</tr>
<tr>
<td>(I_{B^+})</td>
<td>Input Bias Current (+V_{IN})</td>
<td>Typ</td>
<td>5</td>
<td>mV</td>
</tr>
<tr>
<td>(I_{B^-})</td>
<td>Input Bias Current (-V_{IN})</td>
<td>Max</td>
<td>10</td>
<td>mV</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection</td>
<td>Min</td>
<td>65</td>
<td>dB</td>
</tr>
<tr>
<td>(-CMRR)</td>
<td>Common Mode Rejection</td>
<td>Typ</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (-V_{IN})</td>
<td>Min</td>
<td>65</td>
<td>dB</td>
</tr>
<tr>
<td>(-IPSRR)</td>
<td>Power Supply Rejection Ratio (-V_{IN})</td>
<td>Typ</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Transimpedance (-V_{IN})</td>
<td>Min</td>
<td>0.2</td>
<td>(\mu A/V)</td>
</tr>
<tr>
<td>(R_{IN^-})</td>
<td>Input Resistance (-V_{IN})</td>
<td>Typ</td>
<td>0.4</td>
<td>(\mu A/V)</td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Input Range (+V_{IN})</td>
<td>Max</td>
<td>80</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(V_O)</td>
<td>Output Voltage Swing ((-V_{IN}) + 3.5)</td>
<td>Min</td>
<td>(V_{IN})</td>
<td></td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input High Threshold at (-V_{IN})</td>
<td>Typ</td>
<td>(V_{IH})</td>
<td></td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input Low Threshold at (-V_{IN})</td>
<td>Max</td>
<td>(V_{IL})</td>
<td></td>
</tr>
<tr>
<td>(I_{SC})</td>
<td>Output Short-Circuit Current (-V_{IN})</td>
<td>Min</td>
<td>80</td>
<td>(V)</td>
</tr>
<tr>
<td>(I_{OH})</td>
<td>Input Current of Force A or Force B, (V_{FORCE} = 5V)</td>
<td>Typ</td>
<td>(I_{OH})</td>
<td></td>
</tr>
<tr>
<td>(I_{OL})</td>
<td>Current of Force A or Force B, (V_{FORCE} = 0V)</td>
<td>Max</td>
<td>(I_{OL})</td>
<td></td>
</tr>
</tbody>
</table>
### Open Loop DC Electrical Characteristics — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>Feedthrough, Forced</td>
<td>Feedthrough of Deselected Input to Output, Deselected Input at 100% Gain Control</td>
<td>60</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;GAIN&lt;/sub&gt;, 100%</td>
<td>Minimum Voltage at V&lt;sub&gt;GAIN&lt;/sub&gt; for 100% Gain</td>
<td>0.45</td>
<td>0.5</td>
<td>0.55</td>
</tr>
<tr>
<td>V&lt;sub&gt;GAIN&lt;/sub&gt;, 0%</td>
<td>Maximum Voltage at V&lt;sub&gt;GAIN&lt;/sub&gt; for 0% Gain</td>
<td>-0.55</td>
<td>-0.5</td>
<td>-0.45</td>
</tr>
<tr>
<td>NL, Gain</td>
<td>Gain Control Non-linearity, V&lt;sub&gt;IN&lt;/sub&gt; = ±0.5V</td>
<td>2</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;IN, VG&lt;/sub&gt;</td>
<td>Impedance between V&lt;sub&gt;GAIN&lt;/sub&gt; and V&lt;sub&gt;GAIN&lt;/sub&gt;</td>
<td>4.5</td>
<td>5.5</td>
<td>6.5</td>
</tr>
<tr>
<td>RL, AV = 1</td>
<td>Signal Non-linearity, V&lt;sub&gt;IN&lt;/sub&gt; = ±1V, V&lt;sub&gt;GAIN&lt;/sub&gt; = 0.55V</td>
<td>&lt;0.01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RL, AV = 0.5</td>
<td>Signal Non-linearity, V&lt;sub&gt;IN&lt;/sub&gt; = ±1V, V&lt;sub&gt;GAIN&lt;/sub&gt; = 0V</td>
<td>0.03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RL, AV = 0.25</td>
<td>Signal Non-linearity, V&lt;sub&gt;IN&lt;/sub&gt; = ±1V, V&lt;sub&gt;GAIN&lt;/sub&gt; = −0.25V</td>
<td>0.07</td>
<td>0.4</td>
<td></td>
</tr>
</tbody>
</table>

### Closed Loop AC Electrical Characteristics

V<sub>S</sub> = ±15V, A<sub>V</sub> = +1, R<sub>F</sub> = R<sub>IN</sub> = 1 kΩ, R<sub>L</sub> = 5000Ω, C<sub>L</sub> = 15 pF, C<sub>IN-</sub> = 2 pF, T<sub>A</sub> = 25°C, A<sub>V</sub> = 100% unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate; V&lt;sub&gt;OUT&lt;/sub&gt; from −3V to +3V</td>
<td>330</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>30</td>
<td>60</td>
<td>-1 dB</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain; AC Amplitude of 286 mV&lt;sub&gt;p-p&lt;/sub&gt;</td>
<td>0.02</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>at 3.58 MHz on DC Offset of −0.7V, 0V and +0.7V</td>
<td>0.07</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 100%</td>
<td>0.07</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 50%</td>
<td>0.07</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 25%</td>
<td>0.07</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dθ</td>
<td>Differential Phase; AC Amplitude of 286 mV&lt;sub&gt;p-p&lt;/sub&gt;</td>
<td>0.02</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>at 3.58 MHz on DC Offset of −0.7V, 0V and +0.7V</td>
<td>0.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 100%</td>
<td>0.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 50%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 25%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;S&lt;/sub&gt;</td>
<td>Settling Time to 0.2%; V&lt;sub&gt;OUT&lt;/sub&gt; from −2V to +2V</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 100%</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A&lt;sub&gt;V&lt;/sub&gt; = 25%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;FORCE&lt;/sub&gt;</td>
<td>Propagation Delay from V&lt;sub&gt;FORCE&lt;/sub&gt; = 1.4V to 50%</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW, Gain</td>
<td>−3 dB Gain Control Bandwidth, V&lt;sub&gt;GAIN&lt;/sub&gt; Amplitude 0.5 V&lt;sub&gt;p-p&lt;/sub&gt;</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;REC&lt;/sub&gt;, Gain</td>
<td>Gain Control Recovery from Overload; V&lt;sub&gt;GAIN&lt;/sub&gt; from −0.7V to 0V</td>
<td>70</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Typical Performance Curves

Large-Signal Pulse Response Gain = +1

![Large-Signal Pulse Response Gain = +1](image)

Large-Signal Pulse Response Gain = -1

![Large-Signal Pulse Response Gain = -1](image)

Small-Signal Pulse Response for Various Gains

![Small-Signal Pulse Response for Various Gains](image)

Frequency Response for Different Gains AV = +1

![Frequency Response for Different Gains AV = +1](image)

Frequency Response with Different Values of RF - Gain = +1

![Frequency Response with Different Values of RF - Gain = +1](image)

Frequency Response with Different Values of RF - Gain = -1

![Frequency Response with Different Values of RF - Gain = -1](image)
Typical Performance Curves — Contd.

**Frequency Response with Different Gains**

![Graph showing frequency response with different gains](image1)

**Frequency Response with Various Load Capacitances and Resistances**

![Graph showing frequency response with various load capacitances and resistances](image2)

**Frequency Response with Various Values of Parasitic $C_{IN}$**

![Graph showing frequency response with various values of parasitic $C_{IN}$](image3)

**Input Noise Voltage and Current vs Frequency**

![Graph showing input noise voltage and current vs frequency](image4)

**Change in Bandwidth and Slewrate with Supply Voltage — Gain = +1**

![Graph showing change in bandwidth and slewrate with supply voltage — gain = +1](image5)

**Change in Bandwidth and Slewrate with Supply Voltage — Gain = -1**

![Graph showing change in bandwidth and slewrate with supply voltage — gain = -1](image6)
Typical Performance Curves — Contd.

Change in Bandwidth and Slewrate with Temperature - Gain = +1

Change in Bandwidth and Slewrate with Temperature - Gain = -1

DC Nonlinearity vs Input Voltage - Gain = +1

Change in Vos and Ib- vs die Temperature

Differential Gain and Phase Errors vs Gain Control Setting - Gain = +1

Differential Gain and Phase Errors vs Gain Control Setting - Gain = -1
Typical Performance Curves — Contd.

**Differential Phase Error vs DC Offset — Gain = +1**

- \( V_{S} = \pm 15V \)
- \( A_{V} = 25\% \)
- \( A_{V} = 50\% \) AND 75\%
- \( A_{V} = 100\% \)

**Differential Phase Error vs DC Offset — Gain = -1**

- \( V_{S} = \pm 15V \)
- \( A_{V} = 25\% \)
- \( A_{V} = 50\% \) OR 75\%
- \( A_{V} = 100\% \)

**Attenuation over Frequency — Gain = +1**

- \( V_{G} = +0.6V \)
- \( V_{G} = -0.6V \)

**Attenuation over Frequency — Gain = -1**

- \( V_{G} = +0.6V \)
- \( V_{G} = -0.6V \)
Typical Performance Curves — Contd.

**Gain vs $V_G$ ($1 \, V_{DC}$ at $V_{INA}$)**

Gain Control Response to a Non-Overloading Step, Constant Sinewave at $V_{INA}$

**$V_{GAIN}$ Overload Recovery Response—No AC Input**

Cross-Fade Balance $-0V$ on $A_{IN}$ and $B_{IN}$; Gain $= +1$
Typical Performance Curves — Contd.

- **Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Supply Voltage**
- **Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs $V_{\text{GAIN Offset}}$**
- **Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Die Temperature**

---

**Force Response**

- **Force**
- **$V_{\text{OUT}}$**

---

**Force-Induced Output Transient**

- **Force**
- **$V_{\text{OUT}}$**

---

**Supply Current vs Supply Voltage**

- **Power Dissipation vs Ambient Temperature**

---

**Package Power Dissipation vs Ambient Temperature**

- **PLASTIC DIP PACKAGE**
- **SURFACE MOUNT PACKAGE**
Test Circuit, $A_V = +1$

\[
\text{OUTPUT} = A_{IN} (0.5 + V_{GAIN}) + B_{IN} (0.5 - V_{GAIN}) \\
\text{FOR} \ -0.5V \leq V_{GAIN} \leq +0.5V
\]
Applications Information
The EL4095 is a general-purpose two-channel fader whose input channels each act as a current-feedback amplifier (CFA) input. Each input can have its own gain factor as established by external resistors. For instance, the Test Circuit shows two channels each arranged as +1 gain, with the traditional single feedback resistor $R_F$ connected from $V_{OUT}$ to the $-V_{IN}$ of each channel.

The EL4095 can be connected as an inverting amplifier in the same manner as any CFA:

![EL4095C In Inverting Connection Diagram]

Frequency Response
Like other CFA's, there is a recommended feedback resistor, which for this circuit is 1 KΩ. The value of $R_F$ sets the closed-loop $-3$ dB bandwidth, and has only a small range of practical variation. The user should consult the typical performance curves to find the optional value of $R_F$ for a given circuit gain. In general, the bandwidth will decrease slightly as closed-loop gain is increased; $R_F$ can be reduced to make up for bandwidth loss. Too small a value of $R_F$ will cause frequency response peaking and ringing during transients. On the other hand, increasing $R_F$ will reduce bandwidth but improve stability.

\[
\text{OUTPUT} = -A_{IN} \left( \frac{R_F}{R_{NA}} \right) \left( 0.5 + V_{GAIN} \right)
\]

\[
- R_{IN} \left( \frac{R_F}{R_{NB}} \right) \left( 0.5 - V_{GAIN} \right)
\]

FOR $-0.5V \leq V_{GAIN} \leq +0.5V$
Applications Information — Contd.
Stray capacitance at each \(-\text{VIN}\) terminal should absolutely be minimized, especially in a positive-gain mode, or peaking will occur. Similarly, the load capacitance should be minimized. If more than 25 pF of load capacitance must be driven, a load resistor from 100\(\Omega\) to 400\(\Omega\) can be added in parallel with the output to reduce peaking, but some bandwidth degradation may occur. A “snubber” load can alternatively be used. This is a resistor in series with a capacitor to ground, 150\(\mu\)F and 100\(\mu\)F being typical values. The advantage of a snubber is that it does not draw DC load current. A small series resistor, low tens of ohms, can also be used to isolate reactive loads.

Distortion
The signal voltage range of the \(+\text{VIN}\) terminals is within 3.5V of either supply rail.

One must also consider the range of error currents that will be handled by the \(-\text{VIN}\) terminals. Since the \(-\text{VIN}\) of a CFA is the output of a buffer which replicates the voltage at \(+\text{VIN}\), error currents will flow into the \(-\text{VIN}\) terminal. When an input channel has 100% gain assigned to it, only a small error current flows into its negative input; when low gain is assigned to the channel the output does not respond to the channel’s signal and large error currents flow.

Here are a few idealized examples, based on a gain of +1 for channels A and B and \(R_F = 1\ k\Omega\) for different gain settings:

<table>
<thead>
<tr>
<th>Gain</th>
<th>(V_{\text{INA}})</th>
<th>(V_{\text{INB}})</th>
<th>((-V_{\text{INA}}))</th>
<th>((-V_{\text{INB}}))</th>
<th>(V_{\text{OUT}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>1V</td>
<td>0</td>
<td>0</td>
<td>1 mA</td>
<td>1V</td>
</tr>
<tr>
<td>75%</td>
<td>1V</td>
<td>0</td>
<td>-250 (\mu)A</td>
<td>750 (\mu)A</td>
<td>0.75V</td>
</tr>
<tr>
<td>50%</td>
<td>1V</td>
<td>0</td>
<td>-500 (\mu)A</td>
<td>500 (\mu)A</td>
<td>0.5V</td>
</tr>
<tr>
<td>25%</td>
<td>1V</td>
<td>0</td>
<td>-750 (\mu)A</td>
<td>250 (\mu)A</td>
<td>0.25V</td>
</tr>
<tr>
<td>0%</td>
<td>1V</td>
<td>0</td>
<td>-1 mA</td>
<td>0</td>
<td>0V</td>
</tr>
</tbody>
</table>

Thus, either \(-\text{VIN}\) can receive up to 1 mA error current for 1V of input signal and 1 k\(\Omega\) feedback resistors. The maximum error current is 3 mA for the EL4095, but 2 mA is more realistic. The major contributor of distortion is the magnitude of error currents, even more important than loading effects. The performance curves show distortion versus input amplitude for different gains.

If maximum bandwidth is not required, distortion can be reduced greatly (and signal voltage range enlarged) by increasing the value of \(R_F\) and any associated gain-setting resistor.

100% Accuracies
When a channel gain is set to 100%, static and gain errors are similar to those of a simple CFA. The DC output error is expressed by

\[
V_{\text{OUT, Offset}} = V_{\text{OS}} \cdot A_V + (I_{\text{B}} -) \cdot R_F.
\]

The input offset voltage scales with feed-back gain, but the bias current into the negative input, \(I_{\text{B}} -\), adds an error not dependent on gain. Generally, \(I_{\text{B}} -\) dominates up to gains of about seven.

The fractional gain error is given by

\[
E_{\text{GAIN}} = (R_F + A_V \cdot R_{\text{IN}} -) / R_F + A_V \cdot R_{\text{IN}} / R_{\text{OL}}
\]

The gain error is about 0.3% for a gain of one, and increases only slowly for increasing gain. \(R_{\text{IN}} -\) is the input impedance of the input stage buffer, and \(R_{\text{OL}}\) is the transimpedance of the amplifier, 80 k\(\Omega\) and 350 k\(\Omega\) respectively.

Gain Control Inputs
The gain control inputs are differential and may be biased at any voltage as long as \(V_{\text{GAIN}}\) is less than 2.5V below \(V^+\) and 3V above \(V^-\). The differential input impedance is 5.5 k\(\Omega\), and a common-mode impedance is more than 500 k\(\Omega\). With zero differential voltage on the gain inputs, both signal inputs have a 50% gain factor. Nominal calibration sets the 100% gain of \(V_{\text{INA}}\) input at +0.5V of gain control voltage, and 0% at −0.5V of gain control. \(V_{\text{INB}}\)'s gain is complementary to that of \(V_{\text{INA}}\); +0.5V of gain control sets 0% gain at \(V_{\text{INB}}\) and −0.5V gain control sets 100% \(V_{\text{INB}}\) gain. The gain control does not have a completely abrupt transition at the 0% and 100% points. There is about 10 mV of “soft” transfer at the gain endpoints. To obtain the most accurate 100% gain factor or best attenuation of 0% gain, it is necessary to overdrive the gain control input by about 30 mV. This would set the gain control voltage range as −0.565 mV to +0.565V, or 30 mV beyond the maximum guaranteed 0% to 100% range.
Applications Information — Contd.

In fact, the gain control internal circuitry is very complex. Here is a representation of the terminals:

**Representation of Gain Control**

Inputs $V_G$ and $\bar{V}_G$

For gain control inputs between ±0.5V ($\pm 90\ \mu A$), the diode bridge is a low impedance and all of the current into $V_G$ flows back out through $\bar{V}_G$. When gain control inputs exceed this amount, the bridge becomes a high impedance as some of the diodes shut off, and the $V_G$ impedance rises sharply from the nominal 5.5 KΩ to over 500 KΩ. This is the condition of gain control overdrive. The actual circuit produces a much sharper overdrive characteristics than does the simple diode bridge of this representation.

The gain input has a 20 MHz $-3\ dB$ bandwidth and 17 ns risetime for inputs to ±0.45V. When the gain control voltage exceeds the 0% or 100% values, a 70 ns overdrive recovery transient will occur when it is brought back to linear range. If quicker gain overdrive response is required, the Force control inputs of the EL4095 can be used.

**Force Inputs**

The Force inputs completely override the $V_{GAIN}$ setting and establish maximum attainable 0% and 100% gains for the two input channels. They are activated by a TTL logic low on either of the FORCE pins, and perform the analog switching very quickly and cleanly. FORCEA causes 100% gain on the A channel and 0% on the B channel. FORCEB does the reverse, but there is no defined output state when FORCEA and FORCEB are simultaneously asserted.

The Force inputs do not incur recovery time penalties, and make ideal multiplexing controls. A typical use would be text overlay, where the A channel is a video input and the B channel is digitally created text data. The FORCE input is set low normally to pass the video signal, but released to display overlay data. The gain control can be used to set the intensity of the digital overlay.

**Other Applications Circuits**

The EL4095 can also be used as a variable-gain single input amplifier. If a 0% lower gain extreme is required, one channel’s input should simply be grounded. Feedback resistors must be connected to both $-V_{IN}$ terminals; the EL4095 will not give the expected gain range when a channel is left unconnected.

This circuit gives +0.5 to +2.0 gain range, and is useful as a signal leveller, where a constant output level is regulated from a range of input amplitudes:
Application Information — Contd.

Leveling Circuit with $0.5 \leq A_V \leq 2$

Here the A input channel is configured for a gain of $+2$ and the B channel for a gain of $+1$ with its input attenuated by $\frac{1}{2}$. The connection is virtuous because the distortions do not increase monotonically with reducing gain as would the simple single-input connection.

For video levels, however, these constants can give fairly high differential gain error. The problem occurs for large inputs. Assume that a "twice-size" video input occurs. The A-side stage sees the full amplitude, but the gain would be set to 100% B-input gain to yield an overall gain of...
Application Information — Contd.

½ to produce a standard video output. The 

\(-V_{\text{IN}}\) of the A side is a buffer output that reproduces the input signal, and drives \(R_{\text{GA}}\) and \(R_{\text{FA}}\). Into the two resistors 2.1 mA of error current flows for a typical 1.4V of input DC offset, creating distortion in a A-side input stage. \(R_{\text{GA}}\) and \(R_{\text{FA}}\) could be increased together in value to reduce the error current and distortions, but increasing \(R_{\text{FA}}\) would lower bandwidth. A solution would be to simply attenuate the input signal magnitude and restore the EL4095 output level to standard level with another amplifier so:

Reduced-Gain Leveler for Video Inputs and Differential Gain and Phase Performance (see text)
Application Information — Contd.

Although another amplifier is needed to gain the output back to standard level, the reduced error currents bring the differential phase error to less than 0.1° over the entire input range.

A useful technique to reduce video distortion is to DC-restore the video level going into the EL4095, and offsetting black level to −0.35V so that the entire video span encompasses ±0.35V rather than the unrestored possible span of ±0.7V (for standard-sized signals). For the preceding leveler circuit, the black level should be set more toward −0.7V to accommodate the largest input, or made to vary with the gain control itself (large gain, small offset; small gain, larger offset).

The EL4095 can be wired as a four quadrant multiplier:

**EL4095 Connected as a Four-Quadrant Multiplier**

![Diagram of EL4095 as a Four-Quadrant Multiplier](image-url)
Application Information — Contd.
The A channel gains the input by +1 and the B channel by −1. Feedthrough suppression of the Y input can be optimized by introducing an offset between channel A and B. This is easily done by injecting an adjustable current into the summing junction (−VIN terminal) of the B input channel.

The two input channels can be connected to a common input through two dissimilar filters to create a DC-controlled variable filter. This circuit provides a controlled range of peaking through rolloff characteristics:

![Variable Peaking Filter Diagram](image-url)
Applications Information — Contd.
The EL4095 is connected as a unity-gain fader, with an LRC peaking network connected to the A-input and an RC rolloff network connected to the B-input. The plot shows the range of peaking controlled by the \( V_{\text{GAIN}} \) input. This circuit would be useful for flattening the frequency response of a system, or for providing equalization ahead of a lossy transmission line.

Noise
The electrical noise of the EL4095 has two components: the voltage noise in series with \( +V_{\text{IN}} \) is 5 nV/\( \sqrt{\text{Hz}} \) wideband, and there is a current noise injected into \(-V_{\text{IN}}\) of 35 pA/\( \sqrt{\text{Hz}} \). The output noise will be
\[
V_{\text{n, out}} = \sqrt{(A_V \cdot V_{\text{n, input}})^2 + (I_{\text{n, input}} \cdot R_F)^2}
\]
and the input-referred noise is
\[
V_{\text{n, input-referred}} = \sqrt{(V_{\text{n, input}})^2 + (I_{\text{n, input}} \cdot R_F/A_V)^2}
\]
where \( A_V \) is the fed-back gain of the EL4095. Here is a plot of input-referred noise vs \( A_V \):

Input-Referred Noise vs Closed-Loop Gain

Thus, for a gain of three or more the fader has a noise as good as an op-amp. The only trade-off is that the dynamic range of the input is reduced by the gain due to the nonlinearity caused by gained-up output signals.

Power Dissipation
Peak die temperature must not exceed 150°C. This allows 75°C internal temperature rise for a 75°C ambient. The EL4095 in the 14-pin PDIP package has a thermal resistance of 65°C/W, and can thus dissipate 1.15W at a 75°C ambient temperature. The device draws 20 mA maximum supply current, only 600 mW at \( \pm 15 \)V supplies, and the circuit has no dissipation problems in this package.

The SO-14 surface-mount package has a 105°C/W thermal resistance with the EL4095, and only 714 mW can be dissipated at 75°C ambient temperature. The EL4095 thus can be operated with \( \pm 15 \)V supplies at 75°C, but additional dissipation caused by heavy loads must be considered. If this is a problem, the supplies should be reduced to \( \pm 5 \)V to \( \pm 12 \)V levels.

The output will survive momentary short-circuits to ground, but the large available current will overheat the die and also potentially destroy the circuit's metal traces. The EL4095 is reliable within its maximum average output currents and operating temperatures.

EL4095C Macromodel
This macromodel is offered to allow simulation of general EL4095 behavior. We have included these characteristics:

- Small-signal frequency response
- Signal path DC distortions
- Output loading effects
- \( V_{\text{GAIN}} \) I-V characteristics
- Input impedance
- \( V_{\text{GAIN}} \) overdrive recovery delay
- Off-channel feedthrough
- 100% gain error
- Output impedance over frequency
- FORCE operation
- \(-V_{\text{IN}}\) characteristics and sensitivity to parasitic capacitance

These will give a good range of results of various operating conditions, but the macromodel does not behave identically as the circuit in these areas:

- Temperature effects
- Manufacturing tolerances
- Signal overload effects
- Supply voltage effects
- Signal and \( V_{\text{GAIN}} \) operating range
- Slewrate limitations
- Current-limit
- Noise
- Video and high-frequency distortions
- Power supply interactions
- Glitch and delay from
- FORCE inputs
EL4095C Macromodel — Contd.

*** EL4095 macromodel ***

******

••••

+VinB

-ForceA

-ForceB

Vout

/Vgain

Vgain

-ForceA

-ForceB

-ForceA

-ForceB

+VinA

+VinA

.SUBCKT 4095macromodel ( 1 2 4 5 7 10 11 13 14 )

***

Rol 810 0 290k
Ccomp 810 0 4.3p
G1 110 0 810 0 -10
Rout 110 0 0.1
Lout 110 7 350n
RLout 110 0 7
Rina+ 14 0 5E6
Rinb+ 1 0 5E6
Rvg 11 0 2E6
Rvgg 10 0 2E6
Rforcea 4 0 1E9
Rforceb 5 0 1E9

******

*** Input channel A

***

Rina 22 313 79
Ra 111 0 1k
Rfeedthrougha 13 313 1.0
Cfeedthrougha 23 13 2500p
Ccompa 111 0 2p
E1a 23 313 302 25 -1
E2a 22 0 14 0 0.9999
Rspicea 23 313 1E12
G1a 111 0 POLY(1) (22,313) 0.0 0.0125 -150E-6
G2a 810 0 POLY(2) (113,0) (113,0) 0.0 0.0 0.0 0.0 0.001

*** Input channel B

***

Rinb 25 302 79
Rb 120 0 1k
Rfeedthroughb 2 302 1.0
Cfeedthroughb 24 2 2500p
Ccompb 120 0 2p
E1b 24 302 22 313 -1
E2b 25 0 1 0 0.9999
Rspiceb 24 302 1E12
G1b 120 0 POLY(1) (25,302) 0.0 0.0125 -150E-6
G2b 810 0 POLY(2) (120,0) (119,0) 0.0 0.0 0.0 0.0 0.001

*** Gain control

***

Rspice1 113 0 1E12
Rspice2 119 0 1E12
R1 114 0 1E7
R11 204 206 2.5E6
R12 205 206 2.5E6
C10 201 0 9.5E-16
D1 114 115 Dclamp
D2 116 114 Dclamp
D3 204 4 Dclamp
EL4095C  Video Gain Control/Fader/Multiplexer

EL4095C Macromodel — Contd.

D4 205 5 Dclamp
.model Dclamp D(TT=200n)
Vtul 206 0 2.4
V1 115 0 4999.3
V2 0 116 4999.3
V3 113 117 0.5
V4 119 118 0.5
V5 203 115 0.7
V6 116 202 0.7
G10 114 0 11 10 -0.001
G11 11 10 114 0 -2E-8
E10 117 0 201 0 1E-4
E11 118 0 201 0 -1E-4
S1 114 200 5 0 Nopen
S2 200 201 4 0 Nopen
S3 203 201 4 0 Nclosed
S4 202 201 5 0 Nclosed
.model Nopen VSWITCH(Ron=100 Roff=1E12 Von=1.6 Voff=1.2)
.model Nclosed VSWITCH( Ron=100 Roff=1E12 Von=1.2 Voff=1.6)
***
.ENDS
******

4095-37
The EL4095 Macromodel Schematic

EL4095C Macromodel — Contd.

The EL4095 Macromodel Schematic
EL4095C Macromodel — Contd.
**Features**

- 3 ns A-B switching
- 300 MHz bandwidth
- Fixed gain of 2, for cable driving
- > 650V/μs slew rate
- TTL/CMOS compatible switch

**Applications**

- RGB multiplexing
- Picture-in-picture
- Cable driving
- HDTV processing
- Switched gain amplifiers
- ADC input multiplexer

**General Description**

The EL4332C is a triple very high speed 2:1 Multiplexer-Amplifier. It is intended primarily for component video multiplexing and is especially suited for pixel switching. The amplifiers have their gain set to 2 internally, which reduces the need for many external components. The gain-of-2 facilitates driving back terminated cables. All three amplifiers are switched simultaneously from their A to B inputs by the TTL/CMOS compatible, common A/B control pin.

A - 3 dB bandwidth of 300 MHz together with 3 ns multiplexing time enable the full performance of the fastest component video systems to be realized.

The EL4332C runs from standard ±5V supplies, and is available in the narrow 16-pin small outline package.

**Connection Diagram**

[Diagram showing the connection of the EL4332C multiplexer-amplifier with labeled pins and connections.]
**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC to VEE</td>
<td>14V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC to any GND</td>
<td>12V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEE to any GND</td>
<td>12V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous Output Current</td>
<td>45 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Any Input</td>
<td>VEE - 0.3V to VCC + 0.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. EJantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TJ = TC = TA.

**Test Level**

- **I**: 100% production tested and QA sample tested per QA test plan QXC0002.
- **II**: 100% production tested at TA = 25°C and QA sample tested at TA = 25°C.
- **III**: QA sample tested per QA test plan QXC0002.
- **IV**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at TA = 25°C for information purposes only.

**DC Electrical Characteristics** \( V_{CC} = +5V, \ V_{EE} = -5V, \) Temperature = 25°C, \( R_L = \infty \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Referred Offset Voltage</td>
<td>8</td>
<td>20</td>
<td></td>
<td>II</td>
<td>mV</td>
</tr>
<tr>
<td>( dV_{OS} )</td>
<td>Input Referred Offset Voltage Delta (Note 1)</td>
<td>2</td>
<td>5</td>
<td></td>
<td>II</td>
<td>mV</td>
</tr>
<tr>
<td>( R_{IN} )</td>
<td>Input Resistance</td>
<td>30</td>
<td></td>
<td></td>
<td>V</td>
<td>kΩ</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>-7</td>
<td>-30</td>
<td></td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>( dI_B )</td>
<td>Input Bias Current Delta (Note 1)</td>
<td>0.5</td>
<td>2.5</td>
<td></td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>( A_V )</td>
<td>Gain</td>
<td>1.94</td>
<td>2.00</td>
<td>2.06</td>
<td>II</td>
<td>V/V</td>
</tr>
<tr>
<td>( dA_V )</td>
<td>Gain Delta (Note 1)</td>
<td>0.5</td>
<td></td>
<td></td>
<td>II</td>
<td>%</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td>3.3</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td>( PSRR )</td>
<td>Power Supply Rejection Ratio</td>
<td>50</td>
<td>70</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Voltage Swing into 500Ω load</td>
<td>±2.7</td>
<td>±3.6</td>
<td>±3/−2.7</td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Voltage Swing into 150Ω load</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Current Output, Measured with 75Ω Load (Note 2)</td>
<td>30</td>
<td>40</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td>( X_{talk_{AB}} )</td>
<td>Crosstalk from Non-selected Input (at DC)</td>
<td>-70</td>
<td>-100</td>
<td></td>
<td>III</td>
<td>dB</td>
</tr>
<tr>
<td>( X_{talk_{CH-CH}} )</td>
<td>Crosstalk from one Amplifier to another Amplifier</td>
<td>-70</td>
<td>-100</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input Logic High Level</td>
<td>2.0</td>
<td></td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input Logic Low Level</td>
<td></td>
<td>0.8</td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Logic Low Input Current (( V_{IN} = 0V ))</td>
<td>-0.3</td>
<td>-40</td>
<td>-80</td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Logic High Input Current (( V_{IN} = 0V ))</td>
<td>-3</td>
<td>0</td>
<td>3</td>
<td>II</td>
<td>μA</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Total Supply Current</td>
<td>38</td>
<td>48</td>
<td>60</td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

Note 1: Each channel’s A-input to its B-input.
Note 2: There is no short circuit protection on any output.
### AC Electrical Characteristics

\[ V_{CC} = +5V, V_{EE} = -5V, \]  
Temperature = 25°C, \( R_L = 150\Omega \), \( C_L = 3 \text{ pF} \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>−3 dB Bandwidth</td>
<td>300</td>
<td>V</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>BW 0.1dB</td>
<td>±0.1 dB Bandwidth</td>
<td>105</td>
<td>V</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>DG</td>
<td>Differential Gain at 3.58 MHz</td>
<td>0.04</td>
<td>V</td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>DP</td>
<td>Differential Phase at 3.58 MHz</td>
<td>0.08</td>
<td>V</td>
<td></td>
<td>V</td>
<td>°</td>
</tr>
<tr>
<td>Pkg</td>
<td>Peaking with Nominal Load</td>
<td>0.2</td>
<td>V</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (4V Square Wave, Measured 25%–75%)</td>
<td>650</td>
<td>V</td>
<td></td>
<td>V</td>
<td>V/μs</td>
</tr>
<tr>
<td>( t_s )</td>
<td>Settling Time to 0.1% of Final Value</td>
<td>13</td>
<td>V</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{SW} )</td>
<td>Time to Switch Inputs</td>
<td>3</td>
<td>V</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot, ( V_{OUT} = 4 V_{P-P} )</td>
<td>8</td>
<td>V</td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>( I_{SO \ ab} )</td>
<td>Input to Input Isolation at 10 MHz</td>
<td>60</td>
<td>V</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>10M</td>
<td>Input to Input Isolation at 100 MHz</td>
<td>40</td>
<td>V</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>( I_{SO \ ch-ch} )</td>
<td>Channel to Channel Isolation at 10 MHz</td>
<td>61</td>
<td>V</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>10M</td>
<td>Channel to Channel Isolation at 100 MHz</td>
<td>50</td>
<td>V</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
</tbody>
</table>

### Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1, A2, A3</td>
<td>&quot;A&quot; inputs to amplifiers 1, 2 and 3 respectively</td>
</tr>
<tr>
<td>B1, B2, B3</td>
<td>&quot;B&quot; inputs to amplifiers 1, 2 and 3 respectively</td>
</tr>
<tr>
<td>GND1, GND2, GND3</td>
<td>These are the individual ground pins for each channel.</td>
</tr>
<tr>
<td>Out1, Out2, Out3</td>
<td>Amplifier outputs. Note: there is no short circuit protection on any output.</td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td>Positive power supply. Typically +5V.</td>
</tr>
<tr>
<td>( V_{EE} )</td>
<td>Negative power supply. Typically −5V.</td>
</tr>
<tr>
<td>A/B</td>
<td>Common input select pin, a logic high selects the &quot;A&quot; inputs, logic low selects the &quot;B&quot; inputs. CMOS/TTL compatible.</td>
</tr>
</tbody>
</table>
Burn In Schematic
Typical Performance Curves

Small Signal Transient Response

Switching to Ground from a Large Signal Uncorrelated Sine Wave

Switching from Ground to a Large Signal Uncorrelated Sine Wave

Large Signal Transient Response

Switching to Ground from a Small Signal Uncorrelated Sine Wave

Switching from Ground to a Small Signal Uncorrelated Sine Wave
Typical Performance Curves — Contd.

Switching Glitch (Inputs at Ground)

Switching from a Family of DC Levels to Ground

Switching from Ground to a Family of DC Levels

Channel A/B Switching Delay

Gain vs Frequency

Gain vs Frequency
Typical Performance Curves — Contd.

**-3 dB BW vs Supply Voltage**

![Graph showing -3 dB bandwidth vs total supply voltage.](image)

**Bandwidth vs Die Temperature**

![Graph showing bandwidth vs die temperature.](image)

**Frequency Response with Capacitive Loads**

![Graph showing frequency response with capacitive loads.](image)

**Input Voltage Noise over Frequency**

![Graph showing input voltage noise over frequency.](image)

**A-Input to B-Input Isolation**

![Graph showing A-input to B-input isolation.](image)

**Channel-Channel Isolation**

![Graph showing channel-channel isolation.](image)
Typical Performance Curves — Contd.

Output Swing vs Supply Voltage

Output Swing vs Frequency

Slew Rate vs Supply Voltage

Slew Rate vs Die Temperature

Supply Current vs Supply Voltage

Maximum Power Dissipation
Typical Applications

Figure 1. Typical Connection for a 2:1 Component Video Multiplexer
Applications

Figure 1 shows a typical use for the EL4332C. The circuit is a component video (R,G,B or Y,U,V) multiplexer. Since the gain of the internal amplifiers has been set to 2, the only extra components needed are the supply decoupling capacitors and the back terminating resistors, if transmission lines are to be driven. The EL4332 can drive backmatched 50Ω or 75Ω loads.

Grounds

It will be noticed that each mux-amp channel has its own separate ground pin. These ground pins have been kept separate to keep the channel separation inside the chip as large as possible. The feedback resistors use these ground pins as their reference. The resistors total 400Ω, so there is a significant signal current flowing from these pins to ground.

The ground pins should all be connected together, to a ground plane underneath the chip. 1 oz. copper for the ground plane is highly recommended.

Further notes and recommended practices for high speed printed circuit board layout can be found in the tutorials in the Elantec databooks.

Supplies

Supply bypassing should be as physically near the power pins as possible. Chip capacitors should be used to minimize lead inductance. Note that larger values of capacitor tend to have larger internal inductances. So when designing for 3 transmission lines or similar moderate loads, a 0.1 µF ceramic capacitor right next to the power pin in parallel with a 22 µF tantalum capacitor placed as close to the 0.1 µF is recommended. For lighter loadings, or if not all the channels are being used, a single 4.7 µF capacitor has been found quite adequate.

Note that component video signals do tend to have a high level of signal correlation. This is especially true if the video signal has been derived from 3 synchronously clocked DACs. This corresponds to all three channels drawing large slew currents simultaneously from the supplies. Thus, proper bypassing is critical.
Logic Inputs
The A/B select, logic input, is internally referenced to ground. It is set at 2 diode drops above ground, to give a threshold of about 1.4V (see Figure 2a). The PNP input transistor requires that the driving gate be able to sink current, typically < 30 \( \mu \)A, for a logic "low". If left to float, it will be a logic "high".

The input PNP transistors have sufficient gain that a simple level shift circuit (see Figure 2b) can be used to provide a simple interface with Emitter Coupled Logic. Typically, 200 mV is enough to switch from a solid logic "low" to a "high".

The capacitor \( C_{ff} \) is only in the network to prevent the A/B pin’s capacitance from slowing the control signal. The network shown level shifts the ECL levels, \(-0.7V\) to \(-1.5V\) to \(+1.6V\) and \(+1.1V\) respectively. The terminating resistor, \( R_{tt} \), is required since the open emitter of the ECL gate can not sink current. If a \(-2V\) rail is not being used, a 220\( \Omega \) to 330\( \Omega \) resistor to the \(-5.2V\) rail would have the same effect.

Expanding the Multiplexer
In Figure 3, a 3:1 multiplexer circuit is shown. The expansion to more inputs is very straightforward. Since the EL4332C has a fixed gain of 2, interstage attenuators may be required as shown in Figure 3. The truth table for the 3:1 multiplexer select lines is:

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>Mux Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>R3, G3, B3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>R2, G2, B2</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>R1, G1, B1</td>
</tr>
</tbody>
</table>

When interstage attenuators are used, the values should be kept down in the region of 50\( \Omega \)–300\( \Omega \). This is to prevent a combination of circuit board stray capacitance and the EL4332C’s input capacitance forming a significant pole. For example, if instead of 100\( \Omega \) as shown, resistors of 1 k\( \Omega \) had been used, and assuming 3 pF of stray and 3 pF of input capacitance, a pole would be formed at about 53 MHz.
Figure 3. Typical Connection for a 3:1 Component Video Multiplexer
A Bandwidth Selectable Circuit
In Figure 4, a circuit is shown that allows three signals to be either low pass filtered or full bandwidth.

This could be useful where an input signal is frequently noisy. The component values shown give a Butterworth LPF response, with a -3 dB frequency of 50 MHz. Note again, the resistor values are low, so that stray capacitance does not affect the desired cut-off frequency.

Figure 4. Switched 50 MHz Low Pass Filter for High/Low Resolution Monitors
EL4332 Macromodel

* EL4332 Macromodel
* Revision A, April 1996

*Applications Hints. The EL4332 has two V<sub>CC</sub> pins, one V<sub>EE</sub> pin, and three ground pins. The V<sub>CC</sub> pins (pins 14 and 15 are internally shorted together in the model, but the ground pins (GND1, GND2, and GND3 (nodes 2, 7, and 10, respectively) must be connected to ground (node 0) using a 1e-6Ω resistor. Alternatively, nodes 2, 7, and 10 may be connected to ground through a 25Ω resistor in parallel with a 4 nH inductor to simulate package and PCB parasitics.

* Connections:

* OUT1
  * GND1
  *  A1
  *  B1
  *  B2
  *  A2
  *  GND2
  *  OUT2
  * 1 2 3 4 5 6 7 8

* OUT3
  * GND3
  *  B3
  *  A3
  *  V<sub>EE</sub>
  *  V<sub>CC</sub>
  *  V<sub>CC</sub>
  *  A/B
  * 9 10 11 12 13 14 15 16

.subckt EL4332/EL 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
**********A B Switch **********
Rshort 14 15 1e-12
rshort1 15 0 100 Meg
Isw 14 110 1.5 mA
vref 111 0 1.6V
q1 101 16 110 qp
q2 102 111 110 qp
R1 101 13 500
R2 102 13 500
Rd1 107 0 100
Esw 107 0 table [v(102, 101)*100] (0,0) (1,1)
**********Amplifier #1 **********
q131 103 3 112 qp
q141 104 114 113 qp
EL4332 Macromodel — Contd.

q151 105 4 115 qp
q161 106 117 116 qp
Ia1 14 112 1 mA
Ia2 14 113 1 mA
Ib1 14 115 1 mA
Ib2 14 116 1 mA
Rga1 112 113 275
Rgb1 115 116 275
R3 103 13 275
R4 104 13 275
R5 105 13 275
R6 106 13 275
R7 114 400
R8 114 2 400
R9 1 117 400
R10 117 2 400
Ediff 108 0 value \( (v(104,103)*v(107)) + (v(106,105)*(1-v(107))) \)
rdiff 108 0 1K

* Compensation Section

* gal 0 134 108 0 1m
rh1 134 0 5 Meg
ccl 134 0 0.6 pF

* Poles

* ep1 141 0 134 0 1.0
rpa1 141 142 200
cpa1 142 0 0.75 pF
rpb1 142 143 200
cpb1 143 0 0.75 pF

* Output Stage

* i01 15 150 1.0 mA
i02 151 13 1.0 mA
q7 13 143 150 qp
q8 15 143 151 qn
q9 15 150 152 qn
q10 13 151 153 qp
ros1 152 1 2
ros2 153 1 2

********* Amplifier #2 *********
q23 203 6 212 qp
q24 204 214 213 qp
q25 205 5 215 qp
q26 206 217 216 qp
EL4332 Macromodel — Contd.

EL4332C
Triple 2:1 300 MHz Mux-Amp \( A_\nu = 2 \)

<table>
<thead>
<tr>
<th>In12</th>
<th>14 212 1 mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>In22</td>
<td>14 213 1 mA</td>
</tr>
<tr>
<td>Ib12</td>
<td>14 215 1 mA</td>
</tr>
<tr>
<td>Ib22</td>
<td>14 216 1 mA</td>
</tr>
<tr>
<td>Rga2</td>
<td>212 213 275</td>
</tr>
<tr>
<td>Rgb2</td>
<td>215 216 275</td>
</tr>
<tr>
<td>R231</td>
<td>203 13 275</td>
</tr>
<tr>
<td>R241</td>
<td>204 13 275</td>
</tr>
<tr>
<td>R251</td>
<td>205 13 275</td>
</tr>
<tr>
<td>R261</td>
<td>206 13 275</td>
</tr>
<tr>
<td>R271</td>
<td>8 214 400</td>
</tr>
<tr>
<td>R281</td>
<td>214 7 400</td>
</tr>
<tr>
<td>R291</td>
<td>8 217 400</td>
</tr>
<tr>
<td>R210</td>
<td>217 7 400</td>
</tr>
<tr>
<td>Ediff2</td>
<td>208 0 value { (v(204,203)\cdot v(107)) + (v(206,205)\cdot (1-v(107))) }</td>
</tr>
<tr>
<td>rdiff2</td>
<td>208 0 1K</td>
</tr>
<tr>
<td>* Compensation Section</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td></td>
</tr>
<tr>
<td>ga2</td>
<td>0 234 208 0 1m</td>
</tr>
<tr>
<td>rh2</td>
<td>234 0 5 Meg</td>
</tr>
<tr>
<td>cc2</td>
<td>234 0 0.6 pF</td>
</tr>
<tr>
<td>* Poles</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td></td>
</tr>
<tr>
<td>ep2</td>
<td>241 0 234 0 1.0</td>
</tr>
<tr>
<td>rpa2</td>
<td>241 242 200</td>
</tr>
<tr>
<td>cpa2</td>
<td>242 0 0.75 pF</td>
</tr>
<tr>
<td>rpb2</td>
<td>242 243 200</td>
</tr>
<tr>
<td>cbp2</td>
<td>243 0 0.75 pF</td>
</tr>
<tr>
<td>* Output Stage</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td></td>
</tr>
<tr>
<td>i012</td>
<td>15 250 1.0 mA</td>
</tr>
<tr>
<td>i022</td>
<td>251 13 1.0 mA</td>
</tr>
<tr>
<td>q271</td>
<td>13 243 250 qp</td>
</tr>
<tr>
<td>q281</td>
<td>15 243 251 qn</td>
</tr>
<tr>
<td>q291</td>
<td>15 250 252 qn</td>
</tr>
<tr>
<td>q201</td>
<td>13 251 253 qp</td>
</tr>
<tr>
<td>ros12</td>
<td>252 8 2</td>
</tr>
<tr>
<td>ros22</td>
<td>253 8 2</td>
</tr>
<tr>
<td>* Amplifier #3</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td></td>
</tr>
<tr>
<td>q331</td>
<td>303 12 312 qp</td>
</tr>
<tr>
<td>q341</td>
<td>304 314 313 qp</td>
</tr>
<tr>
<td>q351</td>
<td>305 11 315 qp</td>
</tr>
<tr>
<td>q361</td>
<td>306 317 316 qp</td>
</tr>
<tr>
<td>In13</td>
<td>14 312 1 mA</td>
</tr>
<tr>
<td>In23</td>
<td>14 313 1 mA</td>
</tr>
</tbody>
</table>
The text contains a Macromodel for the EL4332C Triple 2:1 300 MHz Mux-Amp. The model includes components such as resistors (Rga3, Rgb3, R310, etc.), capacitors (Ediff3, rdiff3, etc.), and current sources (Ib13, Ib23, etc.). It also includes compensation and pole components (ga3, rh3, cc3, ep3, rpa3, cpa3, rpb3, cpb3, etc.). The output stage is also defined with components like q371, q381, q391, q301, ros13, ros23, etc. Additionally, power supply current and models for npn and pnp transistors are specified.
**Features**
- 80 MHz – 3 dB bandwidth for gains of 1 to 10
- 800 V/μs slew rate
- 15 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible DC restore function
- Available in 16 lead P-DIP, 16 lead SOL

**Applications**
- RGB drivers requiring DC restoration
- RGB multiplexers requiring DC restoration
- RGB building blocks
- Video gain blocks requiring DC restoration
- Sync and color burst processing

**General Description**
The EL4390C is three wideband current-mode feedback amplifiers optimized for video performance, each with a DC restore amplifier. The DC restore function is activated by a common TTL/CMOS compatible control signal while each channel has a separate restore reference.

Each amplifier can drive a load of 150Ω at video signal levels. The EL4390C operates on supplies as low as ±4V up to ±15V.

Being a current-mode feedback design, the bandwidth stays relatively constant at approximately 80MHz over the ±1 to ±10 gain range. The EL4390C has been optimized for use with 1300Ω feedback resistors.

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4390CN</td>
<td>-40°C to +85°C</td>
<td>16-Pin P-DIP</td>
<td>MDP0031</td>
<td>1</td>
</tr>
<tr>
<td>EL4390CM</td>
<td>-40°C to +85°C</td>
<td>16-Lead SOL</td>
<td>MDP0027</td>
<td>1</td>
</tr>
</tbody>
</table>

**Connection Diagram**

![Connection Diagram](image)
**Absolute Maximum Ratings** \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Voltage between (V_S^+) and (V_S^-)</strong></td>
<td>+33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Voltage at (V_S^+)</strong></td>
<td>+18V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Voltage at (V_S^-)</strong></td>
<td>-18V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Voltage between (V_{IN}^+) and (V_{IN}^-)</strong></td>
<td>±6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Current into (V_{IN}^+) and (V_{IN}^-)</strong></td>
<td>5mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Internal Power Dissipation**

See Curves

**Operating Ambient Temp. Range**

-40°C to +85°C

**Operating Junction Temperature**

150°C

**Storage Temperature Range**

-65°C to +150°C

---

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25°C) and QA sample tested at (T_A = 25°C); (T_{MAX} \text{ and } T_{MIN}) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25°C) for information purposes only.</td>
</tr>
</tbody>
</table>

---

**Open Loop DC Electrical Characteristics** Supplies at \(\pm 15V\), Load = 1KΩ

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Amplifier Section (not restored)</strong></td>
<td><strong>Input Offset Voltage</strong></td>
<td>+25°C</td>
<td>2</td>
<td>15</td>
<td>II</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td><strong>Input Bias Current</strong></td>
<td>(I_{IN}^+)</td>
<td>+25°C</td>
<td>0.2</td>
<td>5</td>
<td>II</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>Input Bias Current</strong></td>
<td>(I_{IN}^-)</td>
<td>+25°C</td>
<td>10</td>
<td>65</td>
<td>II</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>Transimpedance (Note 1)</strong></td>
<td>(R_{DL})</td>
<td>+25°C</td>
<td>100</td>
<td>220</td>
<td>II</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td><strong>Transimpedance (Note 1)</strong></td>
<td>(R_{IN}^-)</td>
<td>+25°C</td>
<td>50</td>
<td></td>
<td>V</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td><strong>Common-Mode Rejection Ratio (Note 2)</strong></td>
<td>CMRR</td>
<td>+25°C</td>
<td>50</td>
<td>56</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td><strong>Power Supply Rejection Ratio (Note 4)</strong></td>
<td>PSRR</td>
<td>+25°C</td>
<td>50</td>
<td>70</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td><strong>Output Voltage Swing; (R_L = 1kΩ)</strong></td>
<td>(V_o)</td>
<td>+25°C</td>
<td>±12</td>
<td>±13</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>Short-Circuit Current</strong></td>
<td>(I_{SC})</td>
<td>+25°C</td>
<td>45</td>
<td>70</td>
<td>100</td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Supply Current (Quiescent)</strong></td>
<td>(I_{SY})</td>
<td>+25°C</td>
<td>10</td>
<td>20</td>
<td>32</td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Restoring Section**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input Offset Voltage</strong></td>
<td>Composite (V_{OS, COMP}) (\text{(Note 3)})</td>
<td>+25°C</td>
<td>8</td>
<td>35</td>
<td>II</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td><strong>Input Bias Current</strong></td>
<td>Restore (I_{IN}^+) (\text{Bias Current})</td>
<td>+25°C</td>
<td>0.2</td>
<td>5</td>
<td>II</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>Restoring Current Available</strong></td>
<td>(I_{OUT})</td>
<td>+25°C</td>
<td>2</td>
<td>4</td>
<td>II</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td><strong>Power Supply Rejection Ratio (Note 4)</strong></td>
<td>PSRR</td>
<td>+25°C</td>
<td>50</td>
<td>70</td>
<td>II</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td><strong>Conductance</strong></td>
<td>(G_{OUT})</td>
<td>+25°C</td>
<td>8</td>
<td></td>
<td>V</td>
<td>mA/V</td>
<td></td>
</tr>
<tr>
<td><strong>Supply Current, Restoring</strong></td>
<td>(I_{SY, RES})</td>
<td>+25°C</td>
<td>10</td>
<td>23</td>
<td>37</td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td><strong>RES Logic Low Threshold</strong></td>
<td>(V_{IL, RES})</td>
<td>+25°C</td>
<td>1.0</td>
<td>1.4</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>RES Logic High Threshold</strong></td>
<td>(V_{IH, RES})</td>
<td>+25°C</td>
<td>1.4</td>
<td>1.8</td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
**Open Loop DC Electrical Characteristics** Supplies at ±15V, Load = 1kΩ — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Restoring Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;IL, RES&lt;/sub&gt;</td>
<td>RES Input Current, Logic Low</td>
<td>+25°C</td>
<td>2</td>
<td>10</td>
<td>III</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;IH, RES&lt;/sub&gt;</td>
<td>RES Input Current, Logic High</td>
<td>+25°C</td>
<td>0.5</td>
<td>3</td>
<td>III</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: For current feedback amplifiers, \( A_{VOL} = R_{OL}/R_{IN} \).
Note 2: \( V_{CM} = ±10V \) for \( V_S = ±15V \).
Note 3: Measured from \( V_{CL} \) to amplifier output, while restoring.
Note 4: \( V_{OS} \) is measured at \( V_S = ±4.5V \) and \( V_S = ±16V \), both supplies are changed simultaneously.

**Closed Loop AC Electrical Characteristics**

Supplies at ±15V, Load = 150Ω and 15 pF, \( T_A = 25°C \) (See note 7 re: test fixture)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Amplifier Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (Note 5)</td>
<td>800</td>
<td>V</td>
<td>V</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate w/ ±5V Supplies (Note 5)</td>
<td>550</td>
<td>V</td>
<td>V</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth, −3dB, ( A_V = 1 )</td>
<td>95</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth, −0.1 dB</td>
<td>72</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth, −0.1 dB</td>
<td>20</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth, −0.1 dB</td>
<td>14</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain at 3.58 MHz</td>
<td>0.02</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain at 3.58 MHz</td>
<td>0.02</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dθ</td>
<td>Differential Phase at 3.58 MHz</td>
<td>0.03</td>
<td>V</td>
<td>(°)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dθ</td>
<td>Differential Phase at 3.58 MHz</td>
<td>0.06</td>
<td>V</td>
<td>(°)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Restoring Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{RE} )</td>
<td>Time to Enable Restore</td>
<td>35</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{RD} )</td>
<td>Time to Disable Restore</td>
<td>35</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 5: SR is measured at 20% to 80% of 4V pk-pk square wave, with \( A_V = 5 \), \( R_F = 820\Omega \), \( R_G = 200\Omega \).
Note 6: DC offset from −0.714V to +0.714V, AC amplitude is 286m Vp-p, equivalent to 40 ire.
Note 7: Test fixture was designed to minimize capacitance at the \( I_M \) input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.
Table 1. Charge Storage Capacitor Value vs. Droop and Charging Rates

<table>
<thead>
<tr>
<th>Cap Value (nF)</th>
<th>Droop in 60μS (mV)</th>
<th>Charge in 2μS (mV)</th>
<th>Charge in 4μS (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>30</td>
<td>400</td>
<td>800</td>
</tr>
<tr>
<td>22</td>
<td>13.6</td>
<td>182</td>
<td>364</td>
</tr>
<tr>
<td>47</td>
<td>6.4</td>
<td>85</td>
<td>170</td>
</tr>
<tr>
<td>100</td>
<td>3.0</td>
<td>40</td>
<td>80</td>
</tr>
<tr>
<td>220</td>
<td>1.36</td>
<td>18</td>
<td>36</td>
</tr>
</tbody>
</table>

These numbers represent the worst case bias current, and the worst case charging current. Note that to get the full (2mA+) charging current, the clamp input must have >250mV of error voltage.

Note that the magnitude of the bias current will decrease as temperature increases.

The basic droop formula is:
\[ V(\text{droop}) = I_B^+ \times \frac{\text{Line time} - \text{Charge time}}{\text{capacitor value}} \]

and the basic charging formula is:
\[ V(\text{charge}) = I_{\text{OUT}} \times \frac{\text{Charge time}}{\text{capacitor value}} \]

Where \( I_{\text{OUT}} \) is:
\[ I_{\text{OUT}} = \frac{(\text{Clamp voltage} - \text{IN}^+ \text{voltage})}{120} \]
Typical Performance Curves

Gain Flatness for Various RF
\( V_S = \pm 15V, A_V = 0 \text{ dB} \)

Gain Flatness for Various RF
\( V_S = \pm 5V, A_V = 0 \text{ dB} \)

Gain Flatness for Various RF and RG Values
\( V_S = \pm 15V, A_V = 6 \text{ dB} \)

Gain Flatness for Various RF and RG Values
\( V_S = \pm 5V, A_V = 6 \text{ dB} \)

Phase Shift for \( A_V = 2, \quad R_F = R_G = 1300\Omega \)

Phase Shift for \( A_V = 2, \quad R_F = R_G = 1000\Omega \)
at \( V_S = \pm 5V \) and \( V_S = \pm 15V \)

Gain Flatness for Various RF and RG Values
\( V_S = \pm 15V, A_V = 4 \text{ dB}, \quad R_F/R_G \) as Shown

Gain Flatness for Various RF and RG Values
\( V_S = \pm 5V, A_V = 4 \text{ dB}, \quad R_F/R_G \) as Shown

Phase Shift for \( A_V = 5 \text{ dB}, \quad R_F = 820\Omega, \quad R_G = 2000\Omega, \quad V_S = \pm 5V \)
Typical Performance Curves — Contd.

Gain Flatness
Vs = ±5V, AV = 26 dB, RF = 680Ω, RG = 36Ω

Differential Gain
at Vs = ±15V

Differential Phase
at Vs = ±15V

Differential Gain
at Vs = ±5V

Differential Phase
at Vs = ±5V

Frequency Response
for Various CLOAD, Vs = ±15V, RF = RG = 1300Ω

Frequency Response
for Various CLOAD, Vs = ±5V, RF = RG = 1300Ω

Crosstalk,
Channel R and B to Channel G,
Vs = ±5V, RF = RG = 1300Ω
Typical Performance Curves — Contd.

Crosstalk,
The Channel R and G to Channel B, 
\( V_S = \pm 5V, R_F = 1300\Omega \)

-10
-30
-50
-70
-90

Gain (dB)

100 1k 10k 100k 1M 10M 100M

Frequency (Hz)

\( V_S = \pm 5V \)

\( V_S = \pm 5V \)

\( V_S = \pm 5V \)

\( V_S = \pm 15V \)

\( V_S = \pm 5V \)

Phase Shift at \( I_{N+} \) Pin

during Restore,

\( R_S = 75\Omega \) and \( 150\Omega \), \( V_S = \pm 5V \)

\( R_S = 75\Omega \)

\( R_S = 150\Omega \)

\( 10k \) 100k 1M 10M 100M

Frequency (Hz)

IN+ Input Impedance

during HOLD, \( V_S = \pm 5V \)

Impedance (\( \Omega \))

Phase (°)

10k 100k 1M 10M 100M

Frequency (Hz)

IN+ Input Impedance

during SAMPLE, \( V_S = \pm 5V \)

Impedance (\( \Omega \))

Phase (°)

10k 100k 1M 10M 100M

Frequency (Hz)

Phase Restoring vs Clamp,

Voltage at \( V_S = \pm 5V \)

\( I_{OUT} \) Restoring vs Clamp,

\( V_S = \pm 5V \)

\( I_{OUT} = 5.0 \) mA

\( \text{Clamp Voltage (V)} \)

-2.5 0 2.5

-2.5

Frequency (Hz)

Output during DC-Restoration,

Showing DC Droop

\( R_F = R_G = 1300\Omega , \ V_S = \pm 5V \)

\( R_F = 820\Omega \) and \( R_G = 200\Omega \)

\( V_S = \pm 15V \)

Output (V)

-0.6 -0.9 -1.2 -1.5 -1.8 -2.1

Time (μs)

Output (V)

-0.6 -0.9 -1.2 -1.5 -1.8 -2.1

Time (μs)

Output (V)

-0.6 -0.9 -1.2 -1.5 -1.8 -2.1

Time (μs)

 \( A_V = 2 \) 

 \( A_V = 5 \) 

Pulse Response with \( A_V = 2 \), 

\( R_F = R_G = 1300\Omega \) at \( V_S = \pm 5V \)

Pulse Response with \( A_V = 5 \), 

\( R_F = 820\Omega \) and \( R_G = 200\Omega \)

\( V_S = \pm 15V \)
Typical Performance Curves — Contd.

Maximum Power Dissipation vs Ambient Temperature—
16-Pin PDIP

Maximum Power Dissipation vs Ambient Temperature—
16-Pin SOL

Simplified Schematic of One Channel of EL4390
Applications Information

Circuit Operation
Each channel of the EL4390 contains a current feedback amplifier and a TTL/CMOS compatible clamp circuit. The current that the clamp can source or sink into the non-inverting input is approximately:

\[ I = \frac{V_{CLAMP} - V_{IN+}}{120} \]

So, when the non-inverting input is at the same voltage as the clamp reference, no current will flow, and hence no charge is added to the capacitor. When there is a difference in voltage, current will flow, in an attempt to cancel the error at the NON-INVERTING input. The amplifier's offset voltage and \((I_B^- \times R_F)\) DC errors are not cancelled with this loop. It is purely a method of adding a controlled DC offset to the signal.

As well as the offset voltage error, which goes up with gain, and the \(I_B^- \times R_F\) error which drops with gain, there is also the \(I_B^+\) error term. Since the amplifier is capacitively coupled, this small current is slowly integrated and shows up as a very slow ramp voltage. Table below shows the output voltage drift in 60µS for various values of coupling capacitor, all assuming the very worst \(I_B^+\) current.

Table 1. Charge Storage Capacitor Value vs. Droop and Charging Rates

<table>
<thead>
<tr>
<th>Cap Value (nF)</th>
<th>Droop in 60µS (mV)</th>
<th>Charge in 2µS (mV)</th>
<th>Charge in 4µS (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>30</td>
<td>400</td>
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</tr>
<tr>
<td>100</td>
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<td>40</td>
<td>80</td>
</tr>
<tr>
<td>220</td>
<td>1.36</td>
<td>18</td>
<td>36</td>
</tr>
</tbody>
</table>

In normal circuit operation, the picture content will also cause a slow change in voltage across the capacitor, so at every back porch time period, these error terms can be corrected.

When a signal source is being switched, eg. from two different surveillance cameras, it is recommended to synchronize the switching with the vertical blanking period, and to drive the HOLD pin (pin 6) low, during these lines. This will ensure that the system has been completely restored, regardless of the average intensity of the two pictures.

Application Hints

Figures 1 & 2 shows a three channel DC-restoring system, suitable for R-G-B or Y-U-V component video, or three synchronous composite signals.

Figure 1 shows the amplifiers configured for non-inverting gain, and Figure 2 shows the amplifiers configured for inverting gains. Note that since the DC-restoring function is accomplished by clamping the amplifier's non-inverting input, during the back porch period, any signal on the non-inverting input will be distorted. For this reason, it is recommended to use the inverting configuration for composite video, since this avoids the color burst being altered during the clamp time period.

Since all three amplifiers are monolithic, they run at the same temperature, and will have very similar input bias currents. This can be used to advantage, in situations where the droop voltage needs to be compensated, since a single trim circuit can be used for all three channels. A 560KΩ or similar value resistor helps to isolate each signal. See Figure 2. The advantage of compensating for the droop voltage, is that a smaller capacitor can be used, which allows a larger level restoration within one line. See Table 1 for values of capacitor and charge/droop rates.
Applications Information — Contd.

Figure 1
Applications Information — Contd.

Figure 2
Applications Information — Contd.

Figure 3
Applications Information — Contd.
In Figure 3, one of the three channels is used, together with a low-offset op-amp, to automatically trim the bias current of the other two channels. The two remaining channels are shown in the non-inverting configuration, but could equally well be set to provide inverting gains. Two DC-restored channels are typically needed in fader applications. See the EL4094 and EL4095 for suitable, monolithic video faders.

Layout and Dissipation Considerations

As with all high frequency circuits, the supplies should be bypassed with a 0.1μF ceramic capacitor very close to the supply pins, and a 4.7μF tantalum capacitor fairly close, to handle the high current surges. While a ground plane is recommended, the amplifier will work well with a “star” grounding scheme. The pin 3 ground is only used for the internal bias generator and the reference for the TTL compatible “HOLD” input.

As with all current feedback capacitors, all stray capacitance to the inverting inputs should be kept as low as possible, to avoid unwanted peaking at the output. This is especially true if the value of Rf has already been reduced to raise the bandwidth of the part, while tolerating some peaking. In this situation, additional capacitance on the inverting input can lead to an unstable amplifier.

Since there are three amplifiers all in one package, and each amplifier can sink or source typically more than 70mA, some care is needed to avoid excessive die temperatures. Sustained, DC currents, of over 30mA, are not recommended, due to the limited current handling capability of the metal traces inside the IC. Also, the short circuit protection can be tripped with currents as low as 45mA, which is seen as excessive distortion in the output waveform. As a quick rule of thumb, both the SOL and DIP 16 pin packages can dissipate about 1.4 watts at 25°C, and with ±15V supplies and a worst case quiescent current of 32mA, yields 0.96 watts, before any load is driven.

Dissipation of the EL4390 can be reduced by lowering the supply voltage. Although some performance is degraded at lower supplies, as seen in the characteristic curves, it is often found to be a useful compromise. The bandwidth can be recovered, by reducing the value of Rf, and RG as appropriate.
Features

- Unity or +2-gain bandwidth of 80 MHz
- 70 dB off-channel isolation at 4 MHz
- Directly drives high-impedance or 75Ω loads
- .02% and .02° differential gain and phase errors
- 8 ns switching time
- <100 mV switching glitch
- 0.2% loaded gain error
- Compatible with ±3V to ±15V supplies
- 160 mW maximum dissipation at ±5V supplies

General Description

The EL44XX family of video multiplexed-amplifiers offers a very quick 8 ns switching time and low glitch along with very low video distortion. The amplifiers have good gain accuracy even when driving low-impedance loads. To save power, the amplifiers do not require heavy loading to remain stable.

The EL4421 and EL4422 are two-input multiplexed amplifiers. The inputs of the input stages are wired together and the device can be used as a pin-compatible upgrade from the MAX453.

The EL4441 and EL4442 have four inputs, also with common feedback. These may be used as upgrades of the MAX454.

The EL4443 and EL4444 are also 4-input multiplexed amplifiers, but both positive and negative inputs are wired separately. A wide variety of gain- and phase-switching circuits can be built using independent feedback paths for each channel.

The EL4421, EL4441, and EL4443 are internally compensated for unity-gain operation. The EL4422, EL4442, and EL4444 are compensated for gains of +2 or more, especially useful for driving back-matched cables.

The amplifiers have an operational temperature of −40°C to +85°C and are packaged in plastic 8- and 14-pin DIP and 8- and 14-pin SO.

The EL44XX multiplexed-amplifier family is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_+$</td>
<td>Positive Supply Voltage</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>$V_+$ to $V_-$ Supply Voltage</td>
<td>33V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Voltage at any Input or Feedback</td>
<td>$V_+$ to $V_-$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{IN}$</td>
<td>Difference between Pairs of Inputs or Feedback</td>
<td>6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{LOGIC}$</td>
<td>Voltage at A0 or A1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Current into any Input, Feedback, or Logic Pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>30 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_D$</td>
<td>Maximum Power Dissipation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elanec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_{J} = T_{C} = T_{A}$.

### Open-Loop DC Electrical Characteristics

Power supplies at $\pm 5V$, $T_A = 25^\circ C$, $R_L = 500\Omega$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current, Positive Inputs Only of the '21, '22, '41, '42, and All Inputs of the '43 and '44</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>Input Bias Currents of Common Feedback</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Currents of the '43 and '44</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E_G$</td>
<td>Gain Error of the '21 and '41 and '43 (Note 1) '22, '42 and '44</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{VOL}$</td>
<td>Open-Loop Gain (Note 1) EL4443</td>
<td>350</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4444</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input Signal Range, EL4421 and EL4441 (Note 2)</td>
<td>±2.5</td>
<td>±3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio, EL4443 and EL4444</td>
<td>70</td>
<td>90</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio $V_s$ from $\pm 5V$ to $\pm 15V$</td>
<td>60</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Open-Loop DC Electrical Characteristics — Contd.**

Power supplies at ±5V, T_A = 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMIR</td>
<td>Common-Mode Input Range (Note 3) EL4443 and EL4444</td>
<td>± 2.5</td>
<td>± 3</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOUT</td>
<td>Output Swing</td>
<td>± 2.5</td>
<td>± 3.5</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>ISC</td>
<td>Output Short-Circuit Current</td>
<td>± 40</td>
<td>± 80</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>F_T</td>
<td>Unselected Channel Feedthrough '21, '41, '43</td>
<td>70</td>
<td>80</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Attenuation, (Note 1) '22, '42, '44</td>
<td>55</td>
<td>64</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>I_LOGIC</td>
<td>Input Current at A0 and A1 with Input = 0V and 5V</td>
<td>−16</td>
<td>−8</td>
<td>0</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>V_LOGIC</td>
<td>Logic Valid High and Low Input Levels</td>
<td>0.8</td>
<td>2.0</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_S</td>
<td>Supply Current EL4421 and EL4422</td>
<td>11</td>
<td>14</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4441, EL4442, EL4443, and EL4444</td>
<td>13</td>
<td>16</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The '21, '41, and '43 devices are connected for unity-gain operation with 75Ω load and an input span of ±1V. The '22, '42, and '44 devices are connected for a gain of +2 with a 150Ω load and a ±1V input span with R_F = R_G = 270Ω.

Note 2: The '21 and '41 devices are connected for unity gain with a ±3V input span while the output swing is measured.

Note 3: CMIR is assured by passing the CMRR test at input voltage extremes.

**Closed-Loop AC Electrical Characteristics**

Power supplies at ±5V, T_A = 25°C, for EL4421, EL4441, and EL4443 A_V = +1 and R_L = 500Ω, for EL4422, EL4442, and EL4444 A_V = +2 and R_L = 150Ω with R_F = R_G = 270Ω and C_F = 3 pF; for all C_L = 15 pF

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>BW − 3 dB</td>
<td>−3 dB Small-Signal Bandwidth, EL4421, '41, '43</td>
<td>80</td>
<td>65</td>
<td>V</td>
<td>MHz</td>
<td></td>
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<tr>
<td></td>
<td>EL4422, '42, '44</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>BW ± 0.1 dB</td>
<td>0.1 dB Flatness Bandwidth</td>
<td>10</td>
<td>V</td>
<td>V</td>
<td>MHz</td>
<td></td>
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<tr>
<td>Peaking</td>
<td>Frequency Response Peaking</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slewrate, V_OUT between −2.5V and +2.5V, V_S = ±12V</td>
<td>150</td>
<td>200</td>
<td>I</td>
<td>V/μsec</td>
<td></td>
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<tr>
<td></td>
<td>EL4421, EL4441, EL4443</td>
<td></td>
<td></td>
<td>I</td>
<td>V/μsec</td>
<td></td>
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<tr>
<td></td>
<td>EL4422, EL4442, EL4444</td>
<td>180</td>
<td>240</td>
<td>I</td>
<td>V/μsec</td>
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<td>V_n</td>
<td>Input-Referred Noise Voltage Density</td>
<td>18</td>
<td>V</td>
<td>V</td>
<td>nV/rt-hz</td>
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<td></td>
<td>EL4421, EL4441, EL4443</td>
<td></td>
<td></td>
<td>V</td>
<td>nV/rt-hz</td>
<td></td>
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<tr>
<td></td>
<td>EL4422, EL4442, EL4444</td>
<td>14</td>
<td>V</td>
<td>V</td>
<td>nV/rt-hz</td>
<td></td>
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<tr>
<td>d_G</td>
<td>Differential Gain Error, V_OFFSET between −0.7V and +0.7V</td>
<td>0.01</td>
<td>V</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4421, EL4441, EL4443</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4421, EL4441, EL4443</td>
<td>0.10</td>
<td>V</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4422, EL4442, EL4444</td>
<td>0.02</td>
<td>V</td>
<td>V</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4422, EL4442, EL4444</td>
<td>0.11</td>
<td>V</td>
<td>V</td>
<td>%</td>
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</tr>
</tbody>
</table>
Closed-Loop AC Electrical Characteristics

Power supplies at ±5V. TA = 25°C, for EL4421, EL4441, and EL4443 AV = +1 and RL = 500Ω, for EL4422, EL4442, and EL4444 AV = +2 and RL = 150Ω with RF = RG = 270Ω and CF = 3 pF; for all CL = 15 pF — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>dφ</td>
<td>Differential Phase Error, VOFFSET between −0.7V and +0.7V</td>
<td>0.01</td>
<td>V</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td></td>
<td>EL4421, EL4441, EL4443 (VS = ±12V)</td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td></td>
<td>EL4421, EL4441, EL4443 (VS = ±5V)</td>
<td>0.02</td>
<td>V</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td></td>
<td>EL4422, EL4442, EL4444 (VS = ±12V)</td>
<td>0.15</td>
<td>V</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td></td>
<td>EL4422, EL4442, EL4444 (VS = ±5V)</td>
<td>12</td>
<td>V</td>
<td></td>
<td>nsec</td>
<td></td>
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<tr>
<td>TMUX</td>
<td>Multiplex Delay Time, Logic Threshold to 50% Signal Change</td>
<td>8</td>
<td>V</td>
<td></td>
<td>nsec</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4421, '22</td>
<td>100</td>
<td>V</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4441, '42, '43, '44</td>
<td>70</td>
<td>V</td>
<td></td>
<td>mV</td>
<td></td>
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<tr>
<td>VGLITCH</td>
<td>Peak Multiplex Glitch</td>
<td>76</td>
<td>V</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4421, '22</td>
<td>63</td>
<td>V</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>ISO</td>
<td>Channel Off Isolation at 3.58 MHz (See Text)</td>
<td>76</td>
<td>V</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4421, EL4441, EL4443</td>
<td>63</td>
<td>V</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL4422, EL4442, EL4444</td>
<td>76</td>
<td>V</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

Typical Performance Curves

EL4421, EL4441, and EL4443
Small-Signal Transient Response

\[ V_S = \pm 5V, \; R_L = 500\Omega \]

Large-Signal Response

\[ V_S = \pm 12V, \; R_L = 500\Omega \]
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443
Frequency Response for Various Loads
\( V_S = \pm 5\text{V}, A_V = +1 \)

EL4422, EL4442, and EL4444
Frequency Response for Various Loads
\( V_S = \pm 15\text{V}, A_V = +2 \)

EL4443 Open-Loop Gain and Phase vs Frequency

EL4444 Open-Loop Gain and Phase vs Frequency
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443
- 3 dB Bandwidth, Slewrate, and Peaking vs Supply Voltage

EL4422, EL4442, and EL4444
- 3 dB Bandwidth, Slewrate, and Peaking vs Supply Voltage

EL4421, EL4441, and EL4443
Bandwidth, Slewrate, and Peaking vs Temperature, \( A_V = +1, R_C = 500 \Omega \)

EL4422, EL4442, and EL4444 Bandwidth,
Slewrate, and Peaking vs Temperature,
\( A_V = +2, R_D = 150 \Omega, R_C = 27 \Omega, C_Y = 3 \text{ pF} \)

EL4421, EL4441, and EL4443
- 3 dB Bandwidth and Gain Error vs Load Resistance

Input Noise vs Frequency
Typical Performance Curves — Contd.

**EL4421, EL4441, and EL4443 Differential Gain and Phase Errors vs Input Offset; AV = +1, RL = 500Ω, F = 3.58 MHz**

**EL4422, EL4442, and EL4444 Differential Gain and Phase Errors vs Input Offset; AV = +2, RL = 1500Ω, F = 3.58 MHz**

**EL4443 and EL4444 Open-Loop Gain vs Load Resistance**

Change in VOS, AV, and IB with Supply Voltage

Change in VOS, AV, and IB vs Temperature
Typical Performance Curves — Contd.

Switching Waveforms
Switching from Grounded Input to Uncorrelated Sinewave and Back

Channel-to-Channel Switching Glitch

EL4421, EL4441, and EL4443
Unselected Channel Feedthrough vs Frequency

EL4422, EL4442, and EL4444
Unselected Channel Feedthrough vs Frequency

EL4443 and EL4444
Input and Output Range vs Supply Voltage (Output Unloaded)
Applications Information

General Description
The EL44XX family of video mux-amps are composed of two or four input stages whose inputs are selected and control an output stage. One of the inputs is active at a time and the circuit behaves as a traditional voltage-feedback op-amp for that input, rejecting signals present at the unselected inputs. Selection is controlled by one or two logic inputs.

The EL4421, EL4422, EL4441, and EL4442 have all + inputs and − inputs brought out separately so that the input stage can be wired for independent gains and gain polarities with separate feedback networks.

EL4443 and EL4444, on the other hand, have all + inputs and − inputs brought out separately so that the input stage can be wired for independent gains and gain polarities with separate feedback networks.

The EL4421, EL4441, and EL4443 are compensated for unity-gain stability, while the EL4422, EL4442, and EL4444 are compensated for a feedback gain of +2, ideal for driving back-terminated cables or maintaining bandwidth at higher feedback gains.
Applications Information — Contd.

Switching Characteristics

The logic inputs work with standard TTL levels of 0.8V or less for a logic 0 and 2.0V or more for a logic 1, making them compatible for TTL and CMOS drivers. The ground pin is the logic threshold biasing reference. The simplified input circuitry is shown below:

![Simplified Logic Input Circuitry](image1)

The ground pin draws a maximum DC current of 6 μA, and may be biased anywhere between \((V^-) + 2.5V\) and \((V^+) - 3.5V\). The logic inputs may range from \((V^-) + 2.5V\) to \(V^+\), and are additionally required to be no more negative than \(V(Gnd\ pin) - 4V\) and no more positive than \(V(Gnd\ pin) + 6V\).

For example, within these constraints, we can power the EL44XX’s from \(+5V\) and \(+12V\) without a negative supply by using these connections:

![Using the EL44XX Mux Amps with +5V and +12V Supplies](image2)
Applications Information — Contd.

The logic input(s) and ground pin are shifted 2.5V above system ground to correctly bias the mux-amp. Of course, all the signal inputs and output will have to be shifted 2.5V above system ground to ensure proper signal path biasing.

A final caution: the ground pin is also connected to the IC’s substrate and frequency compensation components. The ground pin must be returned to system ground by a short wire or nearby bypass capacitor. In figure 2, the 22 KΩ resistors also serve to isolate the bypassed ground pin from the +5V supply noise.

Signal Amplitudes

Signal input and output voltages must be between \((V^-) + 2.5V\) and \((V^+) - 2.5V\) to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. In unity-gain connections, any input could have ±3V applied and the output would be at ±3V, putting us at our 6V differential limit. Higher-gain circuit applications divide the output voltage and allow for larger outputs. For instance, at a gain of +2 the maximum input is again ±3V and the output swing is ±6V. The EL4443 or EL4444 can be wired for inverting gain with even more amplitude possible.

The output and positive inputs respond to overloading amplitudes correctly; that is, they simply clamp and remain monotonic with increasing +input overdrive. A condition exists, however, where the −input of an active stage is overdriven by large outputs. This occurs mainly in unity-gain connections, and only happens for negative inputs. The overloaded input cannot control the feedback loop correctly and the output can become non-monotonic. A typical scenario has the circuit running on ±5V supplies, connected for unity gain, and the input is the maximum ±3V. Negative input extremes can cause the output to jump from −3V to around −2.3V. This will never happen if the input is restricted to ±2.5V, which is the guaranteed maximum input compliance with ±5V supplies, and is not a problem with greater supply voltages. Connecting the feedback network with a divider will prevent the overloaded output voltage from being large enough to overload the −input and monotonic
behavior is assured. In any event, keeping signals within guaranteed compliance limits will assure freedom from overload problems.

The input and output ranges are substantially constant with temperature.

**Power Supplies**

The mux-amps work well on any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the Gnd pin are observed (see the Switching Characteristics section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 µF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 µF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used as described in the Switching Characteristics section. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the mux-amps increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

\[ P_D = 2V_S \times I_{s,\text{max}} + (V_S - V_O) \times V_O / R_{\text{PAR}} \]

Where \( I_{s,\text{max}} \) is the maximum supply current
\( V_S \) is the ± supply voltage (assumed equal)
\( V_O \) if the output voltage
\( R_{\text{PAR}} \) is the parallel of all resistors loading the output

For instance, the EL4422 draws a maximum of 14 mA and we might require a 2V peak output into 150Ω and a 270Ω +270Ω feedback divider. The \( R_{\text{PAR}} \) is 117Ω. The dissipation with ±5V supplies is 191 mW. The maximum Supply voltage that the device can run on for a given \( P_D \) and the other parameter is

\[ V_S, \text{max} = \frac{(P_D + V_O^2 / R_{\text{PAR}})}{2I_s + V_O / R_{\text{PAR}}} \]

The maximum dissipation a package support is

\[ P_D, \text{max} = \frac{(T_D, \text{max} - T_A, \text{max})}{R_{\text{TH}}} \]

Where \( T_D, \text{max} \) is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance
\( T_A, \text{max} \) is the ambient temperature, 70°C for commercial and 85°C for industrial range
\( R_{\text{TH}} \) is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The most difficult case is the SO-8 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 170°C/W gives a maximum dissipation of 382 mW. This allows a maximum supply voltage of ±9.2V for the EL4422 operated in our example. If the EL4421 were driving a light load (\( R_{\text{PAR}} \to \infty \)), it could operate on ±15V supplies at a 70°C maximum ambient.

The EL4441 through EL4444 can operate on ±12V supplies in the SO package, and all parts can be powered by ±15V supplies in DIP packages.

**Output Loading**

The output stage of the mux-amp is very powerful, and can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain or gain accuracy degrades only 10% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion only a bit, becoming noticeably worse for loads < 100Ω.
Applications Information — Contd.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

Input Connections

The input transistors can be driven from resistive and capacitive sources but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6" of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz.

Often simply placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the mux-amp input. If this is not possible, one can insert series resistors of around 510Ω to de-Q the inputs.

Feedback Connections

A feedback divider is used to increase circuit gain, and some precautions should be observed. The first is that parasitic capacitance at the -input will add phase lag to the feedback path and increase frequency response peaking or even cause oscillation. One solution is to choose feedback resistors whose parallel value is low. The pole frequency of the feedback network should be maintained above at least 200 MHz. For a 3 pF parasitic, this requires that the feedback divider have less than 265Ω impedance, equivalent to two 510Ω resistors when a gain of +2 is desired. Alternatively, a small capacitor across RF can be used to create more of a frequency-compensated divider. The value of the capacitor should match the parasitic capacitance at the -input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors will dominate parasitic effects and allow a higher divider resistance.

The other major concern about the divider concerns unselected-channel crosstalk. The differential input impedance of each input stage is around 200 KΩ. The unselected input's signal sources thus drive current through that input impedance into the feedback divider, inducing an unwanted output. The gain from unselected input to output, the crosstalk attenuation, if RF/RIN. In unity-gain connection the feedback resistor is 0Ω and very little crosstalk is induced. For a gain of +2, the crosstalk is about −60 dB.

Feedthrough Attenuation

The channels have different crosstalk levels with different inputs. Here is the typical attenuation for all combinations of inputs for the mux-amps at 3.58 MHz:

Feedthrough of EL4441 and EL4443 at 3.58 MHz

<table>
<thead>
<tr>
<th>Select Inputs, A1A0</th>
<th>In1</th>
<th>In2</th>
<th>In3</th>
<th>In4</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Selected</td>
<td>−77 dB</td>
<td>−90 dB</td>
<td>−92 dB</td>
</tr>
<tr>
<td>01</td>
<td>−80 dB</td>
<td>Selected</td>
<td>−77 dB</td>
<td>−90 dB</td>
</tr>
<tr>
<td>10</td>
<td>−101 dB</td>
<td>−76 dB</td>
<td>Selected</td>
<td>−66 dB</td>
</tr>
<tr>
<td>11</td>
<td>−96 dB</td>
<td>−84 dB</td>
<td>−66 dB</td>
<td>Selected</td>
</tr>
</tbody>
</table>

Feedthrough of EL4421 at 3.58 MHz

<table>
<thead>
<tr>
<th>Channel Select Input, A0</th>
<th>In1</th>
<th>In2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Selected</td>
<td>−88 dB</td>
</tr>
<tr>
<td>1</td>
<td>−93 dB</td>
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</tr>
</tbody>
</table>

Switching Glitches

The output of the mux-amps produces a small "glitch" voltage in response to a logic input change. A peak amplitude of only about 90 mV occurs, and the transient settles out in 20 ns. The glitch does not change amplitude with different gain settings.

With the four-input multiplexers, when two logic inputs are simultaneously changed, the glitch amplitude doubles. The increase can be avoided by keeping transitions at least 6 ns apart. This can be accomplished by inserting one gate delay in one of the two logic inputs when they are truly synchronous.
Features
- Complete four-quadrant multiplier with output amp—requires no extra components
- Good linearity of 0.3%
- 90 MHz bandwidth for both X and Y inputs
- Operates on ±5V to ±15V supplies
- All inputs are differential
- 400V/μs slew rate

Applications
- Modulation/Demodulation
- RMS computation
- Real-time power computation
- Nonlinearity correction/generation

General Description
The EL4450C is a complete four-quadrant multiplier circuit. It offers wide bandwidth and good linearity while including a powerful output voltage amplifier, drawing modest supply current.

The EL4450C operates on ±5V supplies and has an analog input range of ±2V, making it ideal for video signal processing. AC characteristics do not vary over the ±5V to ±15V supply range.

The multiplier has an operational temperature range of −40°C to +85°C and are packaged in plastic 14-pin P-DIP and SO.

Ordering Information
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
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</thead>
<tbody>
<tr>
<td>EL4450CN</td>
<td>−40°C to +85°C</td>
<td>14-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL4450CM</td>
<td>−40°C to +85°C</td>
<td>14-Lead SO</td>
<td>MDP0027</td>
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</table>

Connection Diagram
### Absolute Maximum Ratings \( (T_\text{A} = 25^\circ \text{C}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+</td>
<td>Positive Supply Voltage</td>
<td>16.5V</td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>V_\text{S}</td>
<td>V+ to V− Supply Voltage</td>
<td>33V</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_\text{IN}</td>
<td>Voltage at any Input or Feedback</td>
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<td></td>
<td></td>
<td>I</td>
<td></td>
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<tr>
<td>ΔV_\text{IN}</td>
<td>Difference between Pairs of Inputs</td>
<td>6V</td>
<td></td>
<td></td>
<td>I</td>
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</tr>
<tr>
<td>I_\text{IN}</td>
<td>Current into any Input or Feedback</td>
<td>4mA</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_\text{j} = T_\text{C} = T_\text{A} \).

### Open-Loop DC Electrical Characteristics \( (T_\text{A} = 25^\circ \text{C}, \text{V}_{\text{FB}} = \text{V}_{\text{OUT}}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_\text{DIFF}</td>
<td>Differential Input Voltage—Clipping 0.2% nonlinearity</td>
<td>1.8</td>
<td>2.0</td>
<td>1.0</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>V_\text{CM}</td>
<td>Common-Mode Range of ( V_\text{DIFF} = 0, V_\text{S} = \pm 5V )</td>
<td>( \pm 2.5 )</td>
<td>( \pm 2.8 )</td>
<td>( \pm 12.5 )</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>V_\text{OS}</td>
<td>Input Offset Voltage</td>
<td>8</td>
<td>35</td>
<td>I</td>
<td>V</td>
<td>mV</td>
</tr>
<tr>
<td>I_\text{B}</td>
<td>Input Bias Current</td>
<td>9</td>
<td>20</td>
<td>I</td>
<td>V</td>
<td>μA</td>
</tr>
<tr>
<td>I_\text{OS}</td>
<td>Output Offset Current between ( X_\text{IN}^+ ) and ( X_\text{IN}^- ), ( Y_\text{IN}^+ ) and ( Y_\text{IN}^- ), \text{REF and FB}</td>
<td>0.5</td>
<td>4</td>
<td>I</td>
<td>V</td>
<td>μA</td>
</tr>
<tr>
<td>Gain</td>
<td>Gain Factor of ( \text{V}<em>{\text{OUT}} = \text{Gain} \times X</em>\text{IN}^+ \times Y_\text{IN} )</td>
<td>0.45</td>
<td>0.5</td>
<td>0.55</td>
<td>I</td>
<td>V/V^2</td>
</tr>
<tr>
<td>NLx</td>
<td>Nonlinearity of X Input; ( X_\text{IN} ) between ( -1V ) and ( +1V )</td>
<td>0.3</td>
<td>0.7</td>
<td>I</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>NLy</td>
<td>Nonlinearity of Y Input; ( Y_\text{IN} ) between ( -1V ) and ( +1V )</td>
<td>0.2</td>
<td>0.35</td>
<td>I</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>R_\text{IN}</td>
<td>Input resistance, ( X_\text{IN}^+ ) to ( X_\text{IN}^- ), ( Y_\text{IN}^+ ) to ( Y_\text{IN}^- ), \text{REF to FB}</td>
<td>230</td>
<td>90</td>
<td>V</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio, ( X_\text{IN} ) and ( Y_\text{IN} )</td>
<td>70</td>
<td>90</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-Supply Rejection Ratio, FB</td>
<td>60</td>
<td>72</td>
<td>I</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>V_\text{O}</td>
<td>Output Voltage Swing ( (V_\text{IN} = 0, V_\text{REF Varied}) )</td>
<td>( \pm 2.5 )</td>
<td>( \pm 2.8 )</td>
<td>( \pm 12.5 )</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>I_\text{SC}</td>
<td>Output Short-Circuit Current</td>
<td>40</td>
<td>85</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_\text{S}</td>
<td>Supply Current, ( V_\text{S} = \pm 15V )</td>
<td>15.4</td>
<td>18</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
EL4450C
Wideband Four-Quadrant Multiplier

Closed-Loop AC Electrical Characteristics
Power Supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15pF

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW, −3 dB</td>
<td>−3 dB Small-Signal Bandwidth, X or Y</td>
<td>90</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>BW, ±0.1 dB</td>
<td>0.1 dB Flatness Bandwidth</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>Peaking</td>
<td>Frequency Response Peaking</td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate, V_OUT between −2V and +2V</td>
<td>300</td>
<td>400</td>
<td></td>
<td>I</td>
<td>V/µs</td>
</tr>
<tr>
<td>V_N</td>
<td>Input-Referred Noise Voltage Density</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
<td>nV/Hz</td>
</tr>
</tbody>
</table>

Test Circuit

Note: For typical performance curves, R_F = 0, R_G = ∞, V_S = ±5V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.

Typical Performance Curves

Transfer Function of X Input for Various Y Inputs

Transfer Function of Y Input for Various X Inputs

3-172
Typical Performance Curves — Contd.

**Frequency Response for Various Feedback Divider Ratios**

- \( V_{OUT} = X \times Y \)  
- \( \text{RATIO} = 1 \)  
- \( \text{RATIO} = 1/2 \)  
- \( \text{RATIO} = 1/5 \)  
- \( \text{RATIO} = 1/10 \)  
- \( V_S = \pm 5V \)  
- \( R_L = 500\Omega \)  
- \( C_L = 15pF \)

**Frequency Response for Various R_L, C_L**

- \( V_S = \pm 5V \)  
- \( R_L = 500\Omega, C_L = 30pF \)  
- \( R_L = 150\Omega, C_L = 30pF \)  
- \( R_L = 500\Omega, C_L = 18pF \)  
- \( R_L = 150\Omega, C_L = 18pF \)  
- \( R_L = 500\Omega, C_L = 8pF \)  
- \( R_L = 150\Omega, C_L = 8pF \)

**X Input Frequency Response for Various Y DC Inputs**

- \( V_S = \pm 5V \)  
- \( R_L = 500\Omega \)  
- \( C_L = 15pF \)

**Y Input Frequency Response for Various X DC Inputs**

- \( V_S = \pm 5V \)  
- \( R_L = 500\Omega \)  
- \( C_L = 15pF \)

**3 dB Bandwidth and Peaking vs Supply Voltage**

- \( V_S = \pm 5V \)  
- \( R_L = 500\Omega \)  
- \( C_L = 15pF \)

**Total Harmonic Distortion of X Input vs Frequency**

- \( Y \text{ INPUT} = 1 \text{VDC} \)  
- \( X \text{ AMPLITUDE} = 1 \text{VRMS} \)  
- \( X \text{ AMPLITUDE} = 300 \text{mVRMS} \)  
- \( X \text{ AMPLITUDE} = 100 \text{mVRMS} \)

**Total Harmonic Distortion of Y Input vs Frequency**

- \( X \text{ INPUT} = 1 \text{VDC} \)  
- \( Y \text{ AMPLITUDE} = 1 \text{VRMS} \)  
- \( Y \text{ AMPLITUDE} = 300 \text{mVRMS} \)  
- \( Y \text{ AMPLITUDE} = 100 \text{mVRMS} \)
Typical Performance Curves — Contd.

Slew Rate vs Supply Voltage

Slew Rate vs Die Temperature

CMRR vs Frequency

Input Voltage Noise vs Frequency

Nonlinearity of X Input

Nonlinearity of Y Input

Bias Current vs Die Temperature

Common-Mode Input Range vs Supply Voltage
Typical Performance Curves — Contd.

Supply Current vs Die Temperature

Supply Current vs Supply Voltage

14-Pin Package Power Dissipation vs Ambient Temperature
Applications Information

The EL4450 is a complete four-quadrant multiplier with 90 MHz bandwidth. It has three sets of inputs; a differential multiplying X-input, a differential multiplying Y-input, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:

The gain of the feedback divider is \( H \), and \( H = \frac{R_G}{(R_G + R_F)} \). The transfer function of the part is

\[
V_{OUT} = A_0 \times \left( \frac{1}{2} \times ((V_{INX} - V_{INX^-}) \times ((V_{INY} + V_{INY^-})) + (V_{REF} - V_{FB})) \right)
\]

\( V_{FB} \) is connected to \( V_{OUT} \) through a feedback network, so \( V_{FB} = H \times V_{OUT} \). \( A_0 \) is the open-loop gain of the amplifier, and is about 600. The large value of \( A_0 \) drives

\[
\left( \frac{1}{2} \times ((V_{INX} - V_{INX^-}) \times ((V_{INY} + V_{INY^-})) + (V_{REF} - V_{FB}) \right) \rightarrow 0.
\]

Rearranging and substituting for \( V_{REF} \)

\[
V_{OUT} = \left( \frac{1}{2} \times ((V_{INX} + V_{INX^-}) \times ((V_{INY} + V_{INY^-})) + (V_{REF}) \right) / H, \text{ or}
\]

Thus the output is equal to one-half the product of \( X \) and \( Y \) inputs and offset by \( V_{REF} \), all gained up by the feedback divider ratio. The EL4450 is stable for a direct connection between \( V_{OUT} \) and \( FB \), and the feedback divider may be used for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360\( \Omega \) or less. Alternatively, a small capacitor across \( R_F \) can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a maximum gain of 1 will dominate parasitic effects and allow a higher divider resistance.

The \( REF \) pin can be used as the output's ground reference, or for DC offsetting of the output, or it can be used to sum in another signal.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6" of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around to 51\( \Omega \) to de-Q the inputs.
Signal Amplitudes
Signal input common-mode voltage must be between (V−) + 2.5V and (V+) − 2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ± 6V to prevent damage. The differential signal range is ± 2V in the EL4450C. The input range is substantially constant with temperature.

The Ground Pin
The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−) + 2.5V and (V+) − 3.5V. The ground pin is connected to the IC’s substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies
The EL4450C works well on supplies from ± 3V to ± 15V. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as low as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4450C increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

\[ P_D = 2I_{S,\text{max}}V_S + (V_S - V_O)V_O/R_{\text{PAR}} \]

where

- \( I_{S,\text{max}} \) is the maximum supply current
- \( V_S \) is the ± supply voltage (assumed equal)
- \( V_O \) is the output voltage
- \( R_{\text{PAR}} \) is the parallel of all resistors loading the output

For instance, the EL4450C draws a maximum of 18 mA. With light loading, \( R_{\text{PAR}} \rightarrow \infty \) and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given \( P_D \) and the other parameters is

\[ V_{S,\text{max}} = \frac{(P_D + V_O^2/R_{\text{PAR}})/(2I_S + V_O/R_{\text{PAR}})}{V_S} \]

The maximum dissipation a package can offer is

\[ P_{D,\text{max}} = (T_{J,\text{max}} - T_{A,\text{max}})/\theta_{JA} \]

Where \( T_J,\text{max} \) is the maximum junction temperature, 150°C for reliability, less to retain optimum electrical performance

\( T_A,\text{max} \) is the ambient temperature, 70°C for commercial and 85°C for industrial range

\( \theta_{JA} \) is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum junction temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded significantly.

Output Loading
The output stage is very powerful. It typically can source 85 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain accuracy degrades only 0.2% from no load- to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads < 100Ω.

Capacitive loads will cause peaking in the frequency response. If a capacitive load must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.
Mixer Applications
Because of its lower distortion levels, the Y input is the better choice for a mixer's signal port. The X input would receive oscillator amplitudes of about 1V RMS maximum. Carrier suppression is initially limited by the offset voltage of the Y input, 20 mV maximum, and is about 37 dB worst-case. Better suppression can be obtained by nulling the offset of the X input. Similarly, nulling the offset of the Y input will improve signal-port suppression. Driving an input differentially will also maximize feedthrough suppression at frequencies beyond 10 MHz.

AC Level Detectors
Square-law converters are commonly used to convert AC signals to DC voltages corresponding to the original amplitude in subsystems like automatic gain controls (AGC's) and amplitude-stabilized oscillators. Due to the controlled AC amplitudes, the inputs of the multiplier will see a relatively constant signal level. Best performance will be obtained for inputs between 200 mVRMS and 1 VRMS. The traditional use of the EL4450C as an AGC detector and control loop would be:

Traditional AGC Detector/DC Feedback Circuit
AC Level Detectors — Contd.
The EL4450C simply provides an output equal to the square of the input signal and an integrator filters out the AC component, while comparing the DC component to an amplitude reference. The integrator output is the DC control voltage to the variable-gain sections of the AGC (not shown). If a negative polarity of reference is required, one of the multiplier input terminal pairs is reversed, inverting the multiplier output. Input bias current will cause input voltage offsets due to source impedances; putting a compensating resistor in series with the grounded inputs of the EL4450C will reduce this offset greatly.

This control system will attempt to force

\[ V_{\text{IN,RMS}}^2 / 4 = V_{\text{REF}}. \]

The extra op-amp can be eliminated by using this circuit:

![Simplified AGC Detector/DC Feedback Circuit](image-url)
AC Level Detectors — Contd.

Here the internal op-amp of the EL4450C replaces the external amplifier. The feedback capacitor \( C_F \) does not provide a perfect integration action; a zero occurs at a frequency of \( 1/2\pi R_C F \). This is canceled by including another \( R_C F \) pair at the AGC control output. If the reference voltage must be negative, the resistor at pin 11 is connected to ground rather than the reference and pin 10 connected to the reference.

The amplitude reference will have to support some AC currents flowing through \( R \). If this is a problem, several changes can be made to eliminate it. The reference is connected to pin 10 and the resistor \( R \) connected to pin 11 reconnected to ground, and one of the multiplier input connections are reversed.

Square-law detectors have a restricted input range, about 10:1, because the output rapidly disappears into the DC errors as signal amplitudes reduce. This circuit gives a multiplier output that is the absolute value of the input, thus increasing range to 100:1:

![Absolute-Value Input Circuitry](image)

**Absolute-Value Input Circuitry**
AC Level Detectors — Cont’d.
An ECL comparator produces an output corresponding to the sign of the input, which when multiplied by the input produces an effective absolute-value function. The RC product connected to the X inputs simply emulates the time delay of the comparator to maintain circuit accuracy at higher frequencies.

Nonlinear Function Generation
The REF pin of the EL4450C can be used to sum in various quantities of polynomial function generators. For instance, this sum of REF allows a linear signal path which can have various amounts of squared signal added:

![Polynomial Function Generator](image)

The polarity of the squared signal can be reversed by swapping one of the X or Y input pairs.

The REF and FB pins also simplify feedback schemes that allow square-rooting:

![Square-Rooter](image)

The diode and $I_{\text{pulldown}}$ assure that the output will always produce the positive square-root of the input signal. $I_{\text{pulldown}}$ should be large enough to assure that the diode be forward-biased for any load current. In this configuration, the bandwidth of the circuit will reduce for smaller input signals.
Nonlinear Function Generation — Contd.

The REF and FB terminals can also be used to implement division:

The output frequency response reduces for smaller values of $V_X$, but is not affected by $V_{REF}$.
Features
- Complete two-input fader with output amplifier—uses no extra components
- 80 MHz bandwidth
- Fast fade control speed
- Operates on ±5V to ±15V supplies
- >60 dB attenuation @ 5 MHz

Applications
- Mixing two inputs
- Picture-in-picture
- Text overlay onto video
- General gain control

General Description
The EL4453C is a complete fader subsystem. It variably blends two inputs together for such applications as video picture-in-picture effects.

The EL4453C operates on ±5V to ±15V supplies and has an analog differential input range of ±2V. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of -40°C to +85°C and is packaged in 14-pin P-DIP and SO-14.

The EL4453C is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is free from latch up.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>ELA453CN</td>
<td>-40°C to +85°C</td>
<td>14-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>ELA453CS</td>
<td>-40°C to +85°C</td>
<td>14-Lead SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagram
Absolute Maximum Ratings $T_A = 25^\circ C$

| Parameter                  | Value
|----------------------------|-------
| $V_+$ Positive Supply Voltage | 16.5V |
| $V_S$ V+ to V- Supply Voltage | 33V   |
| $V_{IN}$ Voltage at any Input or Feedback | V+ to V- |
| $\Delta V_{IN}$ Difference between Pairs of Inputs or Feedback | 6V |

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_{J} = T_{C} = T_{A}$.

Test Procedure
- I: 100% production tested and QA sample tested per QA test plan QCX0002.
- II: 100% production tested at $T_A = 25^\circ C$ and QA sample tested at $T_A = 25^\circ C$,
- $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.
- III: QA sample tested per QA test plan QCX0002.
- IV: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- V: Parameter is typical value at $T_A = 25^\circ C$ for information purposes only.

Open-Loop DC Electrical Characteristics
Power Supplies at $\pm 5V$, Sum+ = Sum- = 0, $T_A = 25^\circ C$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DIFF}$</td>
<td>$V_{INA}$, $V_{INB}$, or Sum Differential Input Voltage—</td>
<td>1.8</td>
<td>2.0</td>
<td>0.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.2% Nonlinearity</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Common-Mode Range (All Inputs; $V_{DIFF} = 0$)</td>
<td>$V_S = \pm 5V$</td>
<td>$\pm 2.5$</td>
<td>$\pm 2.8$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V$</td>
<td>$\pm 12.5$</td>
<td>$\pm 12.8$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>A or B Input Offset Voltage</td>
<td>25</td>
<td></td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{FADE}$ 100%</td>
<td>Extrapolated Voltage for 100% Gain for $V_{INA}$</td>
<td>0.9</td>
<td>1.05</td>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FADE}$ 0%</td>
<td>Extrapolated Voltage for 0% Gain for $V_{INA}$</td>
<td>$-1.2$</td>
<td>$-1.15$</td>
<td>$-0.9$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current (All Inputs) with all $V_{IN} = 0$</td>
<td>9</td>
<td>20</td>
<td></td>
<td>I</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current between $V_{INA}^+$ and $V_{INA}^-$, $V_{INB}^+$ and $V_{INB}^-$, Fade+ and Fade−, and Sum+ and Sum−</td>
<td>0.2</td>
<td>4</td>
<td></td>
<td>I</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$F_T$</td>
<td>$V_{INA}$ Signal Feedthrough, $V_{FADE} = -1.5V$</td>
<td>$-100$</td>
<td>$-60$</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>$N_L$</td>
<td>A or B Input Nonlinearity, $V_{IN}$ between $+1V$ and $-1V$, $V_{INA}$ or $V_{INB}$</td>
<td>0.2</td>
<td>0.5</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Sum Input</td>
<td>0.5</td>
<td></td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>$R_{IN}$, Signal</td>
<td>Input Resistance, A, B, or Sum Input</td>
<td>230</td>
<td></td>
<td></td>
<td>V</td>
<td>k\Omega</td>
</tr>
<tr>
<td>$R_{IN}$, Fade</td>
<td>Input Resistance, Fade Input</td>
<td>120</td>
<td></td>
<td></td>
<td>V</td>
<td>k\Omega</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common-Mode Rejection Ratio, $V_{INA}$ or $V_{INB}$</td>
<td>70</td>
<td>80</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
<td>50</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>$E_G$</td>
<td>Gain Error, $V_{FADE} = 1.5V$, $V_{INA}$ or $V_{INB}$</td>
<td>$-2$</td>
<td>+2</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Sum Input</td>
<td>$-4$</td>
<td>+4</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>$V_O$</td>
<td>Output Voltage Swing ($V_{IN} = 0$, $V_{REF}$ Varied)</td>
<td>$V_S = \pm 5V$</td>
<td>$\pm 2.5$</td>
<td>$\pm 2.8$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = \pm 15V$</td>
<td>$\pm 12.5$</td>
<td>$\pm 12.8$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Output Short-Circuit Current</td>
<td>40</td>
<td>85</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current, $V_S = \pm 15V$</td>
<td>17</td>
<td>21</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
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### Closed-Loop AC Electrical Characteristics

Power supplies at \( \pm 12V, T_A = 25°C, R_L = 500Ω, C_L = 15 \text{ pF}, V_{FADE} = 1.5V, \text{Sum}^+ = \text{Sum}^- = 0 \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW, (-3) dB</td>
<td>(-3) dB Small-Signal Bandwidth, (V_{IN A}) or (V_{IN B})</td>
<td>80</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW, (\pm 0.1) dB</td>
<td>(0.1) dB Flatness Bandwidth, (V_{IN A}) or (V_{IN B})</td>
<td>9</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peaking</td>
<td>Frequency Response Peaking</td>
<td>1.0</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW, Fade</td>
<td>(-3) dB Small-Signal Bandwidth, Fade Input</td>
<td>80</td>
<td>V</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate, (V_{OUT}) between (-2V) and (+2V)</td>
<td>TBD</td>
<td>I</td>
<td>V/(\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_N)</td>
<td>Input-Referred Noise Voltage Density</td>
<td>160</td>
<td>V</td>
<td>nV/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(F_T)</td>
<td>Feedthrough of Faded-Out Channel, (F = 3.58\ MHz)</td>
<td>(-63)</td>
<td>V</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(dG)</td>
<td>Differential Gain Error, (V_{OFFSET}) from 0 to (\pm 0.714V), Fade at 100% (V_{IN A}) or (V_{IN B}) Sum Input</td>
<td>0.05</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(d\theta)</td>
<td>Differential Phase Error, (V_{OFFSET}) from 0 to (\pm 0.71V), Fade at 100% (V_{IN A}) or (V_{IN B}) Sum Input</td>
<td>0.1</td>
<td>V</td>
<td>(*)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Test Circuit

![Test Circuit Diagram](image)

Note: For typical performance curves \(\text{Sum}^+ = \text{Sum}^- = 0\), \(R_P = 0Ω\), \(R_G = \infty\), \(V_{FADE} = +1.5V\), and \(C_L = 15\ \text{pF}\), unless otherwise noted.
Typical Performance Curves

**Frequency Response**

- $V_o = \pm 5V$, $V_{in}A$ or $V_{in}B$
- $V_S = \pm 15V$, $V_{in}A$ or $V_{in}B$

**Frequency Response vs Gain**

- $A_v = 1$
- $A_v = 2$
- $A_v = 4$
- $A_v = 10$

- $V_o = \pm 5V$

**Frequency Response for Various Loads, $V_S = \pm 5V$**

- $A_v = 1$
- $R_L = 500\Omega$, $C = 36\, \text{pF}$
- $R_L = 150\Omega$, $C = 36\, \text{pF}$
- $R_L = 500\Omega$, $C = 23\, \text{pF}$

- $V_S = \pm 15V$

**-3 dB Bandwidth and Peaking**

- $V_o = \pm 5V$

**-3 dB Bandwidth and Peaking vs Supply Voltage**

- $F = 3\, \text{dB}$

**-3 dB Bandwidth and Peaking vs Die Temperature**

- $BANDWIDTH, V_S = \pm 15V$
- $PEAKING, V_S = \pm 15V$
Typical Performance Curves — Contd.

Frequency Response for Different Gains, $V_S = \pm 5V$

Input Common-Mode Rejection Ratio vs Frequency

Input Voltage and Current Noise vs Frequency

$V_{IN}$ Differential Gain and Phase Error vs Gain

$V_{IN}$ Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. $V_S = \pm 5V$

$V_{IN}$ Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. $V_S = \pm 12V$
Typical Performance Curves — Contd.

Nonlinearity vs $V_{IN}$ Signal Span

Nonlinearity vs Sum Signal Span

Slew Rate vs Supply Voltage

Slew Rate vs Die Temperature

$V_{IN}$A Gain vs $V_{FADE}$

Frequency Response of Fade Input
Typical Performance Curves — Contd.

**Transient Response of Fade Input**
Constant Signal into $V_{INA}$

- $V_{FADE}$
- $V_{OUT}$

**Overdrive Recovery Glitch from $V_{FADE}$, No Input Signal**

- Overdriven $V_{FADE}$
- $V_{OUT}$ at 20 mV/cm

**$V_{INA}$ Transient Response for Various Gains**

- Zero gain
- 25% gain
- 50% gain
- 100% gain

**Cross-Fade Balance with $V_{INA} = V_{INB} = 0$**

- $V_{FADE}$
- $V_{OUT}$ at 5mV/cm

**Supply Current vs Supply Voltage**

- $T_A = 25^\circ C$
- Die Temperature = 150$^\circ C$

**Supply Current vs Die Temperature**

- $V_S = \pm 15V$
- $V_S = \pm 5V$
Applications Information

The EL4453C is a complete two-quadrant fader/gain control with 80 MHz bandwidth. It has four sets of inputs; a differential signal input $V_{\text{INA}}$, a differential signal input $V_{\text{INB}}$, a differential fade-controlling input $V_{\text{FADE}}$, and another differential input Sum which can be used to add in a third input at full gain. This is the general connection of the EL4453C:
Applications Information — Contd.
The gain of the feedback dividers are $H_A$ and $H_B$, and $0 \leq H \leq 1$. The transfer function of the part is

$$V_{OUT} = A_0 \times \left[ \left( (V_{INA}) - H_A \times V_{OUT} \right) \times \frac{(1 + \left( V_{FADE}^+ \right) - \left( V_{FADE}^- \right))/2 + (V_{INB}) - H_B \times V_{OUT} \times (1 - \left( V_{FADE}^+ \right) + \left( V_{FADE}^- \right))/2 + (\text{Sum} +) - (\text{Sum} -)) \right],$$

with $-1 \leq \left( V_{FADE}^+ \right) - \left( V_{FADE}^- \right) \leq +1$ numerically.

$A_0$ is the open-loop gain of the amplifier, and is about 600. The large value of $A_0$ drives

$$\left( (V_{INA}) - H_A \times V_{OUT} \right) \times \frac{(1 + \left( V_{FADE}^+ \right) - \left( V_{FADE}^- \right))/2 + (V_{INB}) - H_B \times V_{OUT} \times (1 - \left( V_{FADE}^+ \right) + \left( V_{FADE}^- \right))/2 + (\text{Sum} +) - (\text{Sum} -)) \rightarrow 0.$$

Rearranging and substituting

$$V_{OUT} = \frac{F \times V_{INA} + \bar{F} \times V_{INB} + \text{Sum}}{F \times H_A + \bar{F} \times H_B}$$

Where $F = \left(1 + \left( V_{FADE}^+ \right) - \left( V_{FADE}^- \right)/2, \bar{F}=\left(1-(V_{FADE}^+)+ (V_{FADE}^-))/2, and \text{Sum} = (\text{Sum} +) - (\text{Sum} -)$

In the above equations, $F$ represents the fade amount, with $F = 1$ giving 100% gain on $V_{INA}$ but 0% for $V_{INB}$; $\bar{F} = 0$ giving 0% gain for $V_{INA}$ but 100% to $V_{INB}$. $\bar{F}$ is $1 - F$, the complement of the fade gain. When $F = 1$,

$$V_{OUT} = \frac{V_{INA} + \text{Sum}}{H_A}$$

and the amplifier passes $V_{INA}$ and $\text{Sum}$ with a gain of $1/H_A$. Similarly, for $F = 0$

$$V_{OUT} = \frac{V_{INB} + \text{Sum}}{H_B}$$

and the gains vary linearly between fade extremes.

The EL4453C is stable for a direct connection between $V_{OUT}$ and $V_{INA}$ or $V_{INB}$, yielding a gain of $+1$. The feedback divider may be used for higher output gain, although with the traditional loss of bandwidth. It is important to keep the feedback dividers' impedances low so that stray capacitance does not diminish the feedback loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least $150 \text{MHz}$; typical strays of 3 pF thus require a feedback impedance of $360 \Omega$ or less. Alternatively, a small capacitor across $R_F$ can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a gain of two will dominate parasitic effects and allow a higher divider resistance. Either input channel can be set up for inverting gain using traditional feedback resistor connections.

At 100% gain, an input stage operates just like an op-amp's input, and the gain error is very low, around $-0.2\%$. Furthermore, nonlinearities are vastly improved since the gain core sees only small error signals, not full inputs. Unfortunately, distortions increase at lower fade gains for a given input channel.

The Sum pins can be used to inject an additional input signal, but it is not as linear as the $V_{IN}$ paths. The gain error is also not as good as the main inputs, being about 1%. Both sum pins should be grounded if they are not to be used.
Fade-Control Characteristics

The quantity \( V_{\text{FADE}} \) in the above equations is bounded as \(-1 \leq V_{\text{FADE}} \leq 1\), even though the externally applied voltages often exceed this range. Actually, the gain transfer function around \(-1\) V and \(+1\) V is “soft,” that is, the gain does not clip abruptly below the 0%-\( V_{\text{FADE}} \) voltage or above the 100%-\( V_{\text{FADE}} \) level. An overdrive of 0.3V must be applied to \( V_{\text{FADE}} \) to obtain truly 0% or 100%. Because the 0% = or 100%-\( V_{\text{FADE}} \) levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied \( V_{\text{FADE}} \) range of \(-1.5\) V to \(+1.5\) V will assure the full span of numerical \(-1 \leq V_{\text{FADE}} \leq 1\) and \(0 \leq F \leq 1\).

The fade control has a small-signal bandwidth equal to the \( V_{\text{IN}} \) channel bandwidth, and overload recovery resolves in about 20 ns.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about six inches of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high frequency construction obviates any such problems, where the input source is reasonably close to the fader input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between \((V-) + 2.5\) V and \((V+) - 2.5\) V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to \(\pm 6\) V to prevent damage. The differential signal range is \(\pm 2\) V in the EL4453C. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 \( \mu \)A maximum DC current, and may be biased anywhere between \((V-) + 2.5\) V and \((V+) - 3.5\) V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and channel-to-channel isolation over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4453C works well on any supplies from \(\pm 3\) V to \(\pm 15\) V. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 \( \mu \)F tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 \( \mu \)F can be used if small load currents flow.

Singe-polarity supplies, such as \(+12\) V with \(+5\) V can be used, where the ground pin is connected to \(+5\) V and \(V-\) to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the fader increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

\[
P_D = 2 \times V_S, \text{max} \times V_S + (V_S - V_O) \times V_O/R_{\text{PAR}}
\]

where \( I_{S, \text{max}} \) is the maximum supply current
\( V_S \) is the \(\pm\) supply voltage (assumed equal)
\( V_O \) is the output voltage
\( R_{\text{PAR}} \) is the parallel of all resistors loading the output
Power Supplies — Contd.

For instance, the EL4453C draws a maximum of 21 mA. With light loading, $R_{PAR} \to \infty$ and the dissipation with $\pm 5\text{V}$ supplies is 210 mW. The maximum supply voltage that the device can run on for a given $P_D$ and the other parameters is

$$V_S, \text{ max} = \frac{(P_D + V_O^2/R_{PAR})}{(2I_S + V_O/R_{PAR})}$$

The maximum dissipation a package can offer is

$$P_D, \text{ max} = \frac{(T_D, \text{ max} - T_A, \text{ max})}{\theta_{JA}}$$

where $T_D, \text{ max}$ is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

$T_A, \text{ max}$ is the ambient temperature, 70°C for commercial and 85°C for industrial range

$\theta_{JA}$ is the thermal resistance of the mounted package, obtained from datasheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 70°C, the 80°C temperature rise and package thermal resistance of 110°/W gives a dissipation of 636 mW at 85°C. This allows $\pm 15\text{V}$ operation over the commercial temperature range, but higher ambient temperature or output loading may require lower supply voltages.

Output Loading

The output stage of the EL4453C is very powerful. It typically can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads $< 100\Omega$.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.
Features

- NTSC, PAL and SECAM sync separation
- Single supply, +5V
- Precision 50% slicing, internal caps
- Built-in color burst filter
- Decodes non-standard verticals
- Pin compatible with LM1881
- Low power
- Typically 1.5 mA supply current
- Resistor programmable scan rate
- Few external components
- Available in 8-pin DIP and SO-8 pkg.

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline#</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4581CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL4581CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Demo Board

A dedicated demo board is not available. However, this device can be placed on the EL4584/5 Demo Board.

General Description

The EL4581C extracts timing information from standard negative going video sync found in NTSC, PAL, and SECAM broadcast systems. It can also be used in non standard formats and with computer graphics systems at higher scan rates, by adjusting a single external resistor. When the input does not have correct serration pulses in the vertical interval, a default vertical output is produced.

Outputs are composite sync, vertical sync, burst/back porch output, and odd/even output. The later operates only in interlaced scan formats.

The EL4581C provides a reliable method of determining correct sync slide level by setting it to the mid-point between sync tip and blanking level at the back porch. This 50% level is determined by two internal self timing sample and hold circuits that track sync tip and back porch levels. This also provides a degree of hum and noise rejection to the input signal, and compensates for varying input levels of 0.5 p-p to 2.0 Vp-p.

A built in linear phase, third order, low pass filter attenuates the chroma signal in color systems to prevent incorrectly set color burst from disturbing the 50% sync slide.

This device may be used to replace the industry standard LM1881, offering improved performance and reduced power consumption.

The EL4581C video sync separator is manufactured using Elantec's high performance analog CMOS process.

Connection Diagram

[Connection Diagram Image]

Manufactured under U.S. Patent No. 5,528,303
Absolute Maximum Ratings \( T_A = 25°C \)

- **\( V_{CC} \) Supply**
  - 7V
  - Pin Voltages: \(-0.5\, \text{V} \) to \( V_{CC} + 0.5\, \text{V} \)
- **Storage Temperature**
  - \(-65°C \) to \(+150°C \)
- **Operating Temperature Range**
  - \(-40°C \) to \(+85°C \)
- **Lead Temperature**
  - 260°C

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

**Test Level**

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at ( T_A = 25°C ) and QA sample tested at ( T_A = 25°C ), ( T_{\text{MAX}} ) and ( T_{\text{MIN}} ) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at ( T_A = 25°C ) for information purposes only.</td>
</tr>
</tbody>
</table>

**DC Electrical Characteristics**

Unless otherwise state \( V_{DD} = 5V, T_A = 25°C, R_{\text{set}} = 680\, \text{k}Ω \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{DD} )</td>
<td>( V_{DD} = 5V ) (Note 1)</td>
<td>25°C</td>
<td>0.75</td>
<td>1.7</td>
<td>3</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Clamp Voltage</td>
<td>Pin 2, Unloaded</td>
<td>25°C</td>
<td>1.3</td>
<td>1.5</td>
<td>1.9</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Discharge Current</td>
<td>Pin 2 = 2V</td>
<td>25°C</td>
<td>6</td>
<td>10</td>
<td>20</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>Clamp Charge Current</td>
<td>Pin 2, ( V_{IN} = 1V )</td>
<td>25°C</td>
<td>2</td>
<td>3</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Ref Voltage</td>
<td>Pin 6, ( V_{DD} = 5V ) (Note 2)</td>
<td>25°C</td>
<td>1.5</td>
<td>1.8</td>
<td>2.1</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} ) Output Low Voltage</td>
<td>( I_{OL} = 1.6, mA )</td>
<td>25°C</td>
<td></td>
<td>800</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OH} ) Output High Voltage</td>
<td>( I_{OH} = -40, μA )</td>
<td>25°C</td>
<td>4</td>
<td></td>
<td></td>
<td>IV</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( I_{OH} = -1.6, mA )</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** No video signal, outputs unloaded.

**Note 2:** Tested for \( V_{DD} \, 5V \pm 5\% \) which guarantees timing of output pulses over this range.
Dynamic Characteristics

$V_{DD} = 5V, I_V \text{ pk-pk video, } T_A = 25^\circ C, C_L = 15 \, \text{pF}, I_{OH} = -1.6 \, \text{mA, } I_{OL} = 1.6 \, \text{mA. Signal voltages are peak to peak.}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertical Sync Width, $t_{VS}$</td>
<td>(Note 3)</td>
<td>25$^\circ$C</td>
<td>190</td>
<td>230</td>
<td>300</td>
<td>I</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Burst/Back Porch Width, $t_B$</td>
<td>(Note 3)</td>
<td>25$^\circ$C</td>
<td>2.5</td>
<td>3.5</td>
<td>4.5</td>
<td>I</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Vertical Sync Default Delay $t_{VSD}$</td>
<td></td>
<td>25$^\circ$C</td>
<td>40</td>
<td>55</td>
<td>70</td>
<td>I</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Filter Attenuation</td>
<td>$F_{IN} = 3.4 , \text{MHz}$ (Note 4)</td>
<td>25$^\circ$C</td>
<td>24</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>Composite Sync Prop Delay</td>
<td>$V_{IN} - \text{ Composite Sync}$ (Note 3)</td>
<td>25$^\circ$C</td>
<td>260</td>
<td>400</td>
<td></td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>Input Dynamic Range</td>
<td>$p-p , \text{NTSC Signal}$ (Note 5)</td>
<td>25$^\circ$C</td>
<td>0.5</td>
<td>2</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Slice Level</td>
<td>Input Voltage = $1V_{P-P}$ (Note 6)</td>
<td>25$^\circ$C</td>
<td>40%</td>
<td>50%</td>
<td>60%</td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>

Note 3: C/S, Vertical and Burst outputs are all active low – $V_{OH} = 2.4V$, $V_{OL} = 0.8V$.
Note 4: Attenuation is a function of Rset (PIN6).
Note 5: Typical min. is 0.3 $V_{P-P}$.
Note 6: Refers to threshold level of sync. tip to back porch amplitude.

Pin Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Composite Sync Out</td>
<td>Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.</td>
</tr>
<tr>
<td>2</td>
<td>Composite Video in</td>
<td>AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).</td>
</tr>
<tr>
<td>3</td>
<td>Vertical Sync Out</td>
<td>Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Supply ground.</td>
</tr>
<tr>
<td>5</td>
<td>Burst/Back Porch Output</td>
<td>Burst/Back porch output. Low during burst portion of composite video.</td>
</tr>
<tr>
<td>6</td>
<td>$R_{SET}$</td>
<td>An external resistor to ground sets all internal timing. 681k, 1% resistor will provide correct timing for NTSC signals.</td>
</tr>
<tr>
<td>7</td>
<td>Odd/Even Output</td>
<td>Odd/Even field output. Low during odd fields, high during even fields. Transitions occur at start of Vert Sync pulse.</td>
</tr>
<tr>
<td>8</td>
<td>$V_{DD} , 5V$</td>
<td>Positive supply. (5V)</td>
</tr>
</tbody>
</table>

Note: $R_{SET}$ must be a 1% resistor.
Typical Performance Characteristics

- **RSET vs Horizontal Frequency**
- **Back Porch Clamp On Time vs RSET**
- **Vertical Pulse Width vs RSET**
- **Vertical Default Delay Time vs RSET**
- **Vertical Pulse Width vs Temperature**
- **Supply Current vs Temperature**

Input Signal = 300 mVp-p

EL4581 Filter Characteristic
Constant Delay 240 ns
Timing Diagrams

SIGNAL 1a. COMPOSITE VIDEO INPUT, FIELD ONE

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.
d. Odd-even output is low for even field, and high for odd field.
e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).
Figure 2

SIGNAL 2a. COMPOSITE VIDEO INPUT

SIGNAL 2b. COMPOSITE SYNC. OUTPUT

SIGNAL 2c. VERTICAL SYNC. OUTPUT

SIGNAL 2d. ODD - EVEN OUTPUT

SIGNAL 2e. BURST/BACK PORCH OUTPUT

Figure 3

SIGNAL 3a. COMPOSITE VIDEO INPUT

SIGNAL 3b. VERTICAL SYNC. OUTPUT

(No Vertical Sync Pulses)

Vert Sync Default Delay
Figure 4. Standard (NTSC Input) H. Sync Detail
Description of Operation
A simplified block schematic is shown in Figure 2. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC coupled to pin 2 via the capacitor $C_1$, nominally 0.1 pF. The clamp circuit $A_1$ will prevent the input signal on pin 2 going any more negative than 1.5V, the value of reference voltage $V_{R1}$. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source $I_1$, nominally 10 µA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 µs for a 15.75 kHz timebase. From $I \cdot t = C \cdot V$, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of $\times 12.5$). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with $C_1$ will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be $V_{DD}$ less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450kΩ. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source $I_1$ directly tracks reference current $I_{TR}$ and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter ($F_1$) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. Note that the filter cut-off frequency is a function of $RSET$ through $I_{OT}$ and is proportional to $I_{OT}$.

Internal reference voltages (block $V_{REF}$) with high immunity to supply voltage variation are derived on the chip. Reference $V_{R4}$ with op-amp $A_2$ forces pin 6 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance $RSET$ will determine the value of the reference current $I_{TR}$. The internal resistance $R_3$ is only about 6 kΩ, much less than $RSET$. All the internal timing functions on the chip are referenced to $I_{TR}$ and have excellent supply voltage rejection.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync. pulse with a threshold voltage $V_{R2}$ which is referenced at a fixed level above the clamp voltage $V_{R1}$. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 µs to enable the actual sample of 2 µs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors.

The 50% level of the sync tip is derived, through the resistor divider $R_1$ and $R_2$, from the sample and held voltages $V_{TIP}$ and $V_{BP}$, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S output buffer $B_1$ and the other internal circuit blocks, the vertical, back porch and odd/even functions.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer
Description of Operation — Contd.

vertical sync. pulse widths. The internal timing circuits are referenced to $I_{OT}$ and $V_{R3}$, the timeout period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absence of a serration pulse, an internal timer will default the start of vertical.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of $I_{OT}$ and will therefore track the scan rate set by $RSET$.

The odd/even circuit (O/E) comprises of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 7 is high during the odd field.

Loss of video signal can be detected by monitoring the C/S output. The 50% level of the previous video signal will remain held on the S/H capacitors after the input video signal has gone and the input on pin 2 has defaulted to the clamp voltage. Consequently the C/S output will remain low longer than the normal vertical pulse period. An external timing circuit could be used to detect this condition.

Block Diagram

*Note: RSET must be a 1% resistor.*
Features
- NTSC, PAL and SECAM sync separation
- Single supply, +5V operation
- Precision 50% slicing, internal caps
- Built in programmable color burst filter
- Decodes non-standard verticals
- Horizontal sync output
- Sync. pulse amplitude output
- Same socket can be used for 8-pin EL4581
- Low power CMOS
- Detects loss of signal
- Resistor programmable scan rate
- Few external components
- Available in 16-Pin DIP and SO-16 pkg.

Applications
- Video special effects
- Video test equipment
- Video distribution
- Multimedia
- Displays
- Imaging
- Video data capture
- Video triggers

General Description
The EL4583C extracts timing from video sync in NTSC, PAL, and SECAM systems, and non standard formats, or from computer graphics operating at higher scan rates. Timing adjustment is via an external resistor. Input without valid vertical interval (no serration pulses) produces a default vertical output.

A larger package (16-pin) is used for greater flexibility. The "core" pins match the same pin functions of the 8-pin (EL4581C etc.) for substitution in applications not requiring these features.

Outputs are: composite sync, vertical sync, filter, burst/back porch, horizontal, no signal detect, level, and odd/even output (in interlaced scan formats only).

The EL4583C sync slice level is set to a mid-point halfway between sync tip and the blanking level. This 50% point is determined by two internal sample and hold circuits that track sync tip and back porch levels. It provides hum and noise rejection and compensates for input levels of 0.5V to 2.0Vp-p.

A built in filter attenuates the chroma signal to prevent color burst from disturbing the 50% sync slice. Cut off frequency is set by a resistor to ground from the Filter Cut Off pin. The filter can be by-passed, the video signal is fed to the Video Input.

A DC voltage, twice the sync amplitude, from the Level Output pin drives AGC circuits. A TTL/CMOS compatible No Signal Detect Output signals a loss or reduction in input signal level. A resistor sets the Set Detect Level.

The EL4583C is manufactured using Elantec's high performance analog CMOS process.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4583CN</td>
<td>-40°C to +85°C</td>
<td>16-Pin DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL4583CS</td>
<td>-40°C to +85°C</td>
<td>16-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagram

*Note: RSET must be a 1% resistor.*
### Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Supply</td>
<td></td>
<td>7V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>260°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Pin Voltages</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td>-0.5V to VCC + 0.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0602.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25^\circ C) and QA sample tested at (T_A = 25^\circ C), (T_{MAX}) and (T_{MIN}) per QA test plan QCX0602.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0602.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25^\circ C) for information purposes only.</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics \((V_{DD} = 5V, T_A = 25^\circ C, RSET = 681k, RF = 22k, RLV = 82k)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD</td>
<td>(V_{DD} = 5V) (Note 1)</td>
<td>25°C</td>
<td>2.5</td>
<td>4</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Clamp Voltage</td>
<td>Pins 4, 8, unloaded</td>
<td>25°C</td>
<td>1.3</td>
<td>1.55</td>
<td>1.8</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>No Signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clamp Charge Current</td>
<td>Pins 4, 8, (V_{IN} = 4)</td>
<td>25°C</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Ref. Voltage (V_{REF})</td>
<td>Pin 12, (V_{DD} = 5V) (Note 3)</td>
<td>25°C</td>
<td>1.5</td>
<td>1.75</td>
<td>2</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Filter Reference Voltage, VRF</td>
<td>Pin 1</td>
<td>25°C</td>
<td>0.35</td>
<td>0.5</td>
<td>0.65</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Level Reference Current</td>
<td>Pin 2 (Note 4)</td>
<td>25°C</td>
<td>1.5</td>
<td>2.5</td>
<td>3.5</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>VOL Output Low Voltage</td>
<td>(I_{OL} = 1.6\ \mu A)</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>VOH Output High Voltage</td>
<td>(I_{OH} = -40\ \mu A)</td>
<td>25°C</td>
<td>4</td>
<td>2.4</td>
<td>4</td>
<td>IV</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(I_{OH} = -1.6\ \mu A)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: No video signal, outputs unloaded.
Note 2: At loss of signal (pin 10 high) the pull down current source switches to a value of 10 \(\mu A\).
Note 3: Tested for \(V_{DD} 5V \pm 5\%\).
Note 4: Current sourced from pin 2 is \(V_{REF}/RSET\).
Dynamic Characteristics

RF = 22 kΩ, RSET = 681 kΩ, VDD = 5V, 1 Vp-p, VIDEO, TA = 25°C, C_L = 15 pF, IOH = -1.6 mA, IOL = 1.6 mA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Horizontal Pulse Width, Pin 15, t_H</td>
<td>(Note 5)</td>
<td>3.8</td>
<td>5</td>
<td>6.2</td>
<td>I</td>
<td>μs</td>
</tr>
<tr>
<td>Vertical Sync Width, Pin 5, t_VS</td>
<td>(Note 6)</td>
<td>195</td>
<td></td>
<td></td>
<td>I</td>
<td>μs</td>
</tr>
<tr>
<td>Burst/Back Porch Width, Pin 11, t_B</td>
<td>(Note 5)</td>
<td>2.7</td>
<td>3.7</td>
<td>4.7</td>
<td>I</td>
<td>μs</td>
</tr>
<tr>
<td>Filter Attenuation</td>
<td>F_IN = 3.6 MHz</td>
<td>12</td>
<td></td>
<td></td>
<td>IV</td>
<td>dB</td>
</tr>
<tr>
<td>Comp. Sync Prop. Delay, t_CS</td>
<td>V_IN (Pin 4)—Comp Sync</td>
<td>250</td>
<td>400</td>
<td></td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>Input Dynamic Range</td>
<td>p-p NTSC Signal</td>
<td>0.4</td>
<td>2</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Slice Level</td>
<td>Input Voltage = 1 Vp-p</td>
<td>40%</td>
<td>50%</td>
<td>60%</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VSlice/VBlank</td>
<td>40%</td>
<td>50%</td>
<td>60%</td>
<td>IV</td>
<td></td>
</tr>
<tr>
<td>Level Out, Pin 9</td>
<td>Input Voltage = 1 Vp-p</td>
<td>555</td>
<td>620</td>
<td>685</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>Pin 4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vertical Sync Default Time, t_VSD</td>
<td>(Note 8)</td>
<td>27</td>
<td>36</td>
<td>45</td>
<td>I</td>
<td>μs</td>
</tr>
<tr>
<td>Loss of Signal Time-Out</td>
<td>Pin 10</td>
<td>400</td>
<td>600</td>
<td>800</td>
<td>I</td>
<td>μs</td>
</tr>
<tr>
<td>Burst/Back Porch Delay, t_BD</td>
<td>See Figure 4</td>
<td>250</td>
<td>400</td>
<td></td>
<td>V</td>
<td>μs</td>
</tr>
</tbody>
</table>

Note 5: Width is a function of RSET.
Note 6: c/s, Vertical, Back porch and H are all active low, VOH = 0.8V. Vertical is 3H lines wide of NTSC signal.
Note 7: Attenuation is a function of RF. See filter typical characteristics.
Note 8: Vertical pulse width in absence of serrations on input signal.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Filter Cut-Off</td>
<td>A resistor RF connected between this input and ground determines the input filter characteristic. Increasing RF increases the filter 3.58 MHz color burst attenuation. See the graph showing filter characteristics.</td>
</tr>
<tr>
<td>2</td>
<td>Set Detect Level</td>
<td>A resistor RLV connected between pin 2 and ground determines the value of the minimum signal which will trigger the loss of signal output on pin 10. The relationship is VpMIN = 0.75 RLV/RSET, where VpMIN is the minimum detected sync pulse amplitude applied to pin 4. See characterization curve.</td>
</tr>
<tr>
<td>3</td>
<td>Composite Sync Output</td>
<td>This output replicates all the sync inputs on the input video.</td>
</tr>
<tr>
<td>4</td>
<td>Filter Input</td>
<td>The filter is a 3 pole active filter with a gain of 2, designed to produce a constant phase delay of nominally 260 ns with signal amplitude. Resistor RF on pin 1 controls the filter cut-off. An internal clamp sets the minimum voltage on pin 4 at 1.55V when the input becomes low impedance. Above the clamp voltage, an input current of 1 μA charges the input coupling capacitor. With loss of signal, the current source switches to a value of 10 μA, for faster signal recovery.</td>
</tr>
<tr>
<td>5</td>
<td>Vertical Sync Output</td>
<td>The vertical sync output is synchronous with the first serration pulse rising edge in the vertical interval of the input signal and ends on the trailing edge of the first equalizing Output pulse after the vertical interval. It will therefore be slightly more than 3H lines wide.</td>
</tr>
</tbody>
</table>
### Pin Description — Contd.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Digital Ground</td>
<td>This is the ground return for digital buffer outputs.</td>
</tr>
<tr>
<td>7</td>
<td>Filter Output</td>
<td>Output of the active 3 pole filter which has its input on pin 4. It is recommended to ac couple the output to pin 8.</td>
</tr>
<tr>
<td>8</td>
<td>Video Input</td>
<td>This input can be directly driven by the signal if it is desired to bypass the filter, for example, in the case of strong clean signals. This input is 6 dB less sensitive than the filter input.</td>
</tr>
<tr>
<td>9</td>
<td>Level Output</td>
<td>This pin provides an analog voltage which is nominally equal to twice the sync pulse amplitude of the video input signal applied to pin 4. It therefore provides an indication of signal strength.</td>
</tr>
<tr>
<td>10</td>
<td>No Signal Detect</td>
<td>This is a digital output which goes high when either a) loss of input signal or b) the input signal level falls below a predetermined amplitude as set by RLV on pin 2. There will be several horizontal lines delay before the output is initiated.</td>
</tr>
<tr>
<td>11</td>
<td>Burst/Back Porch</td>
<td>The start of back porch output is triggered on the trailing edge of normal H sync, and on the rising edge of serration pulses in the vertical interval. The pulse is timed out internally to produce a one-shot output. The pulse width is a function of RSET. This output can be used for d.c. restore functions where the back porch level is a known reference.</td>
</tr>
<tr>
<td>12</td>
<td>RSET</td>
<td>The current through the resistor RSET determines the timing of the functions within the I.C. These functions include the sampling of the sync pulse 50% point, back porch output and the 2H eliminator. For faster scan rates, the resistor needs to be reduced inversely. For NTSC 15.7 kHz scan rate RSET is 681k 1%. RSET must be a 1% resistor.</td>
</tr>
<tr>
<td>13</td>
<td>Odd/Even Output</td>
<td>Odd-even output is low for even field and high for odd field. The operation of this circuit has been improved for rejecting spurious noise pulses such as those present in VCR signals.</td>
</tr>
<tr>
<td>14</td>
<td>VDD 5V</td>
<td>The internal circuits are designed to have a high immunity to supply variations, although as with most I.C.s a 0.1 μF decoupling capacitor is advisable.</td>
</tr>
<tr>
<td>15</td>
<td>Horizontal Sync</td>
<td>This output produces only true H pulses of nominal width 5 μs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2H eliminator circuit.</td>
</tr>
<tr>
<td>16</td>
<td>Analog Ground</td>
<td>This is the ground return for the signal paths in the chips, RSET, RF and RLV.</td>
</tr>
</tbody>
</table>
Typical Performance Characteristics

1. **RSET vs Horizontal Frequency**
   - Plot showing RSET (in kΩ) vs Frequency (in kHz).

2. **Back Porch Clamp On Time vs RSET**
   - Plot showing clamp time (in μs) vs RSET (in kΩ).

3. **Vertical Default Delay Time vs RSET**
   - Plot showing delay time (in μs) vs RSET (in kΩ).

4. **Filter 3 dB BW vs RF**
   - Plot showing filter 3 dB bandwidth (in dB) vs Frequency (in kHz).

5. **Level Out (Pin 9) vs Sync. Tip Amplitude**
   - Plot showing level out (in mV) vs sync. tip (in mV).

6. **Minimum Signal Detect vs RLV**
   - Plot showing RLV (in kΩ) vs sync. tip (in mV).

7. **Filter Attenuation vs RF @ f = 3.58 MHz**
   - Plot showing filter attenuation in dBs vs filter resistor on Pin 1 in kΩ.

**Note 1:** For RLV < 100 kΩ, no signal detect output (pin 10) will default high at minimum signal sensitivity specification, or at complete loss of signal.
Timing Diagram

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

f. Horizontal sync output produces the true "H" pulses of nominal width of 5μs. It has the same delay as the composite sync.
**Figure 2**

**SIGNAL 2a. COMPOSITE VIDEO INPUT**

- Slice Level
- 50%
- \( t_{CS} \) Comp Sync Prop Delay

**SIGNAL 2b. COMPOSITE SYNC. OUTPUT**

- \( t_{CS-VS} \) Comp Sync Vert Sync Delay

**SIGNAL 2c. VERTICAL SYNC. OUTPUT**

- \( t_{CS-DE} \) Comp Sync ODD/EVEN Delay

**SIGNAL 2d. ODD - EVEN OUTPUT**

- Burst Delay
- \( t_{BS} \) Burst Width

**SIGNAL 2e. BURST/BACK PORCH OUTPUT**

**Figure 3**

**SIGNAL 3a. COMPOSITE VIDEO INPUT**

- Lines
  - 2
  - 3
  - 4
  - 5
- (No Vertical Sync Pulses)
- \( t_{VS0} \) Vert Sync Default Delay

**SIGNAL 3b. VERTICAL SYNC. OUTPUT**
Figure 4. Standard (NTSC Input) H. Sync Detail
Description of Operation

A simplified block schematic is shown in Figure 1. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC coupled to pin 4 via the capacitor C1, nominally 0.1 uF. The clamp circuit A1 will prevent the input signal on pin 4 going any more negative than 1.5V, the value of reference voltage VR1. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I1, nominally 10 uA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 μs for a 15.75 kHz timebase. From I = C \cdot \frac{V}{t}, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C1 will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be VDD less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I1 directly tracks reference current ITR and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. The filter cut-off frequency is controlled by an external resistor from pin 1 to ground.

Internal reference voltages (block VREF) with high immunity to supply voltage variation are derived on the chip. Reference VR4 with op-amp A2 forces pin 12 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance RSET will determine the value of the reference current ITR. The internal resistance R3 is only about 6 kΩ, much less than RSET. All the internal timing functions on the chip are referenced to ITR and have excellent supply voltage rejection.

To improve noise immunity, the output of the 3 pole filter is brought out to pin 7. It is recommended to AC couple the output to pin 8, the video input pin. In case of strong clean video signal, the video input pin, pin 8, can be driven by the signal directly.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync pulse with a threshold voltage VR2 which is referenced at a fixed level above the clamp voltage VR1. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 μs to enable the actual sample of 2 μs to be taken on the optimum section of the sync pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through IOT.

The 50% level of the sync tip is derived, through the resistor divided R1 and R2, from the sample and held voltages VTIP and VBP, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S output buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.
Description of Operation — Contd.
The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer vertical sync pulse widths. The internal timing circuits are referenced to \( I_{OT} \) and \( V_{R3} \), the timeout period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absence of a serration pulse, an internal timer will default the start of vertical.

The Horizontal circuit senses the C/S edges and produces the true horizontal pulses of nominal width 5 \( \mu \)s. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2 H eliminator circuit. The 2 H eliminator circuit initiates a time out period after a horizontal pulse if generated. The time out period is a function of \( I_{OT} \) which is set by RSET.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of \( I_{OT} \) and will therefore track the scan rate set by \( R_{SET} \).

The odd/even circuit circuit (O/E) is comprised of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 13 is high during the odd field.

Loss of video signal can be detected by monitoring the No Signal Detect Output pin 10. The VTIP voltage held by the sample and hold is compared with a voltage level set by RLV on pin 2. Pin 10 output goes high when the VTIP falls below RLV set value.

VTIP voltage is also passed through an amplifier with gain of 2 and buffed to pin 9. This is done to provide an indication of signal strength. The Level Output signal can be used for AGC applications.
Figure 5

* Note: RSET must be a 1% resistor
**Features**
- 36 MHz, general purpose PLL
- 4 FSC based timing (use the EL4585 for 8 FSC)
- Compatible w/EL4583 Sync Separator
- VCXO, Xtal, or LC tank oscillator
- <2 ns jitter (VCXO)
- User controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed TV scan rate clock divisors
- Selectable external divide for custom ratios
- Single 5V, low current operation

**Applications**
- Pixel Clock regeneration
- Video compression engine (MPEG) clock generator
- Video capture or digitization
- PIP (Picture in Picture) timing generator
- Text or graphics overlay timing

**General Description**
The EL4584C is a PLL (Phase Lock Loop) sub system, designed for video applications but also suitable for general purpose use up to 36 MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to “coast” is provided for applications were periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 4 FSC, 3 FSC, 13.5 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 8 FSC, 6 FSC, 27 MHz (CCIR 601 format) etc. use the EL4585, which includes an additional divide by 2 stage.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be bypassed and an external divider chain used.

<table>
<thead>
<tr>
<th>FREQUENCIES and DIVISORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
</tr>
<tr>
<td>Divisor</td>
</tr>
<tr>
<td>Divisor</td>
</tr>
<tr>
<td>Divisor</td>
</tr>
</tbody>
</table>

CCIR 601 Divisors yield 720 pixels in the portion of each line for NTSC and PAL.
Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL in the active portion.
3Fsc numbers do not yield integer divisors.

**Ordering Information**
- Part No. Temp. Range Package Outline #
  - EL4584CN -40°C to +85°C 16-Pin DIP MDP0031
  - EL4584CS -40°C to +85°C 16-Lead SO MDP0027

For 6Fsc and 8Fsc clock frequencies, see EL4585 datasheet.

**Demo Board**
A demo PCB is available for this product. Request “EL4584/5 Demo Board”.

**Connection Diagram**

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**EL4584C Horizontal Genlock, 4 FSC**

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**Connection Diagram**

- EL4584 SO, P-DIP Packages

---

3-214
Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VCC Supply</strong></td>
<td></td>
<td>7V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Storage Temperature</strong></td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Lead Temperature</strong></td>
<td>260°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Pin Voltages</strong></td>
<td>-0.5V to (V_{CC} + 0.5V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Operating Ambient Temperature Range</strong></td>
<td></td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Test Procedure
- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at \(T_A = 25^\circ C\) and QA sample tested at \(T_A = 25^\circ C\).
- **III**: \(T_{MAX}\) and \(T_{MIN}\) per QA test plan QCX0002.
- **IV**: QA sample tested per QA test plan QCX0002.
- **V**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at \(T_A = 25^\circ C\) for information purposes only.

DC Electrical Characteristics \((V_{DD} = 5V, T_A = 25^\circ C\) unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{DD})</td>
<td>(V_{DD} = 5V) (Note 1)</td>
<td>25°C</td>
<td>2</td>
<td>4</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(V_{IL}) Input Low Voltage</td>
<td></td>
<td>25°C</td>
<td></td>
<td>1.5</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH}) Input High Voltage</td>
<td></td>
<td>25°C</td>
<td>3.5</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IL}) Input Low Current</td>
<td>All inputs except COAST, (V_{IN} = 1.5V)</td>
<td>25°C</td>
<td></td>
<td>-100</td>
<td></td>
<td>I</td>
<td>nA</td>
</tr>
<tr>
<td>(I_{IH}) Input High Current</td>
<td>All inputs except COAST, (V_{IN} = 3.5V)</td>
<td>25°C</td>
<td></td>
<td>100</td>
<td></td>
<td>I</td>
<td>nA</td>
</tr>
<tr>
<td>(I_{IL}) Input Low Current</td>
<td>COAST pin, (V_{IN} = 1.5V)</td>
<td>25°C</td>
<td></td>
<td>-100</td>
<td>-60</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{IH}) Input High Current</td>
<td>COAST pin, (V_{IN} = 3.5V)</td>
<td>25°C</td>
<td></td>
<td>60</td>
<td>100</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(V_{OL}) Output Low Voltage</td>
<td>Lock Det, (I_{OL} = 1.6mA)</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OH}) Output High Voltage</td>
<td>Lock Det, (I_{OH} = -1.6mA)</td>
<td>25°C</td>
<td></td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OL}) Output Low Voltage</td>
<td>CLK, (I_{OL} = 3.2mA)</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OH}) Output High Voltage</td>
<td>CLK, (I_{OH} = -3.2mA)</td>
<td>25°C</td>
<td></td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OL}) Output Low Voltage</td>
<td>OSC Out, (I_{OL} = 200\mu A)</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OH}) Output High Voltage</td>
<td>OSC Out, (I_{OH} = -200\mu A)</td>
<td>25°C</td>
<td></td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_{OL}) Output Low Current</td>
<td>Filter Out, (V_{OUT} = 2.5V)</td>
<td>25°C</td>
<td>200</td>
<td>300</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OH}) Output High Current</td>
<td>Filter Out, (V_{OUT} = 2.5V)</td>
<td>25°C</td>
<td></td>
<td>-300</td>
<td>-200</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OL}/I_{OH}) Current Ratio</td>
<td>Filter Out, (V_{OUT} = 2.5V)</td>
<td>25°C</td>
<td>1.05</td>
<td>1.0</td>
<td>0.95</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>(I_{LEAK}) Filter Out</td>
<td>Coast Mode, (V_{DD} &gt; V_{OUT} &gt; 0V)</td>
<td>25°C</td>
<td></td>
<td>-100</td>
<td>±1</td>
<td>I</td>
<td>nA</td>
</tr>
</tbody>
</table>

Note 1: All inputs to 0V, COAST floating.
AC Electrical Characteristics \((V_{DD} = 5\text{V}, T_A = 25^\circ\text{C} \text{ unless otherwise noted})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO Gain @ 20 MHz</td>
<td>Test Circuit 1</td>
<td>25°C</td>
<td>15.5</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>H-sync S/N Ratio</td>
<td>(V_{DD} = 5\text{V}) (Note 2)</td>
<td>25°C</td>
<td>35</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>Jitter</td>
<td>VCXO Oscillator</td>
<td>25°C</td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>Jitter</td>
<td>LC Oscillator (Typ)</td>
<td>25°C</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 2: Noisy video signal input to EL4583C, H-sync input to EL4584C. Test for positive signal lock.

Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>16,1,2</td>
<td>Prog A,B,C</td>
<td>Digital inputs to select (\div N) value for internal counter. See table below for values.</td>
</tr>
<tr>
<td>3</td>
<td>Osc/VCO Out</td>
<td>Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.</td>
</tr>
<tr>
<td>4</td>
<td>(V_{DD}(A))</td>
<td>Analog positive supply for oscillator, PLL circuits.</td>
</tr>
<tr>
<td>5</td>
<td>Osc/VCO In</td>
<td>Input from external VCO.</td>
</tr>
<tr>
<td>6</td>
<td>(V_{SS}(A))</td>
<td>Analog ground for oscillator, PLL circuits.</td>
</tr>
<tr>
<td>7</td>
<td>Charge Pump Out</td>
<td>Connect to loop filter. If the H-sync phase is leading or H-sync frequency (&gt;) (\text{CLK} \div N), current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency (&lt;) (\text{CLK} \div N), current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.</td>
</tr>
<tr>
<td>8</td>
<td>Div Select</td>
<td>Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting (\text{CLK} \div N). When low, the internal divider is disabled and EXT DIV is an input from an external (\div N).</td>
</tr>
<tr>
<td>9</td>
<td>Coast</td>
<td>Tri-state logic input. Low((&lt;\frac{1}{3}\text{V}<em>{\text{CC}})) = normal mode, Hi (\frac{1}{2}\text{ to }\frac{2}{3}\text{V}</em>{\text{CC}}) = fast lock mode, (\text{High}(\geq\frac{2}{3}\text{V}_{\text{CC}})) = coast mode.</td>
</tr>
<tr>
<td>10</td>
<td>H-sync In</td>
<td>Horizontal sync pulse (CMOS level) input.</td>
</tr>
<tr>
<td>11</td>
<td>(V_{DD}(D))</td>
<td>Positive supply for digital, I/O circuits.</td>
</tr>
<tr>
<td>12</td>
<td>Lock Det</td>
<td>Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.</td>
</tr>
<tr>
<td>13</td>
<td>Ext Div</td>
<td>External Divide input when DIV SEL is low, internal (\div N) output when DIV SEL is high.</td>
</tr>
<tr>
<td>14</td>
<td>(V_{SS}(D))</td>
<td>Ground for digital, I/O circuits.</td>
</tr>
<tr>
<td>15</td>
<td>CLK Out</td>
<td>Buffered output of the VCO.</td>
</tr>
</tbody>
</table>

VCO Divisors Table 1

<table>
<thead>
<tr>
<th>Prog A Pin 16</th>
<th>Prog B Pin 1</th>
<th>Prog C Pin 2</th>
<th>Div Value N</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>851</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>864</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>944</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1135</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>682</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>858</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>780</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>910</td>
</tr>
</tbody>
</table>
Timing Diagrams

PLL Locked Condition (Phase Error = 0)

-110 ns ± 50 ns

H-Sync (input)

Ext. Div. (input or output)

Falling edge of H-sync + 110 ns locks to rising edge of Ext Div signal.

Out of Lock Condition

$\theta_E = \frac{T_\theta}{T_H} \times 360^\circ$

$T_H =$ H-sync period

$T_\theta =$ phase error period

Test Circuit 1

4584-2

4584-3

4584-5
Typical Performance Curves

**Idd vs Fosc**

![Graph showing Idd vs Fosc with labels for different temperatures: 125°C, 40°C, and 25°C.]

**4584 OSC Gain @ 20 MHz vs Temp**

![Graph showing 4584 OSC Gain vs Temp with YIN = 10 mVRMS.]

**Typical Varactor**

![Graph showing typical varactor characteristics with C_T and R_T values for different frequencies.]

**OSC Gain vs Fosc**

![Graph showing OSC Gain vs Fosc with duty cycle vs % values.]

**Charge Pump Duty Cycle vs θ_E**

![Graph showing charge pump duty cycle vs θ_E with range from -2π to 2π.]

3-218
Description Of Operation
The horizontal sync signal (CMOS level, falling leading edge) is input to H-sync input (pin 10). This signal is delayed about 110 ns, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4584C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. The modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to generate the clock. An LC tank resonator has greater "pull" than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The "pullability" of the circuit refers to the ability to "pull" the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of a VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to a divide by N counter, and to the CLK out pin. The divisor N is determined by the state of pins 1, 2, and 16 and is described in table 1 above. The divided signal is sent, along with the delayed H-sync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output FILTER (pin 7). A VCO with positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with control voltage for the oscillators in figures 10 and 11 below.

VCO
The VCO should be tuned so its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The range of the charge pump output (pin 7) is 0 to 5 volts and it can source or sink a maximum of about 300 μA, so all frequency control must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the h-sync signal experiences frequency variations of greater than about 300 ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-SYNC input frequency is greater than CLK frequency ÷ N, charge pump output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, which lowers its capacitance, thus tending to increase VCO frequency. Conversely, filter output pulls current from the filter capacitor when H-SYNC frequency is less than CLK ÷ N, forcing the VCO frequency lower.

Loop Filter
The loop filter controls how fast the VCO will respond to a change in filter output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of charge pump output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and undershoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviation from these values is not out of the ordinary.
Description of Operation — Contd.

External Divide
DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode
Normal mode is enabled by pulling COAST (pin 9) low (below $\frac{1}{3}$ $V_{CC}$). If H-sync and CLK divided by N have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of CLK divided by N exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer uses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

Fast Lock Mode
Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between $\frac{1}{3}$ and $\frac{2}{3}$ $V_{CC}$). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a “fast” lock of the signals. Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value and placing the device into normal mode should result in a normal lock very quickly. Fast Lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

Coast Mode
Coast mode is enabled by pulling COAST (pin 9) high (above $\frac{1}{3}$ $V_{CC}$). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant as possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect
Lock detect (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIV relative to H-SYNC in, tending to offset or add to the 110 ns internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the loop filter series resistor $R_2$ will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110 ns. (See timing diagrams.) Increasing $R_2$ decreases phase error, while decreasing $R_2$ increases phase error. (Phase error is positive when EXT DIV lags H-SYNC.) The resistance needed will depend on VCO design or VCXO module selection.
Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 14.31818 MHz, with an H-sync frequency of 15.734 kHz.
2. Choose a reasonable inductor value (10-20μH works well). We choose 15 μH.
3. Calculate \( C_T \) needed to produce \( F_{OSC} \).

\[
F_{OSC} = \frac{1}{2\pi \sqrt{LC_T}}
\]

\[
C_T = \frac{1}{4\pi^2F^2L} = \frac{1}{4\pi^2(14.3186\times10^6)^2(15.734)} = 8.2 \text{ pF}
\]
4. From the varactor data sheet find \( C_V @ 2.5\text{V} \), the desired lock voltage. \( C_V = 23 \text{ pF for our SMV1204-12, for example.} \)
5. \( C_2 \) should be about 10\( C_V \), so we choose \( C_2 = 220 \text{ pF for our example.} \)
6. Calculate \( C_1 \). Since

\[
C_T = \frac{C_1 C_2 C_V}{(C_1 C_2) + (C_1 C_V) + (C_2 C_V)}
\]

then

\[
C_1 = \frac{C_2 C_T C_V}{(C_2 C_V) - (C_2 C_T) - (C_T C_V)}
\]

For our example, \( C_1 = 14 \text{ pF.} \) (A trim cap may be used for fine tuning. Examples for each frequency using the internal divider follow.

**Typical Application**

Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>L1 (μH)</th>
<th>C1 (pF)</th>
<th>C2 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13.301</td>
<td>15</td>
<td>18</td>
<td>220</td>
</tr>
<tr>
<td>13.5</td>
<td>15</td>
<td>17</td>
<td>220</td>
</tr>
<tr>
<td>14.75</td>
<td>12</td>
<td>18</td>
<td>220</td>
</tr>
<tr>
<td>17.734</td>
<td>12</td>
<td>10</td>
<td>220</td>
</tr>
<tr>
<td>19.238</td>
<td>20</td>
<td>20</td>
<td>220</td>
</tr>
<tr>
<td>12.273</td>
<td>18</td>
<td>17</td>
<td>220</td>
</tr>
<tr>
<td>14.318</td>
<td>15</td>
<td>14</td>
<td>220</td>
</tr>
</tbody>
</table>

Note: Use shielded inductors for optimum performance.
### Xtal VCO Component Values (Approximate)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>R1 (kΩ)</th>
<th>C1 (pF)</th>
<th>C2 (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13.301</td>
<td>300</td>
<td>15</td>
<td>.001</td>
</tr>
<tr>
<td>13.5</td>
<td>300</td>
<td>15</td>
<td>.001</td>
</tr>
<tr>
<td>14.75</td>
<td>300</td>
<td>15</td>
<td>.001</td>
</tr>
<tr>
<td>17.734</td>
<td>300</td>
<td>15</td>
<td>.001</td>
</tr>
<tr>
<td>10.738</td>
<td>300</td>
<td>15</td>
<td>.001</td>
</tr>
<tr>
<td>12.273</td>
<td>300</td>
<td>15</td>
<td>.001</td>
</tr>
<tr>
<td>14.318</td>
<td>300</td>
<td>15</td>
<td>.001</td>
</tr>
</tbody>
</table>

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

### Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:

$$\theta_{in}(s) \rightarrow + \rightarrow KD \rightarrow F(s) \rightarrow KVCO \rightarrow \theta_{out}(s)$$

Where:

- $K_d =$ phase detector gain in A/rad
- $F(s) =$ loop filter impedance in V/A
- $K_{VCO} =$ VCO gain in rad/s/V
- $N =$ internal or external divisor

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_d K_{VCO}}{N \omega_n^2}, C_4 = \frac{C_3}{10}, R_3 = \frac{2N \zeta \omega_n}{K_d K_{VCO}}$$

Where $\omega_n =$ loop filter bandwidth, and $\zeta =$ loop filter damping factor.

1. $K_d = 300 \mu A/2\pi rad = 4.77e-5 A/ rad$ for the EL4584C.

2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example, $\omega_n = 15.734 kHz/20 = 787 Hz \approx 5000 rad/S$.


$$N = \frac{VCO_{frequency}}{H-SYNC_{frequency}} = \frac{14.3188 M}{15.73426 k} = 910$$

4. $K_{VCO}$ represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn’t) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor.
transfer function \( C_V = F(V_C) \), where \( V_C \) is the reverse bias control voltage, and \( C_V \) is varactor capacitance. Since \( F(V_C) \) is nonlinear, it is probably best to build the VCO and measure \( K_{VCO} \) about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals \( K_{VCO} \). For our example, \( K_{VCO} = 6.05 \text{ Mrad/s/V} \).

\[
\text{Fosc vs } V_C, \text{ LC VCO}
\]

**Lock Time**

Let \( T = R_3C_3 \). As \( T \) increases, damping increases, but so does lock time. Decreasing \( T \) decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping \((\zeta = 1)\) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly over-damped \((\zeta > 1)\), trading lock time for increased stability.

**Typical Loop Filter**

\[
\text{LC Loop Filter Components (Approximate)}
\]

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>R2 (k(\Omega))</th>
<th>R3 (k(\Omega))</th>
<th>C3 ((\mu)F)</th>
<th>C4 ((\mu)F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13.301</td>
<td>100</td>
<td>30</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>13.5</td>
<td>100</td>
<td>30</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>14.75</td>
<td>100</td>
<td>33</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>17.734</td>
<td>100</td>
<td>39</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>10.738</td>
<td>100</td>
<td>22</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>12.273</td>
<td>100</td>
<td>27</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>14.318</td>
<td>100</td>
<td>30</td>
<td>0.01</td>
<td>0.001</td>
</tr>
</tbody>
</table>

**Xtal Loop Filter Components (Approximate)**

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>R2 (k(\Omega))</th>
<th>R3 (M(\Omega))</th>
<th>C3 (pF)</th>
<th>C4 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13.301</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>13.5</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>14.75</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
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<td>4.3</td>
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</tr>
<tr>
<td>10.738</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
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<td>100</td>
<td>4.3</td>
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<td>6.8</td>
</tr>
<tr>
<td>14.318</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
</tbody>
</table>
PCB Layout Considerations
It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to “hand-waving” influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.
The VCO and loop filter section of the EL4583/4/5 demo board can be implemented in the following configurations:

(1) VCXO

(2) XTAL

(3) LC Tank
Component Sources

Inductors
• Dale Electronics
  E. Highway 50
  PO Box 180
  Yankton, SD 57078-0180
  (605) 665-9301

Crystals, VCXO, VCO Modules
• Connor-Winfield
  2111 Comprehensive Drive
  Aurora, IL 60606
  (708) 851-4722

• Piezo Systems
  100 K Street
  PO Box 619
  Carlisle, PA 17013
  (717) 249-2151

• Reeves-Hoffman
  400 West North Street
  Carlisle, PA 17013
  (717) 243-5929

• SaRonix
  151 Laura Lane
  Palo Alto, CA 94043
  (415) 856-6900

• Standard Crystal
  9940 Baldwin Place
  El Monte, CA 91731
  (818) 443-2121

Varactors
• Alpha Industries
  20 Sylvan Road
  Woburn, MA 01801
  (617) 935-5150

• Motorola Semiconductor Products
  2100 E. Elliot
  Tempe, AZ 85284
  (602) 244-6900

Note: These sources are provided for information purposes only. No endorsement of these companies is implied by this listing.
Features
• 36 MHz, general purpose PLL
• 8 FSC timing. (Use the EL4584 for 4 FSC)
• Compatible with EL4583C Sync Separator
• VCXO, Xtal, or LC tank oscillator
• <2nS jitter (VCXO)
• User-controlled PLL capture and lock
• Compatible with NTSC and PAL TV formats
• <2nS jitter (VCXO)
• User-controlled PLL capture and lock
• Compatible with NTSC and PAL TV formats
• 8 FSC, 6 FSC, 27 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 4 FSC, 3 FSC, 13.5 MHz (CCIR 601 format) etc., use the EL4584, which does not have the additional divide by 2 stage of the EL4585.

Applications
• Pixel Clock regeneration
• Video compression engine (MPEG) clock generator
• Video Capture or digitization
• PIP (Picture In Picture) timing generator
• Text or Graphics overlay timing

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL4585CN</td>
<td>-40°C to +85°C</td>
<td>16-Pin DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL4585CS</td>
<td>-40°C to +85°C</td>
<td>16-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

For 3Fsc and 4Fsc clock frequency operation, see EL4584 datasheet.

Demo Board
A demo PCB is available for this product. Request "EL4584/5 Demo Board".

General Description
The EL4585C is a PLL (Phase Lock Loop) sub system, designed for video applications, but also suitable for general purpose use up to 36 MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications where periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 8 FSC, 6 FSC, 27 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 4 FSC, 3 FSC, 13.5 MHz (CCIR 601 format) etc., use the EL4584, which does not have the additional divide by 2 stage of the EL4585.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be by passed and an external divider chain used.

<table>
<thead>
<tr>
<th>FREQUENCIES and DIVISORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
</tr>
<tr>
<td>Divisor*</td>
</tr>
<tr>
<td>PAL Fosc (MHz)</td>
</tr>
<tr>
<td>Divisor*</td>
</tr>
<tr>
<td>NTSC Fosc (MHz)</td>
</tr>
</tbody>
</table>

CCIR 601 divisors yield 1440 pixels in the active portion of each line for NTSC and PAL.
Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL.
6Fsc frequencies do not yield integer divisors.
*Divisor does not include + 1 block.

Connection Diagram

Connection Diagram

EL4585 SO, P-DIP Packages

For 3Fsc and 4Fsc clock frequency operation, see EL4584 datasheet.

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EL4585 SO, P-DIP Packages

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Demo Board
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### Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
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<td>VCC Supply</td>
<td>7V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>260°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin Voltages</td>
<td>-0.5V to VCC + 0.5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elatec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Tj = TC = TA.

### Test Level and Test Procedure

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at TA = 25°C and QA sample tested at TA = 25°C, TMAX and TMIN per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at TA = 25°C for information purposes only.</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics (VDD = 5V, TA = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I DD</td>
<td>VDD = 5V (Note 1)</td>
<td>25°C</td>
<td>2</td>
<td>4</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>VIL Input Low Voltage</td>
<td></td>
<td>25°C</td>
<td></td>
<td>1.5</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VH Input High Voltage</td>
<td></td>
<td>25°C</td>
<td>3.5</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL Input Low Current</td>
<td>All inputs except COAST, VIL = 1.5V</td>
<td>25°C</td>
<td>-100</td>
<td></td>
<td>I</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>IIH Input High Current</td>
<td>All inputs except COAST, VIL = 3.5V</td>
<td>25°C</td>
<td>100</td>
<td></td>
<td>I</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>IIL Input Low Current</td>
<td>COAST pin, VIL = 1.5V</td>
<td>25°C</td>
<td>-100</td>
<td>-60</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IIH Input High Current</td>
<td>COAST pin, VIL = 3.5V</td>
<td>25°C</td>
<td>60</td>
<td>100</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VOL Output Low Voltage</td>
<td>Lock Det, IOL = 1.6mA</td>
<td>25°C</td>
<td>0.4</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH Output High Voltage</td>
<td>Lock Det, IOH = -1.6mA</td>
<td>25°C</td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL Output Low Voltage</td>
<td>CLK, IOL = 3.2mA</td>
<td>25°C</td>
<td>0.4</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH Output High Voltage</td>
<td>CLK, IOH = -3.2mA</td>
<td>25°C</td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL Output Low Voltage</td>
<td>OSC Out, IOL = 200μA</td>
<td>25°C</td>
<td>0.4</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH Output High Voltage</td>
<td>OSC Out, IOH = -200μA</td>
<td>25°C</td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IOL Output Low Current</td>
<td>Filter Out, VOUT = 2.5V</td>
<td>25°C</td>
<td>200</td>
<td>300</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IOH Output High Current</td>
<td>Filter Out, VOUT = 2.5V</td>
<td>25°C</td>
<td>-300</td>
<td>-200</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IOL/IIm Current Ratio</td>
<td>Filter Out, VOUT = 2.5V</td>
<td>25°C</td>
<td>1.05</td>
<td>1.0</td>
<td>0.95</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>ILEAK Filter Out</td>
<td>Coast Mode, VDD &gt; VOUT &gt; 0V</td>
<td>25°C</td>
<td>-100</td>
<td>±1</td>
<td>100</td>
<td>nA</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: All inputs to 0V, COAST floating.
AC Electrical Characteristics \( (V_{DD} = 5\text{V}, T_A = 25^\circ\text{C} \text{ unless otherwise noted}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO Gain @ 20 MHz</td>
<td>Test circuit 1</td>
<td>25°C</td>
<td></td>
<td>15.5</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>H-sync S/N Ratio</td>
<td>(V_{DD} = 5\text{V} ) (Note 2)</td>
<td>25°C</td>
<td></td>
<td>35</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>Jitter</td>
<td>VCO Oscillator</td>
<td>25°C</td>
<td></td>
<td>1</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>Jitter</td>
<td>LC Oscillator (Typ)</td>
<td>25°C</td>
<td></td>
<td>10</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 2: Noisy video signal input to EL4583C, H-sync input to EL4585C. Test for positive signal lock.

Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>16, 1, 2</td>
<td>Prog A,B,C</td>
<td>Digital inputs to select ( \div N ) value for internal counter. See table below for values.</td>
</tr>
<tr>
<td>3</td>
<td>Osc/VCO Out</td>
<td>Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.</td>
</tr>
<tr>
<td>4</td>
<td>(V_{DD} ) (A)</td>
<td>Analog positive supply for oscillator, PLL circuits.</td>
</tr>
<tr>
<td>5</td>
<td>Osc/VCO In</td>
<td>Input from external VCO.</td>
</tr>
<tr>
<td>6</td>
<td>(V_{SS} ) (A)</td>
<td>Analog ground for oscillator, PLL circuits.</td>
</tr>
<tr>
<td>7</td>
<td>Charge Pump Out</td>
<td>Connect to loop filter. If the H-sync phase is leading or H-sync frequency (&gt;) (CLkHz \div 2N), current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency (&lt;) (CLkHz \div 2N), current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.</td>
</tr>
<tr>
<td>8</td>
<td>Div Select</td>
<td>Divide select input. When high, the internal divider is enabled and EXT Div becomes a test pin, outputting (CLkHz \div 2N). When low, the internal divider is disabled and EXT Div is an input from an external (\div N).</td>
</tr>
<tr>
<td>9</td>
<td>Coast</td>
<td>Tri-state logic input. Low (&lt;(\frac{1}{2} \times V_{CC})) = normal mode, Hi Z (or (\frac{1}{2} \text{ to } \frac{3}{2} \times V_{CC})) = fast lock mode, High (&gt;(\frac{3}{2} \times V_{CC})) = coast mode.</td>
</tr>
<tr>
<td>10</td>
<td>H-sync In</td>
<td>Horizontal sync pulse (CMOS level) input.</td>
</tr>
<tr>
<td>11</td>
<td>(V_{DD} ) (D)</td>
<td>Positive supply for digital, I/O circuits.</td>
</tr>
<tr>
<td>12</td>
<td>Lock Det</td>
<td>Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.</td>
</tr>
<tr>
<td>13</td>
<td>Ext Div</td>
<td>External Divide input when DIV SEL is low, internal (\div 2N) output when DIV SEL is high.</td>
</tr>
<tr>
<td>14</td>
<td>(V_{SS} ) (D)</td>
<td>Ground for digital, I/O circuits.</td>
</tr>
<tr>
<td>15</td>
<td>CLK Out</td>
<td>Buffered output of the VCO.</td>
</tr>
</tbody>
</table>

Table 5. VCO Divisors

<table>
<thead>
<tr>
<th>Prog A Pin 16</th>
<th>Prog B Pin 1</th>
<th>Prog C Pin 2</th>
<th>Div Value N</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1702</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1728</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1888</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2270</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1364</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1716</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1560</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1820</td>
</tr>
</tbody>
</table>
**Timing Diagrams**

**PLL Locked Condition (Phase Error = 0)**

- H-Sync (input)
- Ext. Div. (input or output)

Timing Diagrams

- ~110 ns ± 50 ns

**Out of Lock Condition**

- H-Sync
- Ext. Div.
- Charge Pump

\[ \theta_E = \frac{T_\theta}{T_H} \times 360° \]

- \( T_H = \) H-sync period
- \( T_\theta = \) phase error period

**Typical Performance Curves**

**Test Circuit 1**

\[ V_{OUT} \]

\[ V_{IN} \]

\[ 10 \text{ mV}_{RMS} \]
Typical Performance Curves — Contd.

Typical Varactor

EL4585 Block Diagram
Description Of Operation
The horizontal sync signal (CMOS level, falling leading edge) is input to H-SYNC input (pin 10). This signal is delayed about 110nS, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4585C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. These modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to regulate the clock. An LC tank resonator has greater “pull” than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The “pullability” of the circuit refers to the ability to pull the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of the VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to the CLK out pin, divided by two, then sent to the divide by N counter. The divisor N is determined by the state of pins 1, 2, and 16 and is described in table 5 above. The divided signal is sent, along with the delayed H-sync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output, (pin 7). A VCO with a positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with increasing control voltage for the oscillators in figures 10 and 11 below.

VCO
The VCO should be tuned so that its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The output range of the charge pump output (pin 7) is 0 to 5 volts, and it can source or sink a maximum of about 300µA, so all frequency control must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the H-sync signal experiences frequency variations of greater than about 300ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-sync input frequency is greater than CLK frequency ÷ 2N, charge pump output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, thus tending to increase VCO frequency. Conversely, charge pump output pulls current from the filter capacitor when H-sync frequency is less than CLK ÷ 2N, forcing the VCO frequency lower.

Loop Filter
The loop filter controls how fast the VCO will respond to a change in phase comparator output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO “hunting”, preferably in one to two oscillations of charge pump output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and under-shoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can’t respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviations from these values are not out of the ordinary.
External Divide
DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by $2^N$. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode
Normal mode is enabled by pulling COAST (pin 9) low (below $1/3 \times V_{cc}$). If H-SYNC and $CLK \div 2^N$ have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of $CLK \div 2^N$ exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

Fast Lock Mode
Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between $1/3$ and $2/3 \times V_{cc}$). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a “fast lock” of the signals. Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value, and placing the device into normal mode should result in a normal lock very quickly. Fast lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

Coast Mode
Coast mode is enabled by pulling COAST (pin 9) high (above $2/3 \times V_{cc}$). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant as possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect
Lock detect (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIV relative to H-SYNC in, tending to offset or add to the 110nS internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the loop filter series resistor $R_2$ will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110nS. (See timing diagrams.) Increasing $R_2$ decreases phase error, while decreasing $R_2$ increases phase error. (Phase error is positive when EXT DIV lags H-SYNC.) The resistance needed will depend on VCO design or VCXO module selection.
Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 28.636MHz, with an H-sync frequency of 15.734kHz.

2. Choose a reasonable inductor value (1-5µH works well). We choose 3.3µH.

3. Calculate $C_T$ needed to produce $F_{OSC}$:

$$F_{OSC} = \frac{1}{2\pi \sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2 F^2 L} = \frac{1}{4\pi^2 (28.636e6)^2 (3.3e-6)} = 9.4\text{pF}$$

4. From the varactor data sheet find $C_Y @ 2.5V$, the desired lock voltage. $C_Y = 23\text{pF}$ for our SMV1204-12 for example.

5. $C_2$ should be about $10C_Y$, so we choose $C_2 = 220\text{pF}$ for our example.

6. Calculate $C_1$. Since

$$C_T = \frac{C_1 C_2 C_Y}{(C_1 C_2) + (C_1 C_Y) + (C_2 C_Y)}$$

then

$$C_1 = \frac{C_2 C_T C_Y}{(C_2 C_Y) - (C_2 C_T) - (C_T C_Y)}.$$ 

For our example, $C_1 = 17\text{pF}$. (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>L1 (µH)</th>
<th>C1 (pF)</th>
<th>C2 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>26.602</td>
<td>3.3</td>
<td>22</td>
<td>220</td>
</tr>
<tr>
<td>27.0</td>
<td>3.3</td>
<td>21</td>
<td>220</td>
</tr>
<tr>
<td>29.5</td>
<td>2.7</td>
<td>22</td>
<td>220</td>
</tr>
<tr>
<td>35.468</td>
<td>2.2</td>
<td>16</td>
<td>220</td>
</tr>
<tr>
<td>21.476</td>
<td>4.7</td>
<td>26</td>
<td>220</td>
</tr>
<tr>
<td>24.546</td>
<td>3.9</td>
<td>22</td>
<td>220</td>
</tr>
<tr>
<td>28.636</td>
<td>3.3</td>
<td>17</td>
<td>220</td>
</tr>
</tbody>
</table>

Note: Use shielded inductors for optimum performance.
Typical Application
Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

\[
F = \frac{1}{2\pi\sqrt{LC_T}}
\]

\[
C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)}
\]

C_1 is to adjust the center frequency, C_2 DC isolates the control from the oscillator, and V1 is the primary control device. C_2 should be much larger than C_V so that V1 has maximum modulation capability. The frequency of oscillation is given by:
Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:

\[ \frac{V_{in}(s)}{V_{out}(s)} = \frac{K_D \cdot K_{VCO}}{N \cdot \omega_n \cdot (1 + \frac{1}{\zeta})} \]

Where:

- \( K_D \) = phase detector gain in A/rad
- \( F(s) \) = loop filter impedance in V/A
- \( K_{VCO} \) = VCO gain in rad/s/V
- \( N \) = Total internal or external divisor (see 3 below)

It can be shown that for the loop filter shown below:

\[ C_3 = \frac{K_D \cdot K_{VCO}}{N \cdot \omega_n^2} \]

Where \( \omega_n \) = loop filter bandwidth, and \( \zeta \) = loop filter damping factor.

1. \( K_D = 300\mu A/2\pi \text{rad} = 4.77e-5 \text{A/rad} \) for the EL4585C.

2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example, \( \omega_n = 15.734 \text{kHz} / 20 = 787 \text{ Hz} \approx 5000 \text{ rad/S} \).

3. \( N = 910 \times 2 = 1820 \) from table 1.

4. \( K_{VCO} \) represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn’t) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor transfer function \( C_v = F(V_C) \), where \( V_C \) is the reverse bias control voltage, and \( C_v \) is the varactor capacitance. Since \( F(V_C) \) is nonlinear, it is probably best to build the VCO and measure \( K_{VCO} \) about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals \( K_{VCO} \). For our example, \( K_{VCO} = 9.06 \text{ Mrad/s/V} \).

5. Now we can solve for \( C_3, C_4, \) and \( R_3 \).

\[
C_3 = \frac{K_D \cdot K_{VCO}}{N \cdot \omega_n^2} = \frac{(4.77e-5)(9.06e6)}{(1820)(5000)^2} = 0.01\mu F
\]

\[
C_4 = \frac{C_3}{10} = 0.001\mu F
\]

\[
R_3 = \frac{2N\zeta\omega_n}{K_D \cdot K_{VCO}} = \frac{(2)(1820)(1)(5000)}{(4.77e-5)(9.06e6)} = 42.1k\Omega
\]

We choose \( R_3 = 43k\Omega \) for convenience.

6. Notice \( R_2 \) has little effect on the loop filter design. \( R_2 \) should be large, around 100k, and can be adjusted to compensate for any static phase error \( T_\theta \) at lock, but if made too large, will slow loop response. If \( R_2 \) is made smaller, \( T_\theta \) (see timing diagrams) increases, and if \( R_2 \) in-
creases, \( T_\theta \) decreases. For \( \text{LDET} \) to be low at lock, \(|T_\theta| < 50\text{mS}\). \( C_4 \) is used mainly to attenuate high frequency noise from the charge pump. The effect these components have on time to lock is illustrated below.

**Lock Time**

Let \( T = R_3C_3 \). As \( T \) increases, damping increases, but so does lock time. Decreasing \( T \) decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping \((\xi = 1)\) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly over-damped \((\xi > 1)\), trading lock time for increased stability.

### Typical Loop Filter

![Typical Loop Filter Diagram](image)

### LC Loop Filter Components (Approximate)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>( R_2 ) (kΩ)</th>
<th>( R_3 ) (kΩ)</th>
<th>( C_3 ) (μF)</th>
<th>( C_4 ) (μF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>26.602</td>
<td>100</td>
<td>39</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>27.0</td>
<td>100</td>
<td>39</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>29.5</td>
<td>100</td>
<td>43</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>35.468</td>
<td>100</td>
<td>51</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>21.476</td>
<td>100</td>
<td>30</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>24.546</td>
<td>100</td>
<td>36</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>28.636</td>
<td>100</td>
<td>43</td>
<td>0.01</td>
<td>0.001</td>
</tr>
</tbody>
</table>

### Xtal Loop Filter Components (Approximate)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>( R_2 ) (kΩ)</th>
<th>( R_3 ) (MΩ)</th>
<th>( C_3 ) (pF)</th>
<th>( C_4 ) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>26.602</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>27.0</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>29.5</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>35.468</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>21.476</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>24.546</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
<tr>
<td>28.636</td>
<td>100</td>
<td>4.3</td>
<td>68</td>
<td>6.8</td>
</tr>
</tbody>
</table>

**PCB Layout Considerations**

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "hand waving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.
The VCO and loop filter section of the EL4583/4/5 Demo Board can be implemented in the following configurations:

1. **VCXO**

   ![VCXO Diagram]

2. **XTAL**

   ![XTAL Diagram]

3. **LC Tank**

   ![LC Tank Diagram]
Component Sources

Inductors
• Dale Electronics
  E. Highway 50
  PO Box 180
  Yankton, SD 57078-0180
  (605) 665-9301

Crystals, VCXO, VCO Modules
• Connor-Winfield
  2111 Comprehensive Drive
  Aurora, IL 60606
  (708) 851-4722

• Piezo Systems
  100 K Street
  PO Box 619
  Carlisle, PA 17013
  (717) 249-2151

• Reeves-Hoffman
  400 West North Street
  Carlisle, PA 17013
  (717) 243-5929

• SaRonix
  151 Laura Lane
  Palo Alto, CA 94043
  (415) 856-6900

• Standard Crystal
  9940 Baldwin Place
  El Monte, CA 91731
  (818) 443-2121

Varactors
• Alpha Industries
  20 Sylvan Road
  Woburn, MA 01801
  (617) 935-5150

• Motorola Semiconductor Products
  2100 E. Elliot
  Tempe, AZ 85284
  (602) 244-6900

Note: These sources are provided for information purposes only. No endorsement of these companies is implied by this listing.
Communications

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
### Differential Line Driver/Receiver Amplifiers at ±5Vs and ±15Vs

- **EL1501C** Differential Line Driver/Receiver
  - SLIDE™ - ADSL Twisted Pair Line Interface.
- **EL4430/31C** Differential Line Receiver
  - Video on Twisted Pair - ADSL/HDSL Twisted Pair Receiver.
- **EL2140/41C** Differential Line Driver
  - Video or High Speed Data on Twisted Pair - HDSL/ADSL Twisted Pair Driver.
- **EL2142C** Differential Line Receiver
  - Video or High Speed Data on Twisted Pair - HDSL/ADSL Twisted Pair Receiver.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Function</th>
<th>Comments</th>
<th>V_{OUT} diff pk-pk</th>
<th>I_{OUT} pk</th>
<th>THD at V_{OUT}</th>
<th>Bandwidth at 3 dB</th>
<th>Test Gain</th>
<th>Slew Rate</th>
<th>Diff Gain</th>
<th>Diff Phase</th>
<th>Is at ±15V</th>
<th>Supply Voltage Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min pk Typ Typ Typ Typ Typ Typ Typ Typ Min Max</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Up to ±15Vs</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL1501C</td>
<td>Driver</td>
<td>for ADSL</td>
<td>45 V_{p-p}</td>
<td>150 mA</td>
<td>−60 dBc</td>
<td>63 MHz</td>
<td>+10 A_{V}</td>
<td>1000 V/μs</td>
<td>0.17%</td>
<td>0.06°</td>
<td>36 mA</td>
<td>±4.5 V</td>
<td>±16V</td>
</tr>
<tr>
<td></td>
<td>Receiver</td>
<td>Implements Hybrid</td>
<td>22.5 V_{p-p}</td>
<td>31 mA</td>
<td>−72 dBc</td>
<td>80 MHz</td>
<td>−1 A_{V}</td>
<td>600 V/μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EL4430C</strong></td>
<td>Receiver</td>
<td>Good CMRR</td>
<td></td>
<td></td>
<td></td>
<td>82 MHz</td>
<td>+1 A_{V}</td>
<td>380 V/μs</td>
<td>0.02%</td>
<td>0.02°</td>
<td>16 mA</td>
<td>±4.5 V</td>
<td>±16V</td>
</tr>
<tr>
<td><strong>EL4431C</strong></td>
<td>Receiver</td>
<td>Good CMRR</td>
<td></td>
<td></td>
<td></td>
<td>80 MHz</td>
<td>+2 A_{V}</td>
<td>380 V/μs</td>
<td>0.04%</td>
<td>0.08°</td>
<td>16 mA</td>
<td>±4.5 V</td>
<td>±16V</td>
</tr>
<tr>
<td><strong>Up to ±5Vs</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2140C</td>
<td>Driver</td>
<td>Fixed Gain</td>
<td>12 V_{p-p}</td>
<td>50 mA</td>
<td>−75 dBc</td>
<td>150 MHz</td>
<td>+2 A_{V}</td>
<td>800 V/μs</td>
<td>0.24%</td>
<td>0.16°</td>
<td>11 mA</td>
<td>±3 V</td>
<td>±6V</td>
</tr>
<tr>
<td>EL2141C</td>
<td>Driver</td>
<td>Adjustable Gain</td>
<td>12 V_{p-p}</td>
<td>50 mA</td>
<td>−75 dBc</td>
<td>150 MHz</td>
<td>+2 A_{V}</td>
<td>800 V/μs</td>
<td>0.24%</td>
<td>0.16°</td>
<td>11 mA</td>
<td>±3 V</td>
<td>±6V</td>
</tr>
<tr>
<td>EL2142C</td>
<td>Receiver</td>
<td>Match for EL2140/41</td>
<td></td>
<td></td>
<td></td>
<td>150 MHz</td>
<td>+1 A_{V}</td>
<td>400 V/μs</td>
<td>0.2%</td>
<td>0.2°</td>
<td>11 mA</td>
<td>±3 V</td>
<td>±6V</td>
</tr>
</tbody>
</table>

* Subscriber Line Interface DEvice™

**See Amplifier/Buffer Section for datasheet**
Features
- Complete ADSL differential driver and receiver
- 45 Vp-p differential output drive into 200Ω
- −60 dB typical output distortion at full output at 2 MHz
- −73 dB typical receive distortion at 15 Vp-p levels at 2 MHz
- Drives 8 single-ended video loads, or 4 S-VHS loads, or 4 differential video loads
- Power surface-mount package

Applications
- ADSL line interface
- HDSL line driver
- Video distribution amplifier
- Video twisted-pair line driver

General Description
The EL1501C contains two wideband high-voltage drivers and two receive amplifiers. It is designed to drive 45 Vp-p signals at 2 MHz into a 200Ω load differentially with very low distortion. The receive amplifiers also provide very low distortion and noise, and with external resistors can be wired as a hybrid coupler.

All amplifiers are of the current-feedback type, giving high slew rates while consuming moderate power. They retain frequency response over a wide range of externally set gains.

The EL1501C operates on ±5V to ±15V supplies, and retains its bandwidths and linearities over the supply range.

Eight center package pins are used as ground connections and heat spreaders, allowing a dissipation of 2W at the maximum ambient temperature of 85°C.

*Subscriber Line Interface Device
**EL1501C—SLIDE*  
Differential Line Driver/Receiver**

### Absolute Maximum Ratings \( (T_A = 25\,{}^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_S )</td>
<td>( V^+ ) to ( V^- ) Supply Voltage</td>
<td>( 33V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V^+ )</td>
<td>( V^+ ) Voltage to Ground</td>
<td>(-0.3V) to (+33V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V^- )</td>
<td>( V^- ) Voltage to Ground</td>
<td>(-33V) to (0.3V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IN}^+} )</td>
<td>Driver ( V_{\text{IN}^+} ) Voltage</td>
<td>( V^- ) to ( V^+ )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{IN}} )</td>
<td>Current into any Input</td>
<td>8 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OUT}, \text{driver}} )</td>
<td>Output Current from Driver (Static)</td>
<td>75 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OUT}, \text{receiver}} )</td>
<td>Output Current from Receiver (Static)</td>
<td>15 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( P_D )</td>
<td>Maximum Power Dissipation</td>
<td>See Curves</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_A )</td>
<td>Operating Temperature Range</td>
<td>(-40^\circ C) to (+85^\circ C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_S )</td>
<td>Storage Temperature Range</td>
<td>(-60^\circ C) to (+150^\circ C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_F = T_C = T_A \).

**Test Level**
- **I:** 100% production tested and QA sample tested per QA test plan QX0002.
- **II:** 100% production tested at \( T_A = 25^\circ C \) and QA sample tested at \( T_A = 25^\circ C \), \( T_{\text{MAX}} \) and \( T_{\text{MIN}} \) per QA test plan QX0002.
- **III:** QA sample tested per QA test plan QX0002.
- **IV:** Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V:** Parameter is typical value at \( T_A = 25^\circ C \) for information purposes only.

### Open-Loop DC Electrical Characteristics

Power supplies at \( \pm 15V, R_P \) for both drivers and receivers is 1 \( k\Omega \), \( R_L \) for driver is 75\( \Omega \), \( R_L \) for receiver is 200\( \Omega \). \( T_A = 25^\circ C \). Amplifiers tested separately.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{OS}}, \text{driver} )</td>
<td>Driver Input Offset Voltage</td>
<td>(-30)</td>
<td>30</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta V_{\text{OS}}, \text{drivers} )</td>
<td>Driver-to-Driver ( V_{\text{OS}} ) Mismatch</td>
<td>(-10)</td>
<td>10</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{\text{B}}, \text{driver} )</td>
<td>Non-Inverting Driver Input Bias Current</td>
<td>(-10)</td>
<td>10</td>
<td></td>
<td>I</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( I_{\text{B}}, \text{driver} )</td>
<td>Inverting Driver Input Bias Current</td>
<td>(-40)</td>
<td>40</td>
<td></td>
<td>I</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( \Delta I_{\text{B}}, \text{drivers} )</td>
<td>Driver-to-Driver ( I_{\text{B}} ) Mismatch</td>
<td>(-36)</td>
<td>36</td>
<td></td>
<td>I</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( R_{\text{OL}}, \text{drivers} )</td>
<td>Driver Transimpedance, ( V_{\text{OUT}} ) from (-12V) to (+12V)</td>
<td>0.4</td>
<td>1.6</td>
<td></td>
<td>I</td>
<td>M( \Omega )</td>
</tr>
<tr>
<td>( V_{\text{OUT}}, \text{driver} )</td>
<td>Driver Loaded Output Swing</td>
<td>( \pm 12.0)</td>
<td>( \pm 13)</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{OS}}, \text{receiver} )</td>
<td>Receiver Input Offset Voltage</td>
<td>(-30)</td>
<td>30</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta V_{\text{OS}}, \text{receivers} )</td>
<td>Receiver-to-Receiver ( V_{\text{OS}} ) Mismatch</td>
<td>(-10)</td>
<td>10</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{\text{B}}, \text{receiver} )</td>
<td>Receiver Inverting Input Bias Current</td>
<td>(-15)</td>
<td>15</td>
<td></td>
<td>I</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( \Delta I_{\text{B}}, \text{receivers} )</td>
<td>Receiver-to-Receiver ( I_{\text{B}} ) Mismatch</td>
<td>(-16)</td>
<td>16</td>
<td></td>
<td>I</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( R_{\text{OL}}, \text{receiver} )</td>
<td>Receiver Transimpedance, ( V_{\text{OUT}} ) from (-4V) to (+4V)</td>
<td>2</td>
<td>6</td>
<td></td>
<td>I</td>
<td>M( \Omega )</td>
</tr>
<tr>
<td>( V_{\text{OUT}}, \text{receiver} )</td>
<td>Receiver Loaded Output Swing</td>
<td>( \pm 6.25)</td>
<td>( \pm 10)</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( I_S )</td>
<td>All Outputs at 0V</td>
<td>30</td>
<td>36</td>
<td>45</td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>
## Closed-Loop AC Electrical Characteristics

Power supplies at ±15V, $R_F$ for both drivers and receivers is 510Ω, $R_L$ for drivers is 75Ω, $R_L$ for receivers is 200Ω. $C_L = 15$ pF. Driver gain is +10 and receiver gain is −1. $T_A = 25^\circ C$. Amplifiers tested separately.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BW, driver</strong></td>
<td>−3 dB Bandwidth of Driver Amplifiers</td>
<td>63</td>
<td>V</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td><strong>HD, driver</strong></td>
<td>Total Harmonic Distortion of Driver</td>
<td></td>
<td></td>
<td></td>
<td>dBc</td>
<td></td>
</tr>
<tr>
<td>$f = 2$ MHz, Supplies at ±15V, 22.5 Vp-p Output</td>
<td>−60</td>
<td>V</td>
<td>dBc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f = 2$ MHz, Supplies at ±9V, 10.5 Vp-p Output</td>
<td>−66</td>
<td>V</td>
<td>dBc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f = 300$ kHz, Supplies at ±5V, 6 Vp-p Output</td>
<td>−71</td>
<td>V</td>
<td>dBc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>dG, driver</strong></td>
<td>Driver Differential Gain Error, Standard NTSC Test</td>
<td></td>
<td></td>
<td></td>
<td>dBc</td>
<td></td>
</tr>
<tr>
<td>$A_V = +2$, $V_S = ±12V$, $R_L = 37.5$Ω</td>
<td>0.17</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>dθ, driver</strong></td>
<td>Driver Differential Phase Error, Standard NTSC Test</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$A_V = +2$, $V_S = ±12V$, $R_L = 37.5$Ω</td>
<td>0.06</td>
<td>V</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SR, driver</strong></td>
<td>Driver Slewrate, $V_{OUT}$ from −10V to +10V Measured at ±5V</td>
<td>TBD</td>
<td>I</td>
<td>1000</td>
<td>V/μsec</td>
<td></td>
</tr>
<tr>
<td><strong>e_N, driver</strong></td>
<td>Driver Input Noise Voltage</td>
<td>3.3</td>
<td>V</td>
<td></td>
<td>nV/Hz</td>
<td></td>
</tr>
<tr>
<td><strong>i_N, driver</strong></td>
<td>Driver − Input Noise Current</td>
<td>18</td>
<td>V</td>
<td></td>
<td>pA/Hz</td>
<td></td>
</tr>
<tr>
<td><strong>BW, receiver</strong></td>
<td>−3 dB Bandwidth of Receive Amplifiers</td>
<td>80</td>
<td>V</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td><strong>HD, receiver</strong></td>
<td>Total Harmonic Distortion of Receive Amplifiers</td>
<td></td>
<td></td>
<td></td>
<td>dBc</td>
<td></td>
</tr>
<tr>
<td>$f = 2$ MHz, Supplies at ±15V, 11.25 Vp-p Output</td>
<td>−72</td>
<td>V</td>
<td>dBc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f = 2$ MHz, Supplies at ±9V, 5.25 Vp-p Output</td>
<td>−71</td>
<td>V</td>
<td>dBc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f = 300$ kHz, Supplies at ±5V, 3 Vp-p Output</td>
<td>−73</td>
<td>V</td>
<td>dBc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SR, receiver</strong></td>
<td>Receiver Slewrate, $V_{OUT}$ from −4V to +4V Measured at ±2.5V</td>
<td>TBD</td>
<td>I</td>
<td>600</td>
<td>V/μsec</td>
<td></td>
</tr>
<tr>
<td><strong>e_N, receiver</strong></td>
<td>Receiver Input Noise Voltage</td>
<td>3</td>
<td>V</td>
<td></td>
<td>nV/Hz</td>
<td></td>
</tr>
<tr>
<td><strong>i_N, receiver</strong></td>
<td>Receiver − Input Noise Current</td>
<td>12</td>
<td>V</td>
<td></td>
<td>pA/Hz</td>
<td></td>
</tr>
</tbody>
</table>
Test Circuit

Typical Performance Curves

Driver Frequency Response vs $R_F$ at ±15V Supplies

Driver Frequency Response vs $R_F$ at ±9V Supplies

Driver Frequency Response vs $R_F$ at ±5V Supplies
Typical Performance Curves — Contd.

**Driver Frequency Response vs Gain (Non-Inverting)**

- $V_o = \pm 15V$
- $R_f = 510\Omega$
- $R_i = 100\Omega$
- $A_v = 10$
- $A_v = 20$

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>100k</th>
<th>1M</th>
<th>10M</th>
<th>100M</th>
</tr>
</thead>
<tbody>
<tr>
<td>100k</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
<tr>
<td>1M</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
<tr>
<td>10M</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
<tr>
<td>100M</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
</tbody>
</table>

**Driver Frequency Response vs Gain (Inverting)**

- $V_o = \pm 15V$
- $R_f = 510\Omega$
- $R_i = 100\Omega$
- $A_v = 10$
- $A_v = 20$

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>100k</th>
<th>1M</th>
<th>10M</th>
<th>100M</th>
</tr>
</thead>
<tbody>
<tr>
<td>100k</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
<tr>
<td>1M</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
<tr>
<td>10M</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
<tr>
<td>100M</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-1</td>
</tr>
</tbody>
</table>

**Driver Bandwidth vs Temperature**

- $A_v = 10$
- $R_f = 510\Omega$
- $R_i = 100\Omega$

<table>
<thead>
<tr>
<th>Die Temperature (°C)</th>
<th>25</th>
<th>50</th>
<th>75</th>
<th>100</th>
<th>125</th>
<th>150</th>
</tr>
</thead>
<tbody>
<tr>
<td>Change in Bandwidth (%)</td>
<td>-20</td>
<td>-15</td>
<td>-10</td>
<td>-5</td>
<td>0</td>
<td>5</td>
</tr>
</tbody>
</table>

**Driver Harmonic Distortion vs Frequency (Single Amplifier)**

- $V_o = 6V_{pp}$
- $V_o = 0V_{pp}$

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
<th>10</th>
<th>12</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
<th>22</th>
<th>24</th>
<th>26</th>
</tr>
</thead>
</table>

**Driver Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)**

- $V_o = 12V_{pp}$
- $V_o = 6V_{pp}$

<table>
<thead>
<tr>
<th>Output Amplitude (V_{pp})</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
<th>10</th>
<th>12</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
<th>22</th>
<th>24</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Harmonic Distortion (dBc)</td>
<td>-80</td>
<td>-75</td>
<td>-70</td>
<td>-65</td>
<td>-60</td>
<td>-55</td>
<td>-50</td>
<td>-45</td>
<td>-40</td>
<td>-35</td>
<td>-30</td>
<td>-25</td>
<td>-20</td>
</tr>
</tbody>
</table>

**Driver Differential Gain Error vs DC Input Offset**

- $A_v = 1$ (Single Amplifier)

<table>
<thead>
<tr>
<th>Gain (dB)</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$, DC (V)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

**Driver Differential Phase Error vs DC Input Offset**

- Gain = $1$

<table>
<thead>
<tr>
<th>Differential Phase Error (%)</th>
<th>-0.8</th>
<th>-0.6</th>
<th>0</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$, DC (V)</td>
<td>-0.8</td>
<td>-0.6</td>
<td>0</td>
<td>0.2</td>
<td>0.4</td>
<td>0.6</td>
<td>0.8</td>
</tr>
</tbody>
</table>
Typical Performance Curves — Contd.

**Driver Input Noise Voltage and Current over Frequency**

- Voltage: $V_{in}$
- Current: $I_{in}$

**Driver Differential Gain Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2**

**Driver Differential Phase Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2**

**Receive Amplifier Frequency Response at $V_S = \pm 15V$**

- $A_V = -111$
- $R_c = 200\Omega$
- $R_e = 450\Omega$
- $R_e = 510\Omega$
- $R_e = 680\Omega$

**Receive Amplifier Frequency Response at $V_S = \pm 5V$**

- $A_V = -111$
- $R_c = 200\Omega$
- $R_e = 450\Omega$
- $R_e = 510\Omega$
- $R_e = 680\Omega$

**Receive Amplifier Harmonic Distortion vs Frequency (Single Amplifier)**

- $V_{out} = 3V_{in}$
- $V_{out} = 6V_{in}$
- $V_{out} = 9V_{in}$

**Receive Amplifier Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)**

- $V_{out} = 4.5V$
- $V_{out} = 8.9V$
- $V_{out} = 11V_{in}$
Applications Information

The EL1501C consists of two power line drivers and two receiver amplifiers that can be connected for full duplex differential line transmission and reception. The amplifiers are designed to be used with signals up to 4 MHz and produce low distortion levels. Here is a typical interface circuit:

![Typical Line Interface Connections](image-url)
Applications Information — Contd.
The drive amplifiers are wired one in positive gain and the other in negative gain configurations to generate a differential output for a single-ended input. The drivers will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers $R_F$'s need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver. The Typical Performance Curves section of this data sheet has a plot of driver responses matched at gains of +1 and -1 using feedback resistors of 910Ω and 750Ω, respectively.

The receiver amplifiers are wired as a hybrid coupler in the circuit. They reject the drivers' output signal (to the matching accuracy of the line impedance and resistors) while passing the signal coming from the line. Their outputs are still differential signals and can be converted to single-ended form by using a wideband instrumentation amplifier such as the EL4430. In a simplistic analysis we set $R_{OUT} = Z_{LINE}/2$ and $R' = 2* R_{IN'}$. Signals coming in from the line convert to currents through the $R_{IN}$'s and pass through the receive amplifiers. Driver outputs pass through the $R'$ resistors and produce signal currents, but they are cancelled by opposite-polarity currents through the $R_{IN'}$ resistors.

The actual value of $R_{OUT}$ is increased from $Z_{LINE}/2$ to make its value in parallel $R_{IN'}$ equal $Z_{LINE}/2$ and better match the line. For proper hybrid balance, $R'$ is increased to compensate for $R_{OUT}$'s adjustment. For $Z_{LINE} = 130Ω$ and $R_{IN'} = 510Ω$, we set $R_{OUT} = 74.5Ω$ and $R' = 1.17 \, kΩ$.

For operating frequencies below 1 MHz, or in cases where the hybrid rejection of the drive signal is not very critical, the receive amplifiers can be wired to provide a single-ended hybrid coupler output:

Receive Amplifiers Providing Hybrid and Differential Conversion
Applications Information — Contd.

Common-mode rejection is as good as resistor and line impedance match, as before, but there is a 4 ns time mismatch due to cascading the receive amplifiers. Thus, rejection of common-mode interference will degrade above 1 MHz.

If the receiver amplifiers are not used, their inputs and outputs may simply be left open. This will reduce power consumption by 2 mA per amplifier.

If a differential signal is available to the drive amplifiers, they may be wired so:

![Diagram of amplifier connections]

Drivers Wired for Differential Input

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The receiver amplifiers are not sensitive to source impedances, since they are wired for inverting gain. The drivers are somewhat sensitive to source impedance, however. In particular, they do not like being driven by inductive sources. More than 100 nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4" of unshielded wiring, or 6" of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Resistive sources greater than 2 kΩ will cause the driver to exhibit increased harmonic distortion. Most amplifier output stages are much lower in impedance and give no problem.

Power Supplies

The EL1501C works well over the ±5V to ±15V supply range. Frequency response varies only slightly, and output drive capability is constant. The major supply voltage issue is power dissipation. The internal dissipation \( P_D \) for an EL1501C running on supply voltages of \( \pm V_S \) and delivering a DC output voltage \( V_O \) into a load of \( R_L \) is

\[
P_D = 2 \times V_S \times I_S + \sum (V_S - V_O) \times V_O / R_L
\]

where the \( \Sigma \) indicates that all four amplifiers can produce dissipation by each driving a load. If outputs are sinusoidal signals of \( V_O \) volts per amplifier peak-to-peak rather than DC the dissipation is

\[
P_D = 2 \times V_S \times I_S + \frac{\sqrt{V_S^2 - V_O^2}}{8} - \frac{V_S \times V_O}{3\pi} + \frac{3 \times V_O}{128} \frac{R_L}{R_L}
\]

Formula 1

As a worst-case example, assume the drivers are running on ±15.75V supplies, each delivering 19.4 V\(_{\text{p-p}}\) outputs into 119Ω (the parallel of resistors the driver in the first schematic would see), and quiescent supply current \( I_S \) is the maximum 43 mA, and is substantially constant over temperature. The quiescent dissipation (the first term of the equation) is 1.42W, and each driver adds 0.44W, for a total of 2.24W dissipation. The 19.4 V\(_{\text{p-p}}\) output level was chosen to produce the maximum internal dissipation: that is, \( V_O = 1.234 \times V_S \) is the most dissipative output level.

The power supplies should be well bypassed close to the EL1501C. 3.3 μF tantalum capacitors work well. Since the load currents are differential, they need not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no ground loops will occur. This scheme is employed in the layout of the EL1501C demonstration board, and documentation can be obtained from the factory.
Heat-Sinking
To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreading and convecting to air. Thus, the ground plane on the component side of the board becomes the heatsink for the EL1501C. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, $\theta_{JM}$, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask can be cut away from the EL1501C to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

The package will exhibit a $\theta_{JM}$ of $80^\circ C/W$ with no assistance from circuit board heatsinks. This will suffice for the lowest supply voltages and output levels. The best $\theta_{JM}$ that can be obtained is about $30^\circ C/W$, and a practical layout would produce $43^\circ C/W$. More detail is available from the Elantec application note *Measuring the Thermal Resistance of Power Surface-Mount Packages*. This plot summarizes the note’s results:

For a given $\theta_{JM}$, the maximum $P_D$ is

$$P_D = (T_{MAX} - T_A)\theta_{JM},$$

where $T_{MAX} = 150^\circ C$, the maximum die temperature in a plastic package, and $T_A$ is the ambient air temperature.
Output Loading
While the drive amplifiers can output in excess of 250 mA, the internal metallization is not designed to carry more than 75 mA of steady DC current and there is no current-limit mechanism. This allows safely driving peak sinusoidal currents of $\pi \times 75$ mA, or 236 mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25 pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Feedback Resistor Value
The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The receive amplifiers are connected in inverting mode and will produce a narrow range of characteristics, but the drives can be used for a wide range of gains. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1 dB peaking) for different supply voltages and gains:

**Optimum Driver Feedback Resistor for Various Gains and Supply Voltages**

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>-1</th>
<th>+1</th>
<th>2.5</th>
<th>5</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>±5V</td>
<td>750Ω</td>
<td>910Ω</td>
<td>750Ω</td>
<td>680Ω</td>
<td>620Ω</td>
</tr>
<tr>
<td>±9V</td>
<td>680Ω</td>
<td>820Ω</td>
<td>680Ω</td>
<td>620Ω</td>
<td>510Ω</td>
</tr>
<tr>
<td>±15V</td>
<td>620Ω</td>
<td>750Ω</td>
<td>620Ω</td>
<td>510Ω</td>
<td>470Ω</td>
</tr>
</tbody>
</table>

Driving Video Loads
Each driver amplifier can drive four doubly-terminated video loads while operating on ±5V supplies. Larger supply voltages slightly improve differential gain and phase distortions, which are around 0.2% and 0.1° for single-ended outputs with the standard NTSC test. Differential-output distortion drops to 0.09% and 0.08°.
Applications Hint. Pins 4, 5, 6, 7, 14, 15, 16 & 17 must be connected to ground (node 0) for proper operation. Use resistors whose value is \(10^{-6}\) ohms.

**Connections:**

* \(V_{IN}^-, DR^+\)
* \(V_{OUT}, DR^+\)
* \(V_-\)
* \(V_{OUT}, DR^-\)
* \(V_{IN}^+, DR^+\)
* \(V_{OUT}, Rcvr^+\)
* \(V_{IN}^-, Rcvr^-\)

**Driver + (Amplifier A)**

*e1a 30 0 8 0 1.0
visa 30 43 0V
h2a 43 44 v1a 1.0
r1a 1 45 25
i1a 45 44 2.5nH
i1a 8 0 1\(\mu\)A
i2a 1 0 5\(\mu\)A
h1a 46 0 visa 600
r2a 46 31 1K
d1a 31 0 dclamp
d2a 0 31 dclamp
e2a 32 0 31 0 0.0016666
**EL1501 Macromodel — Contd.**

```
13a 32 33 0.5µH
c1a 33 0 1pF
r5a 33 0 200
g1a 0 34 33 0 1.0
ro1a 34 0 2Meg
c2a 34 0 3pF
q1a 3 34 35 qp
q2a 18 34 36 qn
q3a 18 35 37 qn
q4a 3 36 38 qp
r7a 37 2 2
r8a 38 2 2
i3a 18 35 3.3mA
i4a 36 3 3.3mA
ivosa 0 42 2mA
v1a 42 0 0V
```

*Driver — (Amplifier B)*

```
e1b 50 0 13 0 1.0
v1sb 50 63 0V
h2b 63 64 v1b 1.0
r1b 20 65 25
l1b 65 64 2.5nH
i1b 13 0 1µA
l2b 20 0 5µa
h1b 60 0 v1b 600
r2b 66 51 1K
d1b 51 0 dclamp
d2b 0 51 dclamp
e2b 52 0 51 0 0.0016666
i3b 52 53 0.5µH
c1b 53 0 1pF
r5b 53 0 200
g1b 0 54 53 0 1.0
ro1b 54 0 2Meg
c2b 54 0 3pF
q1b 3 54 55 qp
q2b 18 54 56 qn
q3b 18 55 57 qn
q4b 3 56 58 qp
r7b 57 19 2
r8b 58 19 2
i3b 18 55 3.3mA
i4b 56 3 3.3mA
ivosb 0 62 2mA
v1b 62 0 0V
```
**********

*Receiver + (Amplifier C)*

* 

rpin1 4 5 1e-6
rpin2 5 6 1e-6
rpin3 6 7 1e-6
rpin4 7 14 1e-6
e1c 70 0 7 0 1.0
visc 70 83 0V
h2c 83 84 v1b 1.0
rlc 10 85 25
l1c 85 84 2.5nH
i1c 70 0 1µA
i2c 10 0 5µA
h1c 85 0 visc 600
r2c 86 71 1K
d1c 71 0 dclamp
d2c 0 71 dclamp
e2c 72 0 71 0 0.0016666
l3c 72 73 0.5µH
c1c 73 0 1pF
r5c 73 0 200
g1c 0 74 73 0 1.0
rolc 74 0 2Meg
c2c 74 0 4.1pF
q1c 3 74 75 qP
q2c 18 74 76 qn
q3c 18 75 77 qn
q4c 3 76 78 qP
r7c 77 9 2
r8c 78 9 2
i3c 18 75 3.3mA
14c 76 3 3.3mA
ivosc 0 82 2mA
v1c 82 0 0V

**********

*Receiver - (Amplifier D)*

* 

rpin5 17 16 1e-6
rpin6 16 15 1e-6
rpin7 15 14 1e-6
e1d 90 0 14 0 1.0
visd 90 103 0v
h2d 103 104 v1d 1.0
rlc 11 105 25
l1d 105 104 2.5nH
i1d 7 0 1µA
i2d 11 0 5µA
hld 106 0 visd 600
r2d 106 91 1K

**********
EL1501 Macromodel — Contd.

d1d 91 0 dclamp
d2d 0 91 dclamp
e2d 92 0 91 0.0016666
l3d 92 93 0.5µH
cld 93 0 1pF
r5d 93 0 200
gld 0 94 93 0 1.0
rold 94 0 2Meg
c2d 94 0 4.1pF
qld 3 94 95 qp
q2d 18 94 96 qn
q3d 18 95 97 qn
q4d 3 96 98 qp
r7d 97 12 2
r8d 98 12 2
l3d 18 95 3.3mA
l4d 96 3 3.3mA
ivosd 0 102 2mA
vld 102 0 0V

* Model

.model qn npn(is = 5e-15 bf = 350 tf = 0.1nS)
.model qp pnp(is = 5e-15 bf = 350 tf = 0.1nS)
.model dclamp d(is = le-30 ibv = 0.266 bv = 1.9 n = 4)
.ends
**Features**
- Fully differential inputs, outputs, and feedback
- Differential input range ±2.3V
- 150 MHz 3 dB bandwidth
- 800 V/μs slew rate
- −55 dB distortion at 3 MHz
- −75 dB distortion at 100 kHz
- ±5V supplies or +6V single supply
- 50 mA minimum output current
- Output swing (200Ω load) to within 1.5V of supplies (14V pk-pk differential)
- Low power-11 mA typical supply current

**Applications**
- Twisted pair driver
- Differential line driver
- VGA over twisted pair
- ADSL/HDSL driver
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2140CN</td>
<td>−40°C to +85°C</td>
<td>8-pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2140CS</td>
<td>−40°C to +85°C</td>
<td>8-pin SSIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL2141CN</td>
<td>−40°C to +85°C</td>
<td>8-pin PDIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2141CS</td>
<td>−40°C to +85°C</td>
<td>8-pin SSIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

**General Description**

The EL2140C/2141C is a very high bandwidth amplifier whose output is in differential form, and is thus primarily targeted for applications such as driving twisted pair lines, or any application where common mode injection is likely to occur. The input signal can be in either single-ended or differential form, but the output is always in differential form.

On the EL2141C, two feedback inputs provide the user with the ability to set the device gain, (stable at minimum gain of two), whereas the EL2140C comes with a fixed gain of two.

The output common mode level is set by the reference pin (VREF), which has a −3 dB bandwidth of over 100 MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The transmission of ADSL/HDSL signals requires very low distortion amplification, so this amplifier was designed with this as a primary goal. The actual signal distortion levels depend upon input and output signal amplitude, as well as the output load impedance. (See distortion data inside.)

Both outputs (VOUT, VOUTB) are short circuit protected to withstand temporary overload condition.

**Connection Diagrams**
**Absolute Maximum Ratings**

Supply Voltage ($V_{CC} - V_{EE}$): 0V–12.6V

Maximum Output Current: $\pm 60 \text{ mA}$

Storage Temperature Range: $-65^\circ\text{C to } +150^\circ\text{C}$

Operating Junction Temperature: $-65^\circ\text{C to } +150^\circ\text{C}$

**Recommended Operating Temperature**

$V_{IN}, V_{INB}, V_{REF} = V_{EE} + 0.8\text{V (MIN) to } V_{CC} - 0.8\text{V (MAX)}$

$V_{IN} - V_{INB} = \pm 5\text{V}$

**DC Electrical Characteristics**

$V_{CC} = +5\text{V}, V_{EE} = -5\text{V}, T_A = 25^\circ\text{C}, V_{IN} = 0\text{V}, R_L = 200$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{supply}$</td>
<td>Supply Operating Range ($V_{CC} - V_{EE}$)</td>
<td>$\pm 3.0$</td>
<td>$\pm 5.0$</td>
<td>$\pm 6.3$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Power Supply Current (No Load)</td>
<td>11</td>
<td>14</td>
<td>mA</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Input Referred Offset Voltage</td>
<td>$-25$</td>
<td>10</td>
<td>40</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Bias Current ($V_{IN}, V_{INB}, V_{REF}$)</td>
<td>$-20$</td>
<td>6</td>
<td>20</td>
<td>I</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$Z_{IN}$</td>
<td>Differential Input Impedance</td>
<td>400</td>
<td></td>
<td></td>
<td>V</td>
<td>$\text{k}\Omega$</td>
</tr>
<tr>
<td>$V_{DIFF}$</td>
<td>Differential Input Range</td>
<td>$\pm 2.0$</td>
<td>$\pm 2.3$</td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>$A_V$</td>
<td>Voltage Gain (EL2140C) $V_{IN} = 2V_{pk-pk}$</td>
<td>1.95</td>
<td>1.985</td>
<td>2.02</td>
<td>I</td>
<td>V/V</td>
</tr>
<tr>
<td>$A_{VOL}$</td>
<td>Open Loop Voltage Gain (EL2141C)</td>
<td>75</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Input Common Mode Voltage Range (EL2140C)</td>
<td>$-2.6$</td>
<td></td>
<td>$+4.0$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT(200)}$</td>
<td>Output Voltage Swing (200$\Omega$ load, $V_{OUT}$ to $V_{OUTB}$) (EL2141C)</td>
<td>$\pm 3.4$</td>
<td>$\pm 3.6$</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT(100)}$</td>
<td>Output Voltage Swing (100$\Omega$ Load, $V_{OUT}$ to $V_{OUTB}$) (EL2141C)</td>
<td>$\pm 2.9$</td>
<td>$\pm 3.1$</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{N}$</td>
<td>Input Referred Voltage Noise</td>
<td>36</td>
<td></td>
<td></td>
<td>V</td>
<td>nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Output Voltage Control Range (EL2140C)</td>
<td>$-2.5$</td>
<td></td>
<td>$+3.3$</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{REFOS}$</td>
<td>Output Offset Relative to $V_{REF}$</td>
<td>$-60$</td>
<td>$-25$</td>
<td>$+60$</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
<td>60</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>$I_{OUT(min)}$</td>
<td>Minimum Output Current</td>
<td>50</td>
<td>60</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Input Common Mode Rejection Ratio (EL2140C) $V_{CM} = \pm 2\text{V}$</td>
<td>60</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>$R_{OUT}$</td>
<td>$(V_{OUT} - V_{OUTB} = 0\text{V})$ Output Impedance</td>
<td>0.1</td>
<td></td>
<td></td>
<td>V</td>
<td>$\Omega$</td>
</tr>
</tbody>
</table>
# EL2140C/2141C

## 150 MHz Differential Twisted Pair Driver

### AC Electrical Characteristics

\( V_{CC} = +5V, \ V_{EE} = -5V, \ T_A = 25^\circ C, \ V_{IN} = 0V, \ R_{LOAD} = 200 \), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW((-3\ dB))</td>
<td>-3 dB Bandwidth (EL2140C and EL2141C @ gain of 2)</td>
<td>150</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Differential Slewrate</td>
<td>800</td>
<td></td>
<td></td>
<td>V</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>Tstl</td>
<td>Settling Time to 1%</td>
<td>15</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth Product</td>
<td>400</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>(V_{REFBW}(-3\ dB))</td>
<td>(V_{REF}) -3 dB Bandwidth</td>
<td>130</td>
<td></td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>(V_{REFSR})</td>
<td>(V_{REF}) Slewrate</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>THDF1</td>
<td>Distortion at 100 kHz (Note 1)</td>
<td>-75</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>dP</td>
<td>Differential Phase @ 3.58 MHz</td>
<td>0.16</td>
<td></td>
<td></td>
<td>V</td>
<td>(^\circ)</td>
</tr>
<tr>
<td>dG</td>
<td>Differential Gain @ 3.58 MHz</td>
<td>0.24</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
</tbody>
</table>

Note 1: Distortion measurement quoted for \(V_{OUT}-V_{OUTB}\) = 12V pk-pk, \(R_{LOAD}\) = 200\(\Omega\), \(V_{gain}\) = 8.

### Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 (V_{IN})</td>
<td>Non-inverting Input</td>
</tr>
<tr>
<td>3</td>
<td>1 (V_{INB})</td>
<td>Inverting Input (EL2140C only)</td>
</tr>
<tr>
<td>4</td>
<td>4 (FBN)</td>
<td>Inverting Feedback Input. Resistor R3 must be Connected from this Pin to (V_{OUTB}) (EL2141C only)</td>
</tr>
<tr>
<td>4</td>
<td>3 (V_{REF})</td>
<td>Non-inverting Feedback Input. Resistor R1 must be Connected from this Pin to (V_{OUT}) (EL2140C only)</td>
</tr>
<tr>
<td>5</td>
<td>5 (V_{OUTB})</td>
<td>Inverting Output</td>
</tr>
<tr>
<td>6</td>
<td>6 (V_{CC})</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>7</td>
<td>7 (V_{EE})</td>
<td>Negative Supply</td>
</tr>
<tr>
<td>8</td>
<td>8 (V_{OUT})</td>
<td>Non-inverting Output</td>
</tr>
</tbody>
</table>
Typical Performance Curves

**IS vs Supply Voltage**

![Graph showing IS vs Supply Voltage](image)

**EL2140 Frequency Response**

![Graph showing EL2140 Frequency Response](image)

**EL2141 Frequency Response vs Resistor R2 (GAIN = 2)**

![Graph showing EL2141 Frequency Response vs Resistor R2](image)

**Frequency Response vs Temperature**

![Graph showing Frequency Response vs Temperature](image)

**EL2141 Frequency Response vs Resistor R2 (GAIN = 8)**

![Graph showing EL2141 Frequency Response vs Resistor R2](image)

**EL2141 Distortion vs Frequency (GAIN = 6, RLOAD = 200Ω) VIN = 2V pk/pk**

![Graph showing EL2141 Distortion vs Frequency](image)
Typical Performance Curves — Contd.

**EL2140 CMRR vs Frequency**

**EL2141 Output Signal and Common Mode Signal vs Frequency**

**EL2140 VREF Frequency Response**

**EL2140 Small Signal Response (Note 1)**

Note 1: Photo shows voltages on a 100 Ω transmission line terminated at both ends, so voltages at $V_{OUT}$, $V_{OUTB}$ are twice the values shown.
Applications Information

**Choice of feedback resistor**

There is little to be gained from choosing resistor R2 values below 400Ω and, in fact, it would only result in increased power dissipation and signal distortion. Above 400Ω, the bandwidth response will develop some peaking (for a gain of two), but substantially higher resistor R2 values may be used for higher voltage gains, such as up to 2 kΩ at a gain of eight before peaking will develop. R1 and R3 are selected as needed to set the voltage gain, and while R1 = R3 is suggested, the gain equation above holds for any values (see distortion for further suggestions).

**Capacitance considerations**

As with many high bandwidth amplifiers, the EL2140C/2141C prefer not to drive highly capacitive loads. It is best if the capacitance on VOUT and VOUTB is kept below 10 pF if the user does not want gain peaking to develop.

In addition, on the EL2141C, the two feedback nodes FBP and FBN should be laid out so as to minimize stray capacitance, else an additional pole will potentially develop in the response with possible gain peaking.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

**Distortion considerations**

The harmonics that these amplifiers will potentially produce are the 2nd, 3rd, 5th, and 6th. Their amplitude is application dependent. All other harmonics should be negligible by comparison. Each should be considered separately:

- **H2** The second harmonic arises from the input stage, and the lower the applied differential signal amplitude, the lower the magnitude of the second harmonic. For practical considerations of required output signal and input noise levels, the user will end up choosing a circuit gain. Referring to Figure 1, it is best if the voltage at the negative feedback node tracks the VREF node, and the voltage at the positive feedback node tracks the VIN node respectively. This would theoretically require that R1 + R2 = R3, although the lowest distortion is found at about R3 = R1 + (0.7*R2). With this arrangement, the second harmonic should be suppressed well below the value of the third harmonic.
Applications Information — Contd.

H3 The third harmonic should be the dominant harmonic and is primarily affected by output load current which, of course, is unavoidable. However, this should encourage the user not to waste current in the gain setting resistors, and to use values that consume only a small proportion of the load current, so long as peaking does not occur. The more load current, the worse the distortion, but depending on the frequency, it may be possible to reduce the amplifier gain so that there is more internal gain left to cancel out any distortion.

H5 The fifth harmonic should always be below the third, and will not become significant until heavy load currents are drawn. Generally, it should respond to the same efforts applied to reducing the third harmonic.

H6 The sixth harmonic should not be a problem and is the result of poor power supply decoupling. While 100 nF chip capacitors may be sufficient for some applications, it would be insufficient for driving full signal swings into a twisted pair line at 100 kHz. Under these conditions, the addition of 4.7 μF tantalum capacitors would cure the problem.

Typical Applications Circuits

![Diagram of a typical twisted pair application](image)

Figure 1. Typical Twisted Pair Application
Typical Applications Circuits — Contd.

Figure 2. Dual Coaxial Cable Driver

Figure 3. Single Supply Twisted Pair Driver
Figure 4. Differential Line Driver with Equalization

DC Gain = \( \frac{R_1 + R_2 + R_3}{R_2} \) (See Figure 5)

HF Gain = \( \frac{R_1 + \frac{R_2}{R_4} + R_3}{\frac{R_2}{R_4}} \) (See Figure 5)

where \( f_0 = \frac{1}{2 \pi C_1 R_2} \)

and \( f_p = \frac{1}{2 \pi C_1 R_4} \)
Typical Applications Circuits — Contd.

Figure 6. Dual Signal Transmission Circuit
Features
- Differential input range ±2.3V
- 150 MHz 3 dB bandwidth
- 400 V/μs slew rate
- ±5V supplies or single supply
- 50 mA minimum output current
- Output swing (100Ω load) to within 1.5V of supplies
- Low power −11 mA typical

Applications
- Twisted pair receiver
- Differential line receiver
- VGA over twisted pair
- ADSL/HDSL receiver
- Differential to single ended amplification.
- Reception of analog signals in a noisy environment.

General Description
The EL2142C is a very high bandwidth amplifier designed to extract the difference signal from noisy environments, and is thus primarily targeted for applications such as receiving signals from twisted pair lines, or any application where common mode noise injection is likely to occur.

The EL2142C is stable for a gain of one, and requires two external resistors to set the voltage gain.

The output common mode level is set by the reference pin (VREF), which has a −3 dB bandwidth of over 100 MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The output can deliver a minimum of ±50 mA and is short circuit protected to withstand a temporary overload condition.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2142CN</td>
<td>−40°C to +85°C</td>
<td>8-pin DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2142CS</td>
<td>−40°C to +85°C</td>
<td>8-pin SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagrams

EL2142C SO, P-DIP
### Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min to Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ((V_{CC} - V_{EE}))</td>
<td>0V to 12.6V</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>±60 mA</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics

\((V_{CC} = +5V, \ V_{EE} = -5V, \ T_A = 25C, \ V_{IN} = 0V, \ R_L = 100, \) unless otherwise specified)\\

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{supply})</td>
<td>Supply Operating Range ((V_{CC} - V_{EE}))</td>
<td>±3.0</td>
<td>±5.0</td>
<td>±6.3</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_S)</td>
<td>Power Supply Current (no load)</td>
<td>11</td>
<td>14</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(V_{OS})</td>
<td>Input Referred Offset Voltage</td>
<td>-25</td>
<td>10</td>
<td>40</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(I_{IN})</td>
<td>Input Bias Current ((V_{IN}, \ V_{INB}, V_{REF}))</td>
<td>-20</td>
<td>6</td>
<td>20</td>
<td>I</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(Z_{IN})</td>
<td>Differential Input Resistance</td>
<td>400</td>
<td></td>
<td></td>
<td>V</td>
<td>K\Omega</td>
</tr>
<tr>
<td>(C_{IN})</td>
<td>Differential Input Capacitance</td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td>(V_{DIFF})</td>
<td>Differential Input Range</td>
<td>±2.0</td>
<td>±2.3</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(A_{VOL})</td>
<td>Open Loop Voltage Gain</td>
<td>75</td>
<td></td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Input Common Mode Voltage Range</td>
<td>-2.6</td>
<td></td>
<td>+4.0</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OUT})</td>
<td>Output Voltage Swing ((50\Omega) to GND)</td>
<td>±2.9</td>
<td>±3.1</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_{OUT (min)})</td>
<td>Minimum Output Current</td>
<td>50</td>
<td>60</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Input Referred Voltage Noise</td>
<td>36</td>
<td></td>
<td></td>
<td>V</td>
<td>nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>(V_{REF})</td>
<td>Output Voltage Control Range</td>
<td>-2.5</td>
<td></td>
<td>+3.3</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio</td>
<td>60</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(CMRR2)</td>
<td>Input Common Mode Rejection Ratio ((V_{IN} = ±2V))</td>
<td>60</td>
<td>70</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
<tr>
<td>(CMRR1)</td>
<td>Input Common Mode Rejection Ratio ()</td>
<td>50</td>
<td>60</td>
<td></td>
<td>I</td>
<td>dB</td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

\( V_{CC} = +5V, V_{EE} = -5V, T_A = 25C, V_{IN} = 0V, R_{LOAD} = 100 \), unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( BW(-3dB) )</td>
<td>(-3) dB Bandwidth (Gain = 1)</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( SR )</td>
<td>Slewrate</td>
<td></td>
<td>400</td>
<td></td>
<td></td>
<td>( V/\mu s )</td>
</tr>
<tr>
<td>( T_{stl} )</td>
<td>Settling time to 1%</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>GBWP</td>
<td>Gain bandwidth product</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( V_{REFBW}(-3)dB) )</td>
<td>( V_{REF} ) (-3dB) Bandwidth</td>
<td></td>
<td>130</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( V_{REFSR} )</td>
<td>( V_{REF} ) Slewrate</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>( V/\mu sec )</td>
</tr>
<tr>
<td>( dG )</td>
<td>Differential gain at 3.58 MHz.</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td>( % )</td>
</tr>
<tr>
<td>( d\theta )</td>
<td>Differential phase at 3.58 MHz.</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td>( % )</td>
</tr>
</tbody>
</table>

### Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( V_{FB} )</td>
<td>Feedback input</td>
</tr>
<tr>
<td>2</td>
<td>( V_{IN} )</td>
<td>Non-inverting input</td>
</tr>
<tr>
<td>3</td>
<td>( V_{INB} )</td>
<td>Inverting input</td>
</tr>
<tr>
<td>4</td>
<td>( V_{REF} )</td>
<td>Sets output voltage level to ( V_{REF} ) when ( V_{IN} = V_{INB} )</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>( V_{CC} )</td>
<td>Positive supply voltage</td>
</tr>
<tr>
<td>7</td>
<td>( V_{EE} )</td>
<td>Negative supply voltage</td>
</tr>
<tr>
<td>8</td>
<td>( V_{OUT} )</td>
<td>Output voltage</td>
</tr>
</tbody>
</table>
Typical Performance Curves

- **I₅ vs Supply Voltage**
  - Graph showing current (I₅) versus supply voltage (V CC - V EE) with multiple curves indicating different current values.

- **Frequency Response**
  - Graph showing gain versus frequency for different resistor values (R1).
  - Three curves for R1 = 100Ω, 300Ω, and 1000Ω.

- **CMRR vs Frequency**
  - Graph showing CMRR (common-mode rejection ratio) versus frequency with multiple curves indicating different resistor values (R2).

- **Distortion vs Frequency**
  - Graph showing Total Harmonic Distortion (THD) versus frequency with a label indicating gain and load conditions.
  - THD values range from -30 to -80 dB.
Applications Information

Gain Equation
\[ V_{OUT} = \left( \frac{R_2 + R_1}{R_1} \right) \times (V_{IN} - V_{INB} + V_{REF}) \text{ when } R_1 \text{ tied to } GND \]
\[ V_{OUT} = \left( \frac{R_2 + R_1}{R_1} \right) \times (V_{IN} - V_{INB}) \text{ when } R_1 \text{ tied to } V_{REF} \]

Choice of Feedback Resistor
For a gain of one, \( V_{OUT} \) may be shorted back to \( V_{FB} \), but 100\( \Omega \)-200\( \Omega \) improves the bandwidth. For gains greater than one, there is little to be gained from choosing resistor \( R_1 \) value below 200\( \Omega \), for it would only result in increased power dissipation and potential signal distortion. Above 200\( \Omega \), the bandwidth response will develop some peaking (for a gain of one), but substantially higher \( R_1 \) values may be used for higher voltage gains, such as up to 1 k\( \Omega \) at a gain of four before peaking will develop.

Capacitance Considerations
As with many high bandwidth amplifiers, the EL2142C prefers not to drive highly capacitive loads. It is best if the capacitance on \( V_{OUT} \) is kept below 10 pF if the user does not want gain peaking to develop. The \( V_{FB} \) node forms a potential pole in the feedback loop, so capacitance should be minimized on this node for maximum bandwidth.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.
Typical Applications

Figure 1. Typical Twisted Pair Application

Figure 2. Coaxial Cable Driver
Typical Applications — Contd.

Figure 3. Single Supply Receiver

Figure 4. Compensated Line Receiver
Figure 5. Two Channel Multiplexer
# Power MOSFET Driver

<table>
<thead>
<tr>
<th>Single</th>
<th>Dual</th>
<th>Features</th>
<th>Ipeak</th>
<th>$R_{ON}$</th>
<th>$T_{r}/T_{f}$</th>
<th>$V_{SUPPLY}$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7104C</td>
<td></td>
<td>Non-Inverting</td>
<td>4A</td>
<td>3Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7114C</td>
<td></td>
<td>Inverting/Iso-Drains</td>
<td>4A</td>
<td>3Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>*EL7134C</td>
<td></td>
<td>3-State</td>
<td>4A</td>
<td>3Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7144C</td>
<td></td>
<td>2-Input Logic AND</td>
<td>4A</td>
<td>3Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
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<td>Non-Inverting</td>
<td>2A</td>
<td>6Ω</td>
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<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7212C</td>
<td></td>
<td>Inverting</td>
<td>2A</td>
<td>6Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7222C</td>
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<td>Complimentary Output</td>
<td>2A</td>
<td>6Ω</td>
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<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
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<td>3-State</td>
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<td>6Ω</td>
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<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL7242C</td>
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<td>2-Input Logic AND</td>
<td>2A</td>
<td>6Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7243C</td>
<td></td>
<td>Logic AND/OR Output</td>
<td>2A</td>
<td>6Ω</td>
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<td>16.5V</td>
<td>20P-M</td>
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<tr>
<td>EL7252C</td>
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<td>2-Input Logic NAND</td>
<td>2A</td>
<td>6Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL7262C</td>
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<td>Inverting/Iso-Drains</td>
<td>2A</td>
<td>6Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL7272C</td>
<td></td>
<td>Non-Inverting/Iso-Drains</td>
<td>2A</td>
<td>6Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
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</tbody>
</table>

# Programmable Delay Driver

<table>
<thead>
<tr>
<th>Single</th>
<th>Dual</th>
<th>Features</th>
<th>Ipeak</th>
<th>$R_{ON}$</th>
<th>$T_{r}/T_{f}$</th>
<th>$V_{SUPPLY}$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7861C</td>
<td></td>
<td>User-Defined Polarity</td>
<td>1A</td>
<td>10Ω</td>
<td>40 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL7961C</td>
<td></td>
<td>Non-Inverting w/Enable</td>
<td>1A</td>
<td>10Ω</td>
<td>40 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7971C</td>
<td></td>
<td>Inverting w/Enable</td>
<td>1A</td>
<td>10Ω</td>
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<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL7981C</td>
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<td>Complimentary w/Enable</td>
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<td>10Ω</td>
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<td>16.5V</td>
<td>8P-N-S</td>
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<td>EL7962C</td>
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<td>Non-Invert w/Independent Delay</td>
<td>1A</td>
<td>10Ω</td>
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<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL7972C</td>
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<td>Inverting w/Independent Delay</td>
<td>1A</td>
<td>10Ω</td>
<td>40 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
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<tr>
<td>EL7982C</td>
<td></td>
<td>Comp Outputs w/Independent Delay</td>
<td>1A</td>
<td>10Ω</td>
<td>40 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
</tbody>
</table>

*For these datasheets see: Application Specific—A.T.E.
### Power Supply Bridge Drivers

| Single | Dual | Features      | Ipeak | $R_{ON}$ | $\text{Tr}/\text{Tf}$ | $V_{\text{SUPPLY}}$ | Package
<table>
<thead>
<tr>
<th></th>
<th></th>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>P = Pins</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N = PDIP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>S = SOIC</td>
</tr>
<tr>
<td>EL7501C</td>
<td></td>
<td>High-Side Driver</td>
<td>1A</td>
<td>10Ω</td>
<td>100 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7661C</td>
<td></td>
<td>Full Bridge Driver</td>
<td>1A</td>
<td>10Ω</td>
<td>100 ns</td>
<td>16.5V</td>
<td>18P-N</td>
</tr>
<tr>
<td>EL7761C</td>
<td></td>
<td>Half Bridge Driver</td>
<td>1A</td>
<td>10Ω</td>
<td>100 ns</td>
<td>16.5V</td>
<td>16P-N-S</td>
</tr>
</tbody>
</table>

### Special Function Drivers

| Dual   | Quad   | Features                        | Ipeak | $R_{ON}$ | $\text{Tr}/\text{Tf}$ | $V_{\text{SUPPLY}}$ | Package
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
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<th></th>
</tr>
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<tbody>
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<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
<td>P = Pins</td>
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<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N = PDIP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>S = SOIC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>M = SOL</td>
</tr>
<tr>
<td>EL7412C</td>
<td></td>
<td>Integrated 4-Channel Driver</td>
<td>2A</td>
<td>6Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>20P-M</td>
</tr>
<tr>
<td>EL7182C</td>
<td></td>
<td>2 Phase CCD Driver</td>
<td>2A</td>
<td>6Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7240C</td>
<td></td>
<td>Non-Inverting/−V Outputs</td>
<td>2A</td>
<td>3Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7241C</td>
<td></td>
<td>Inverting/− Outputs</td>
<td>2A</td>
<td>3Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>*EL7154C</td>
<td></td>
<td>ATE/+15V ro −5V Outputs</td>
<td>2A</td>
<td>2.5Ω</td>
<td>20 ns/20 ns</td>
<td>16.5V</td>
<td>8P-N-S</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Level Shifter/3-State</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Application Specific - DC:DC Converters - For Datasheets, see Power Product Section

| Single | Features                        | Ipeak | $V_{\text{OUT}}$ | Accuracy | $V_{\text{SUPPLY}}$ | Package
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EL7560C</strong></td>
<td>Ext Ref Integrated PWM + FETs IC</td>
<td>12.4A</td>
<td>2.1V−3.5V</td>
<td>1%</td>
<td>6V</td>
<td>28P-M</td>
</tr>
<tr>
<td><strong>EL7561C</strong></td>
<td>Int Ref Integrated PWM + FETs IC</td>
<td>12.4A</td>
<td>2.1V−3.5V</td>
<td>1%</td>
<td>6V</td>
<td>28P-M</td>
</tr>
<tr>
<td><strong>EL7556C</strong></td>
<td>Int Ref Integrated PWM + FETs IC</td>
<td>6A</td>
<td>Variable</td>
<td>1%</td>
<td>6V</td>
<td>28P-M</td>
</tr>
<tr>
<td><strong>EL7571C</strong></td>
<td>Int Ref PWM Controller IC</td>
<td>Variable</td>
<td>1.3V−3.5V</td>
<td>1%</td>
<td>4.5V−13.2V</td>
<td>20P-M</td>
</tr>
</tbody>
</table>

*For these datasheets see: Application Specific—A.T.E.
**For datasheets see: Application Specific—Data Processing
†See Ordering Information section in this databook.
**Features**
- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating range
- Separate drain connections

**Applications**
- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Resonant charging
- Cascoded drivers

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7104CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDPO031</td>
</tr>
<tr>
<td>EL7104CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDPO027</td>
</tr>
<tr>
<td>EL7114CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDPO031</td>
</tr>
<tr>
<td>EL7114CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDPO027</td>
</tr>
</tbody>
</table>

**General Description**
The EL7104C/EL7114C ICs are matched driver ICs that improve the operation of the industry standard TC-4420/29 clock drivers. The Elantec versions are very high speed drivers capable of delivering peak currents of 4A into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices.

**Connection Diagrams**

**EL7104C**
Non-Inverting Driver

**EL7114C**
Inverting Driver

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V+ to Gnd)</td>
<td></td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pins</td>
<td>−0.3V to +0.3V above V+</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Peak Output Current</td>
<td>4A</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
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<tr>
<td>Ambient Operating Temperature</td>
<td>−40°C to +85°C</td>
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</tr>
</tbody>
</table>

### Important Note
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_A = T_C = T_{A}$.

### Test Level Test Procedure

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at $T_A = 25°C$ for information purposes only.</td>
</tr>
</tbody>
</table>

## DC Electrical Characteristics $T_A = 25°C$, $V+ = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.4</td>
<td>I</td>
<td>V</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>@V+</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>[µA]</td>
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<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
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<td>0.8</td>
<td>I</td>
<td>V</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>@0V</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>[µA]</td>
<td></td>
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<tr>
<td>$V_{HVS}$</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
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<td>V</td>
<td>V</td>
<td></td>
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<td>Output</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>$R_{OH}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100$ mA</td>
<td>1.5</td>
<td>4</td>
<td>I</td>
<td>[Ω]</td>
<td></td>
</tr>
<tr>
<td>$R_{OL}$</td>
<td>Pull-Down Resistance</td>
<td>$I_{OUT} = +100$ mA</td>
<td>2</td>
<td>4</td>
<td>I</td>
<td>[Ω]</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>V+/GND</td>
<td>0.2</td>
<td>10</td>
<td>I</td>
<td>[µA]</td>
<td></td>
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<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>4</td>
<td></td>
<td>IV</td>
<td>A</td>
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<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>200</td>
<td></td>
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<td>[mA]</td>
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<tr>
<td>Power Supply</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Power Supply Current</td>
<td>Input = $V + EL7104$ EL7114</td>
<td>4.5</td>
<td>7.5</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td>I</td>
<td>V</td>
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</table>
AC Electrical Characteristics $T_A = 25^\circ C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 1000 \text{ pF}$</td>
<td>7.5</td>
<td>10</td>
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<tr>
<td></td>
<td></td>
<td>$C_L = 2000 \text{ pF}$</td>
<td></td>
<td></td>
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<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 1000 \text{ pF}$</td>
<td>10</td>
<td></td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 2000 \text{ pF}$</td>
<td>15</td>
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<tr>
<td>$t_{D-ON}$</td>
<td>Turn-On Delay Time</td>
<td>See Timing Table</td>
<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-OFF}$</td>
<td>Turn-Off Delay Time</td>
<td>See Timing Table</td>
<td>18</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Timing Table

Standard Test Configuration

Input Signal

D.U.T.

Output Signal

4.7 $\mu F$

2000 pF

5-6
Typical Performance Curve

Max Power/Derating Curves

- 8-Lead PDIP
- 8-Lead SO

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply Current

"ON" Resistance vs Supply Voltage

CASE:

<table>
<thead>
<tr>
<th>Device</th>
<th>Input Level</th>
<th>Curve</th>
</tr>
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<tbody>
<tr>
<td>EL7104</td>
<td>GND</td>
<td>A</td>
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<tr>
<td>EL7104</td>
<td>V+</td>
<td>C</td>
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<tr>
<td>EL7114</td>
<td>GND</td>
<td>C</td>
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<tr>
<td>EL7114</td>
<td>V+</td>
<td>E</td>
</tr>
</tbody>
</table>
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency

- $V_{DD} = +15V$
- $V_{DD} = +10V$
- $V_{DD} = +5V$
- $C_L = 2000 \text{ pF}$

Frequency

Supply Current (mA)

Rise/Fall Time vs Load

- $V_{DD} = 10V$

Load Capacitance (pF)

Rise/Fall Time vs Supply Voltage

- $C_L = 2000 \text{ pF}$
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage

Rise/Fall Time vs Temperature

Delay vs Temperature
Features
• Logic and input
• 3V and 5V Input compatible
• Clocking speeds up to 10 MHz
• 20 ns Switching/delay time
• 4A Peak drive
• Isolated drains
• Low output impedance—2.5Ω
• Low quiescent current—5 mA
• Wide operating voltage—4.5V–16V

Applications
• Short circuit protected switching
• Under-voltage shut-down circuits
• Switch-mode power supplies
• Motor controls
• Power MOSFET switching
• Switching capacitive loads
• Asymmetrical switching
• Resonant charging
• Cascoded switching

Ordering Information
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7144CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin</td>
<td>P-DIP MDP0031</td>
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<tr>
<td>EL7144CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

General Description
The EL7144C dual input, driver achieves excellent switching while providing added flexibility. The 2-input logic and configuration coupled with the “isolated drains” makes this part well suited for various driver applications requiring an asymmetrical drive, resonant charging, and gated control. Providing twice as much drive as the EL7242 family, the EL7144C is excellent for driving large power MOSFET's and other capacitive loads.

Connection Diagram

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047
Absolute Maximum Ratings

Supply (V+ to Gnd) | 16.5V  | Operating Junction Temperature | 125°C  
Input Pins | -0.3V to +0.3V above V+ | Power Dissipation | 
Peak Output Current | 4A  | SOIC | 570 mW  
Storage Temperature Range | -65°C to +150°C | PDIP | 1050 mW  
Ambient Operating Temperature | -40°C to +85°C | 

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TJ=TC=TA.

Test Level | Test Procedure
--- | ---
I | 100% production tested and QA sample tested per QA test plan QCX0002.
II | 100% production tested at TA = 25°C and QA sample tested at TA = 25°C.
III | TMAX and TMIN per QA test plan QCX0002.
IV | QA sample tested per QA test plan QCX0002.
V | Parameter is guaranteed (but not tested) by Design and Characterization Data.

DC Electrical Characteristics TA = 25°C, V+ = 15V unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logic “1” Input Voltage</td>
<td>VIH = V+</td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>IH</td>
<td>Logic “1” Input Current</td>
<td>VIH = V+</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>μA</td>
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<tr>
<td>VIL</td>
<td>Logic “0” Input Voltage</td>
<td>VIL = GND</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>IL</td>
<td>Logic “0” Input Current</td>
<td>VIL = GND</td>
<td>0.3</td>
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<td>V</td>
<td>V</td>
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<td>VHYS</td>
<td>Input Hysteresis</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROH</td>
<td>Pull-Up Resistance</td>
<td>IOUT = -100 mA</td>
<td>1.5</td>
<td>4</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>ROL</td>
<td>Pull-Down Resistance</td>
<td>IOUT = +100 mA</td>
<td>2</td>
<td>4</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>IOUT</td>
<td>Output Leakage Current</td>
<td>V+ / GND</td>
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<td>10</td>
<td></td>
<td>I</td>
<td>μA</td>
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<tr>
<td>IPK</td>
<td>Peak Output Current</td>
<td>Source</td>
<td>4</td>
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<td></td>
<td>V</td>
<td>A</td>
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<td>PK</td>
<td>Peak Output Current</td>
<td>Sink</td>
<td>4</td>
<td></td>
<td></td>
<td>V</td>
<td>A</td>
</tr>
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<td>IDC</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>200</td>
<td></td>
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<td>I</td>
<td>mA</td>
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Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
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<td>Inputs V+</td>
<td>1</td>
<td>2.5</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td>VS</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td></td>
<td>I</td>
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</table>

5-12
## AC Electrical Characteristics

$T_A = 25^\circ C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 1000 \text{ pF}$</td>
<td>7.5</td>
<td>10</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 2000 \text{ pF}$</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 1000 \text{ pF}$</td>
<td>10</td>
<td></td>
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<td></td>
<td></td>
<td>$C_L = 2000 \text{ pF}$</td>
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<td></td>
<td>20</td>
<td></td>
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<tr>
<td>$t_{D-ON}$</td>
<td>Turn-On Delay Time</td>
<td>See Timing Table</td>
<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-OFF}$</td>
<td>Turn-Off Delay Time</td>
<td>See Timing Table</td>
<td>20</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Timing Table

![Timing Table Diagram](image)

### Standard Test Configuration

![Standard Test Configuration Diagram](image)

### Simplified Schematic

![Simplified Schematic Diagram](image)
Typical Performance Curve

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply Current

"ON" Resistance vs Supply Voltage
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency

Rise/Fall Time vs Load

Rise/Fall Time vs Supply Voltage
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage

Rise/Fall Time vs Temperature

Delay vs Temperature
**Features**
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- Reduced clock skew
- 20 ns Switching/delay time
- 2A Peak drive
- Low quiescent current
- Wide operating voltage—4.5V–16V

**Applications**
- CCD Drivers requiring high-contrast imaging
- Differential line drivers
- Push-pull circuits

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline</th>
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<td>−40°C to +85°C</td>
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<tr>
<td>EL7182CS</td>
<td>−40°C to +85°C</td>
<td>8-Pin SO</td>
<td>MDP0037</td>
</tr>
</tbody>
</table>

**General Description**

The EL7182C is extremely well suited for driving CCD’s, especially where high contrast imaging is desirable. The 16V supply rating is attractive for higher voltage CCD applications, as in color fax machines. The input is TTL and 3V compatible. The low quiescent current requirement is advantageous in portable/battery powered systems. The EL7182 is available in 8-pin P-DIP and 8-lead SO packages.

**Connection Diagram**

![Diagram of EL7182C](image)

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<tr>
<td>Supply (V+ to Gnd)</td>
<td>16.5V</td>
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<tr>
<td>Input Pins</td>
<td>-0.3V to +0.3V above V+</td>
</tr>
<tr>
<td>Combined Peak Output Current</td>
<td>4A</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
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<tr>
<td>Power Dissipation</td>
<td>570 mW</td>
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<tr>
<td>PDIP</td>
<td>1050 mW</td>
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</table>

### Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore Ta = TC = TA.

### Test Level

- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at T_a = 25°C and QA sample tested at T_a = 25°C.
- **III**: T_MAX and T_MIN per QA test plan QCX0002.
- **IV**: QA sample tested per QA test plan QCX0002.
- **V**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at T_a = 25°C for information purposes only.

### DC Electrical Characteristics

Parameters are valid for TA = 25°C, V = 15V unless otherwise specified.

<table>
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<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td><strong>Input</strong></td>
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<td></td>
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</tr>
<tr>
<td>VIH</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>IIH</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>@V+</td>
<td>0.1</td>
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<td></td>
<td>I</td>
<td>μA</td>
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<tr>
<td>VIL</td>
<td>Logic &quot;0&quot; Input Voltage</td>
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<td>I</td>
<td>V</td>
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<tr>
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<td>10</td>
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<td>I</td>
<td>μA</td>
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<td>VHV</td>
<td>Input Hysteresis</td>
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<td>0.3</td>
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<td></td>
<td>V</td>
<td>V</td>
</tr>
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<td><strong>Output</strong></td>
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<td></td>
</tr>
<tr>
<td>ROH</td>
<td>Pull-Up Resistance</td>
<td>IOUT = -100 mA</td>
<td>3</td>
<td>6</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>ROL</td>
<td>Pull-Down Resistance</td>
<td>IOUT = +100 mA</td>
<td>4</td>
<td>6</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>IPK</td>
<td>Peak Output Current</td>
<td>Source, Sink</td>
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<td>2</td>
<td></td>
<td>IV</td>
<td>A</td>
</tr>
<tr>
<td>IDC</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>100</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td>Power Supply Current</td>
<td>Input High</td>
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<td>mA</td>
</tr>
<tr>
<td>VS</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

$T_A = 25\degree C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 500\ \text{pF}$</td>
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<tr>
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<td>$C_L = 1000\ \text{pF}$</td>
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<td></td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 500\ \text{pF}$</td>
<td>10</td>
<td>13</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 1000\ \text{pF}$</td>
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<td></td>
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</tr>
<tr>
<td>$t_{D-ON}$</td>
<td>Turn-On Delay Time</td>
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<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-OFF}$</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td>20</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Timing Table

![Timing Table](image)

### Standard Test Configuration

![Standard Test Configuration](image)

### Simplified Schematic

![Simplified Schematic](image)
EL7182C
2-Phase, High Speed CCD Driver

Typical Performance Curve

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply Current

CASE:

"ON" Resistance vs Supply Voltage

Measured at 100 mA

Pull Down

Pull Up

5-20
Typical Performance Curve — Contd.

**Average Supply Current vs Voltage and Frequency**

![Diagram showing average supply current vs voltage and frequency](image)

- $V_{DD} = +15V$
- $V_{DD} = +10V$
- $V_{DD} = +5V$

**Average Supply Current vs Capacitive Load**

![Diagram showing average supply current vs capacitive load](image)

- $V_{DD} = 10V$
- 10,000 pF
- 1,000 pF
- 100 pF
- No Load

**Rise/Fall Time vs Load**

![Diagram showing rise/fall time vs load capacitance](image)

- $V_{DD} = 10V$
- Load Capacitance (pF)

**Rise/Fall Time vs Supply Voltage**

![Diagram showing rise/fall time vs supply voltage](image)

- $C_L = 1000$ pF
Typical Performance Curve — Contd.

- **Rise/Fall Time vs Temperature**
  - \( V_{DD} = 10V \)
  - \( C_L = 1000 \text{ pF} \)
  - Temperature \( -50 \text{ to } 125 \degree C \)

- **Propagation Delay vs Supply Voltage**
  - \( C_L = 1000 \text{ pF} \)
  - Supply Voltage \( 5 \text{ to } 15 \)

- **Delay Time vs Temperature**
  - \( V_{DD} = 10V \)
  - \( C_L = 1000 \text{ pF} \)
  - Temperature \( -50 \text{ to } 125 \degree C \)
Features

- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range

Applications

- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

General Description

The EL7202C/EL7212C/EL7222C ICs are matched dual-drivers ICs that improve the operation of the industry standard DS0026 clock drivers. The Elantec Versions are very high speed drivers capable of delivering peak currents of 2.0 amps into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

Connection Diagrams

![Connection Diagrams](image)

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V+ to Gnd)</td>
<td>16.5V</td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3V to +0.3V above V+</td>
</tr>
<tr>
<td>Combined Peak Output Current</td>
<td>4A</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>125°C</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>570 mW</td>
</tr>
<tr>
<td>PDIP</td>
<td>1050 mW</td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_d = T_c = T_a$.

### DC Electrical Characteristics $T_a = 25°C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>@V+</td>
<td></td>
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<td>10</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
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<td>0.8</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>@0V</td>
<td>0.1</td>
<td></td>
<td>10</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{HYS}$</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
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<td></td>
<td>V</td>
<td>V</td>
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<tr>
<td><strong>Output</strong></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{OH}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100$ mA</td>
<td>3</td>
<td>6</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{OL}$</td>
<td>Pull-Down Resistance</td>
<td>$I_{OUT} = +100$ mA</td>
<td>4</td>
<td>6</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>2</td>
<td></td>
<td></td>
<td>IV</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>100</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Power Supply Current</td>
<td>Inputs High/7202</td>
<td>4.5</td>
<td>7.5</td>
<td></td>
<td>I</td>
<td>mA</td>
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<tr>
<td></td>
<td></td>
<td>Inputs High/7212</td>
<td>1</td>
<td>2.5</td>
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<td>I</td>
<td>mA</td>
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<tr>
<td></td>
<td></td>
<td>Inputs High/7222</td>
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<td>5.0</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>15</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
AC Electrical Characteristics  $T_A = 25^\circ C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 500 \ pF$</td>
<td>7.5</td>
<td>10</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 1000 \ pF$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 500 \ pF$</td>
<td>10</td>
<td>13</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 1000 \ pF$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{D1}$</td>
<td>Turn-On Delay Time</td>
<td>See Timing Table</td>
<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D2}$</td>
<td>Turn-Off Delay Time</td>
<td>See Timing Table</td>
<td>20</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

![Timing Table](image1.png)

![Standard Test Configuration](image2.png)

![Simplified Schematic](image3.png)
Typical Performance Curve

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply Current

"ON" Resistance vs Supply Voltage
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency

![Graph showing supply current vs voltage and frequency with different supply voltages and frequencies.]

Average Supply Current vs Capacitive Load

![Graph showing supply current vs capacitive load with different load capacitances and supply voltages.]

Rise/Fall Time vs Load

![Graph showing rise/fall time vs load capacitance with different load capacitances.]

Rise/Fall Time vs Supply Voltage

![Graph showing rise/fall time vs supply voltage with different capacitances.]

7202-12
7202-13
7202-14
7202-15
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage

Rise/Fall Time vs Temperature

Delay vs Temperature
EL7212 Macro Model

```
**** EL7212 model ****

* input
*               gnd
*               Vsupply
*               Vout

.subckt M7212 2 3 6 7
V1 12 3 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 3 43.3 pF
D1 14 13 dmod
X1 13 11 2 3 comp1
X2 16 12 15 3 comp1
sp 6 7 16 3 spmod
sn 7 3 16 3 snmod
g1 11 0 13 0 938μ
.model dmod d
.model spmod vswitch ron=3 roff=2meg von=1 voff=1.5
.model snmod vswitch ron=4 roff=2meg von=3 voff=2
.ends M7212
.subckt comp1 out inp inm vss
c1 out vss table (v(inp) - v(inm)) * 5000 = (0,0) (3.2,3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends comp1
```
Features
- 20 ns Propagation delay
- Clock to 10 MHz
- 2 Amp peak output drive
- 3Ω output impedance
- 3V/5V Logic input compatible
- Outputs "OK" below ground
- Operating voltage 4.5V to 16V

Applications
- Tape drive-write head driver
- Current switching
- Center-Tapped transformer driver
- ATE-pin drivers
- Analog switching
- AC switching
- T - switch

General Description
The EL7240C/EL7241C high speed coil drivers accept logic inputs which independently control a pair of 3Ω PMOS FET's. The output transistors share a common source, making these devices well suited for "current steering" and analog switching applications. The typical clamping diodes to ground are removed, thus allowing pins (6) and (7) to swing negative. This feature is desirable when driving "center-tapped" coils referenced to ground. The logic "NAND" input configuration can be used to "enable" the outputs. The EL7240C and EL7241C differ only by their logic polarity.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7240CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL7240CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-SOIC</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL7241CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL7241CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Connection Diagrams

**EL7240C**

```
+-----------------+      +-----------------+
|                  |      |                  |
| INPUT (A)        |      | INPUT (B)        |
|                  |      |                  |
| (A) INPUT        |      | (B) INPUT        |
|                  |      |                  |
| ENABLE           |      |                  |
|                  |      |                  |
| (A) OUTPUT       |      | (B) OUTPUT       |
|                  |      |                  |
| COMMON SOURCE    |      | GND              |
```

**EL7241C**

```
+-----------------+      +-----------------+
|                  |      |                  |
| INPUT (A)        |      | INPUT (B)        |
|                  |      |                  |
| (A) INPUT        |      | (B) INPUT        |
|                  |      |                  |
| ENABLE           |      |                  |
|                  |      |                  |
| (A) OUTPUT       |      | (B) OUTPUT       |
|                  |      |                  |
| COMMON SOURCE    |      | GND              |
```
Absolute Maximum Ratings

Supply (V+ to GND) 16.5V  
Input Pins -0.3V to +0.3V above V+  
Combined Peak Output Current 4A  
Storage Temperature Range -65°C to +150°C  
Ambient Operating Temperature -40°C to +85°C  
Operating Junction Temperature 125°C  
Power Dissipation 570 mW  
1050 mW  

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level Test Procedure
I 100% production tested and QA sample tested per QA test plan QCX0002.  
II 100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.  
III QA sample tested per QA test plan QCX0002.  
IV Parameter is guaranteed (but not tested) by Design and Characterization Data.  
V Parameter is typical value at $T_A = 25°C$ for information purposes only.

DC Electrical Characteristics $T_A = 25°C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>@V+</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>@0V</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>$\mu$A</td>
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<tr>
<td>$V_{HVS}$</td>
<td>Input Hysteresis</td>
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<td>0.3</td>
<td></td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{ON}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100$ mA</td>
<td>3</td>
<td>6</td>
<td>I</td>
<td>$\Omega$</td>
<td></td>
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<tr>
<td>$I_{OFF}$</td>
<td>Off Leakage</td>
<td>$V_{OUT} = 0V$</td>
<td>0.2</td>
<td>10</td>
<td>I</td>
<td>$\mu$A</td>
<td></td>
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<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>Source</td>
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<td>IV</td>
<td>A</td>
<td></td>
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<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Channel</td>
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<td></td>
<td></td>
<td>mA</td>
<td></td>
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<tr>
<td>$V_S$</td>
<td>Source Potential with Grounded Drain</td>
<td>Channel A or B 100 mA Load</td>
<td>2.3</td>
<td>2.75</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Power Supply</td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Power Supply Current</td>
<td>Inputs High</td>
<td>1</td>
<td>2.5</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

\( T_A = 25^\circ C, \, V = 15V \) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{D\text{-ON}} )</td>
<td>Turn-On Delay Time</td>
<td></td>
<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{D\text{-OFF}} )</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td>20</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

Rise and Fall times (\( t_R \) and \( t_F \)) are load dependant.

### Typical Performance Curves

- **Supply Current vs \( V_{DD} \) and Input Connection**
- **Source Voltage vs Current (Grounded Drain)**
- **Output Conduction vs \( V_{GS} \)**
Typical Performance Curves — Contd.

Max Power/Derating Curves

- 8-Lead PDIP
- 8-Lead SO

Max $T_J = 125°C$

Switch Threshold vs Supply Voltage

High Limit = 2.4V

Low Limit = 0.8V

Input Current vs Voltage

$V_{IN}$ 2.500/div (V)

Peak Drive vs Supply Voltage

P-CHANNEL

Delay vs Temperature

$V_{DD} = 10V$
Typical Applications

Write Head Driver

\[ V_{DD} = +12V \]

- **DATA INPUTS**: (A) INPUT, (B) INPUT
- **ENABLE**: 3
- **OUTPUTS**: (A) OUTPUT, (B) OUTPUT
- **Ground (GND)**

High Current LED/Laser Diode Driver

\[ V_{DD} = +5V \]

- **CURRENT ADJ.**
- **INPUT**: ENABLE
- **OUTPUTS**: (A) OUTPUT, (B) OUTPUT
- **Ground (GND)**
Typical Applications — Contd.

Bi-Level Step Generator

Level Shifter
Typical Applications — Contd.

Push-Pull Transformer Driver

High Speed Bipolar Drive Circuit
Typical Applications — Contd.

"Two-Bit" Current Source with Gating

$V_{DD} = +12\text{V}$

[Diagram of EL7240C/EL7241C High Speed Coil Drivers]
Features
- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage — 4.5V – 16V

Applications
- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

General Description
The EL7242C/EL7252C dual input, 2-channel drivers achieve the same excellent switching performance of the EL7212 family while providing added flexibility. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7242C/EL7252C are excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

Connection Diagrams

Manufactured under U.S. Patent Nos. 5,334,883, # 5,341,047
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V+ to Gnd)</td>
<td>16.5V</td>
<td></td>
<td></td>
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<tr>
<td>Input Pins</td>
<td>-0.3V to +0.3V above V+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Combined Peak Output Current</td>
<td>4A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

### Test Level

<table>
<thead>
<tr>
<th>Test Procedure</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at $T_A = 25°C$ for information purposes only.</td>
</tr>
</tbody>
</table>

## DC Electrical Characteristics  $T_A = 25°C$, $V = 15V$ unless otherwise specified

### Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>@V+</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>@0V</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{HVS}$</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
</tbody>
</table>

### Output

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{OH}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100mA$</td>
<td>3</td>
<td>6</td>
<td>I</td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{OL}$</td>
<td>Pull-Down Resistance</td>
<td>$I_{OUT} = +100mA$</td>
<td>4</td>
<td>6</td>
<td>I</td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>2</td>
<td>2</td>
<td>IV</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>100</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

### Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>Power Supply Current</td>
<td>Inputs High</td>
<td>1</td>
<td>2.5</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
# AC Electrical Characteristics

**T<sub>A</sub> = 25°C, V<sub>L</sub> = 15V unless otherwise specified**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Rise Time</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 500 pF</td>
<td>10</td>
<td>20</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 1000 pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;F&lt;/sub&gt;</td>
<td>Fall Time</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 500 pF</td>
<td>10</td>
<td>20</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 1000 pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;D-ON&lt;/sub&gt;</td>
<td>Turn-On Delay Time</td>
<td></td>
<td>20</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;D-OFF&lt;/sub&gt;</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Timing Table

- **Input:** 5V, 2.5V, 0V
- **Inverted Output:** 90%, 10%
- **Non-Inverted Output:** 90%, 10%

## Standard Test Configuration

- **V+**
- **Input:** 1000 pF
- **2.5V**
- **EL7242**
- **Output:** 4.7 µF
- **Load:**

## Simplified Schematic

- **V+**
- **Input Buffer**
- **Reference & Level Shifter**
- **Inverting Buffer w/ Hysteresis**
- **Logic Gate**
- **Super Inverter**
- **Output**
Typical Performance Curve

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply Current

“ON” Resistance vs Supply Voltage

CASE:

A ALL INPUTS GND
B 3 INPUTS GND
C 2 INPUTS GND
D 1 INPUT GND
E ALL INPUTS V+
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency

Average Supply Current vs Capacitive Load

Rise/Fall Time vs Load

Rise/Fall Time vs Supply Voltage
Typical Performance Curve — Contd.

- **Rise/Fall Time vs Temperature**
  - Delay Time (ns)
  - Supply Voltage
  - $C_L = 1000 \text{ pF}$

- **Propagation Delay vs Supply Voltage**
  - Rise/Fall Time (ns)
  - Temperature $\degree\text{C}$
  - $V_{DD} = 10\text{V}$
  - $C_L = 1000 \text{ pF}$

- **Delay vs Temperature**
  - Delay Time (ns)
  - Temperature $\degree\text{C}$
  - $V_{DD} = 10\text{V}$
  - $C_L = 1000 \text{ pF}$
**Features**
- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 20 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage—4.5V–16V

**Applications**
- CCD Drivers
- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7243CM</td>
<td>–40°C to +85°C</td>
<td>20-Lead MDP0027*</td>
<td>Thermal SOL</td>
</tr>
</tbody>
</table>

**General Description**

The EL7243C dual input, 2-channel driver achieves the same excellent switching performance of the EL7212 family while providing added flexibility. The power package makes this part extremely well suited for high frequency and heavy loads as in CCD applications. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7243C is excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

**Connection Diagram**

20-Lead Thermal SOL Package

EL7243C

- GND IN B
- IN C
- IN D
- GND GND
- OUT B
- OUT A

**Note 1:** Pins 4–7 and 14–17 are electrically connected.
**Note 2:** Output pins must be tied together.
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V+ to Gnd)</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3V to +0.3V above V+</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Combined Peak Output Current</td>
<td>4A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1500 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Important Note: All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TJ = TC = TA.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics  \( T_A = 25°C, V_{DD} = 15V \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td>@VDD</td>
<td>2.4</td>
<td>I</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Logic &quot;1&quot; Input Current</td>
<td>( I_{OUT} = -100 mA )</td>
<td>3</td>
<td>6</td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td>@0V</td>
<td>0.8</td>
<td>I</td>
<td>V</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>Logic &quot;0&quot; Input Current</td>
<td>( I_{OUT} = +100 mA )</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output</td>
<td>Pull-Up Resistance</td>
<td>Source/Sink</td>
<td>2</td>
<td></td>
<td></td>
<td>IV</td>
</tr>
<tr>
<td></td>
<td>Pull-Down Resistance</td>
<td></td>
<td>4</td>
<td>6</td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>2</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>200</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power Supply</td>
<td>Power Supply Current</td>
<td>Inputs High</td>
<td>1</td>
<td>2.5</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>

5-45
AC Electrical Characteristics  $T_A = 25^\circ C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 500 , pF$</td>
<td>10</td>
<td>20</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 1000 , pF$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 500 , pF$</td>
<td>10</td>
<td>20</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 1000 , pF$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{D,ON}$</td>
<td>Turn-On Delay Time</td>
<td></td>
<td>20</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D,OFF}$</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td>20</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Timing Table

<table>
<thead>
<tr>
<th>Timing Table</th>
<th>Standard Test Configuration</th>
</tr>
</thead>
</table>

![Timing Table](image)

![Standard Test Configuration](image)

Pins 19, 20 connected to $V^+$. 

---

Simplified Schematic

![Simplified Schematic](image)
Typical Performance Curves

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply Current

"ON" Resistance vs Supply Voltage
Typical Performance Curves — Contd.

**Average Supply Current vs Voltage and Frequency**

- Supply Current (mA) vs Frequency (kHz) for different supply voltages ($V_{DD}$):
  - $V_{DD} = +15V$
  - $V_{DD} = +10V$
  - $V_{DD} = +5V$

- $C_L = 1000 \text{ pF}$

**Average Supply Current vs Capacitive Load**

- Supply Current (mA) vs Frequency (kHz) for different capacitive loads:
  - $V_{DD} = 10V$
  - $10,000 \text{ pF}$
  - $1,000 \text{ pF}$
  - $100 \text{ pF}$
  - No Load

(Equivalent Internal Capacitance = 470 pF)

**Rise/Fall Time vs Load**

- Rise/Fall Time (ns) vs Load Capacitance (pF) for $V_{DD} = 10V$:
  - $C_L = 1000 \text{ pF}$

**Rise/Fall Time vs Supply Voltage**

- Rise/Fall Time (ns) vs Supply Voltage (V) for $C_L = 1000 \text{ pF}$:
### Typical Performance Curves — Contd.

#### Rise/Fall Time vs Temperature

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>Delay Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>7.5</td>
<td>30</td>
</tr>
<tr>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>12.5</td>
<td>10</td>
</tr>
<tr>
<td>15</td>
<td>0</td>
</tr>
</tbody>
</table>

$C_L = 1000 \, \text{pF}$

#### Propagation Delay vs Supply Voltage

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>Rise/Fall Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>30</td>
</tr>
<tr>
<td>-25</td>
<td>20</td>
</tr>
<tr>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>25</td>
<td>0</td>
</tr>
<tr>
<td>50</td>
<td>-10</td>
</tr>
<tr>
<td>75</td>
<td>-15</td>
</tr>
<tr>
<td>100</td>
<td>-20</td>
</tr>
<tr>
<td>125</td>
<td>-25</td>
</tr>
</tbody>
</table>

$V_{DD} = 10V$

$C_L = 1000 \, \text{pF}$

#### Delay vs Temperature

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Delay Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>40</td>
</tr>
<tr>
<td>-25</td>
<td>30</td>
</tr>
<tr>
<td>0</td>
<td>20</td>
</tr>
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<td>25</td>
<td>10</td>
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<tr>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>75</td>
<td>-10</td>
</tr>
<tr>
<td>100</td>
<td>-15</td>
</tr>
<tr>
<td>125</td>
<td>-20</td>
</tr>
</tbody>
</table>

$V_{DD} = 10V$

$C_L = 1000 \, \text{pF}$
Applications Information

Typical CCD Configuration

EL7243 Macromodel

EL7243C
Dual Input, High Speed, Dual Channel CCD Driver
EL7243 Macromodel

* EL7243 Macromodel
* Revision A, January 1996

* Connections

| Gnd | Inp+ | | Inp- | | | out | | | | | VCC |
|-----|------|---|------|---|---|---|---|---|---|---|---|---|
| subckt M7243 | 1 | 2 | 3 | 8 | 10 |

V1 12 1 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 1 43.3pF
D1 14 13 dmod
X1 13 11 2 1 comp1
X2 16 12 15 1 comp1
V2 22 1 1.6
R6 23 25 1K
R7 24 25 5K
R8 21 22 100
C2 25 1 43.3pF
D2 24 23 dmod
X3 23 21 3 1 comp1
X4 26 25 22 1 comp1
X5 16 26 17 1 And-gate
sp 10 8 17 1 spmod
sn 8 1 17 1 snmod
g1 11 1 13 1 938u
g2 21 23 1 938u
.model dmod d
.model spmod vswitch ron = 3 roff = 2meg von = 1 voff = 1.5
.model snmod vswitch ron = 4 roff = 2meg von = 3 voff = 2
.ends M7243

* AND Gate Subcircuit*

.subckt And-gate inp1 inp2 out-AS Vss-A
el out-A Vss-A table {v(inp1)*v(inp2)} = (0,3.2) (3.2, 0)
Rout-a out-a vss-a 10 meg
rinp inp1 vss-a 10 meg
rinp2 inp2 vss-a 10 meg
.ends and-gate

* Comparator Subcircuit *

.subckt comp1 out inp inm vss
el out vss table {(v(inp)-v(inm))*5000} = (0,0) (3.2, 3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends comp1
Features
- Separate drain connections
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Low output impedance
- Low quiescent current
- Wide operating voltage

Applications
- Asymmetrical switching
- Cascoded switching
- Resonant charging
- Floating load circuits
- Bridge circuits

General Description
The EL7262C/EL7272C, dual channel, power MOSFET drivers achieve the same excellent switching performance of the EL7202 family, with the added flexibility derived through the isolated drain architecture. The outputs can be configured in numerous ways, depending upon the application. The EL7262C and EL7272C are available in 8-pin P-DIP and 8-lead SO packages.

Connection Diagrams

Manufactured under U.S. Patent Nos. 5,334,883, 5,341,047
**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V+ to Gnd)</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3V to +0.3V above V+</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Combined Peak Output Current</td>
<td>4A</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
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<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
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<tr>
<td>Operating Junction Temperature</td>
<td>125°C</td>
<td></td>
<td></td>
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<tr>
<td>Power Dissipation</td>
<td>570 mW</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>1050 mW</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LT/27 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

**Test Level**
- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$.
- **III**: QA sample tested per QA test plan QCX0002.
- **IV**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at $T_A = 25°C$ for information purposes only.

**DC Electrical Characteristics** $T_A = 25°C$, $V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>$@V+$</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>$@0V$</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{HVS}$</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>$R_{OH}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100 \text{ mA}$</td>
<td>3</td>
<td>6</td>
<td></td>
<td>I</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$R_{OL}$</td>
<td>Pull-Down Resistance</td>
<td>$I_{OUT} = +100 \text{ mA}$</td>
<td>4</td>
<td>6</td>
<td></td>
<td>I</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>Output Leakage</td>
<td>$V_{OUT} = V+$</td>
<td>0.2</td>
<td>10</td>
<td></td>
<td>I</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>2</td>
<td></td>
<td>IV</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>100</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Power Supply**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Inputs</th>
<th>EL7262</th>
<th>EL7272</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>Power Supply Current</td>
<td></td>
<td>High</td>
<td>EL7262</td>
<td>EL7272</td>
<td>1</td>
<td>2.5</td>
<td>7.5</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Operating Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.5</td>
<td>16</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
**AC Electrical Characteristics**  \( T_A = 25^\circ C, V = 15V \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
</table>
| \( t_R \)  | Rise Time  | \( C_L = 500 \text{ pF} \)  
\( C_L = 1000 \text{ pF} \) | 7.5 | 10  | 20  | IV       | ns    |
| \( t_F \)  | Fall Time  | \( C_L = 500 \text{ pF} \)  
\( C_L = 1000 \text{ pF} \) | 10  | 13  | 20  | IV       | ns    |
| \( t_{D\text{-ON}} \) | Turn-On Delay Time | See Timing Table | 18  | 25  |      | IV       | ns    |
| \( t_{D\text{-OFF}} \) | Turn-Off Delay Time | See Timing Table | 20  | 25  |      | IV       | ns    |

**Timing Table**

- **Input**: 2.5V
- **Inverted Output**: 0 to 90%
- **Non-Inverted Output**: 0 to 90%

**Standard Test Configuration**

- **Input**: 2
- **Output**: 7
- **Capacitance**: 4.7 \( \mu F \)

**Simplified Schematic**

- **Input Buffer**
- **Reference & Level Shifter**
- **Inverting Buffer w/ Hysteresis**
- **2nd Inverting Buffer**
- **Super Inverter**

**Notes**

- 7262-3
- 7262-4
- 7262-5
Typical Performance Curve

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply Current

"ON" Resistance vs Supply Voltage

CASE:

<table>
<thead>
<tr>
<th>Device</th>
<th>Input Level</th>
<th>Curve</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7262</td>
<td>GND</td>
<td>C</td>
</tr>
<tr>
<td>EL7262</td>
<td>GND, V+</td>
<td>D</td>
</tr>
<tr>
<td>EL7262</td>
<td>V+</td>
<td>E</td>
</tr>
<tr>
<td>EL7272</td>
<td>GND</td>
<td>A</td>
</tr>
<tr>
<td>EL7272</td>
<td>GND, V+</td>
<td>B</td>
</tr>
<tr>
<td>EL7272</td>
<td>V+</td>
<td>C</td>
</tr>
</tbody>
</table>
Typical Performance Curve — Contd.

**Average Supply Current vs Voltage and Frequency**

- $V_{DD} = +15V$
- $V_{DD} = +10V$
- $V_{DD} = +5V$
- $C_L = 1000 \text{ pF}$

**Average Supply Current vs Capacitive Load**

- $V_{DD} = 10V$
- No Load
- (Equivalent Internal Capacity = 470 \text{ pF})

**Rise/Fall Time vs Load**

- $V_{DD} = 10V$
- $C_L = 1000 \text{ pF}$

**Rise/Fall Time vs Supply Voltage**

- $C_L = 1000 \text{ pF}$
Typical Performance Curve — Contd.

**Propagation Delay vs Supply Voltage**

- Delay Time (ns)
- Supply Voltage
- \( C_L = 1000 \text{ pF} \)

**Rise/Fall Time vs Temperature**

- Rise Time (ns)
- Fall Time (ns)
- Temperature (°C)
- \( V_{DD} = 10 \text{V} \)
- \( C_L = 1000 \text{ pF} \)

**Delay vs Temperature**

- Delay Time (ns)
- Temperature (°C)
- \( V_{DD} = 10 \text{V} \)
- \( C_L = 1000 \text{ pF} \)
Features
- Excellent response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range

Applications
- Full bridge drivers
- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

General Description
The EL7412C contains (4) high performance matched drivers. These very high speed drivers are capable of delivering peak currents of 2.0 amps into highly capacitive loads and are ideally suited for “Full bridge” and ultrasound applications. The high speed performance is achieved by means of a proprietary “Turbo-Driver” circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. The matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

Connection Diagram

20 Lead Thermal SOL Package

![Connection Diagram](image)

Note 1: Pins 4–7 and 14–17 are electrically connected.

Manufactured under U.S. Patent Nos. 5,334,883, #5,331,047
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min Value</th>
<th>Typ Value</th>
<th>Max Value</th>
<th>Test Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V+ to Gnd)</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3V to +0.3V above V+</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Combined Peak Output Current</td>
<td>8A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Storage Temperature Range     | -65°C to +150°C              |           |           |           |            |
| Power Dissipation             |                               |           |           |           |            |

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level | Test Procedure                                                                 |
----------|-------------------------------------------------------------------------------|
I         | 100% production tested and QA sample tested per QA test plan QCX0002.          |
II        | 100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$ . |
          | $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.                              |
III       | QA sample tested per QA test plan QCX0002.                                     |
IV        | Parameter is guaranteed (but not tested) by Design and Characterization Data. |
V         | Parameter is typical value at $T_A = 25°C$ for information purposes only.     |

DC Electrical Characteristics $T_A = 25°C$, $V_{DD} = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
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<td>2.4</td>
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<td>I</td>
<td>V</td>
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<tr>
<td>$I_{IH}$</td>
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<td>@V_{DD}</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>µA</td>
</tr>
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<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
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<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>@0V</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{HVS}$</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Output</th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{OH}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100 mA$</td>
<td>3</td>
<td>6</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{OL}$</td>
<td>Pull-Down Resistance</td>
<td>$I_{OUT} = +100 mA$</td>
<td>4</td>
<td>6</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current Source/Sink</td>
<td>Source/Sink</td>
<td>2</td>
<td>2</td>
<td></td>
<td>IV</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>100</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
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</table>

Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{S}$</td>
<td>Power Supply Current</td>
<td>Inputs High</td>
<td>2</td>
<td>5</td>
<td></td>
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<td>mA</td>
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<tr>
<td>$V_{S}$</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>15</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
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</table>
AC Electrical Characteristics  $T_A = 25^\circ C, V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 500,\text{pF}$</td>
<td>7.5</td>
<td>10</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 1000,\text{pF}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 500,\text{pF}$</td>
<td>10</td>
<td></td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 1000,\text{pF}$</td>
<td>13</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{D1}$</td>
<td>Turn-On Delay Time</td>
<td>See Timing Table</td>
<td>18</td>
<td></td>
<td>25</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D2}$</td>
<td>Turn-Off Delay Time</td>
<td>See Timing Table</td>
<td>20</td>
<td></td>
<td>25</td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

Timing Table

![Timing Table Diagram](image1)

Standard Test Configuration

![Standard Test Configuration Diagram](image2)

Simplified Schematic

![Simplified Schematic Diagram](image3)
Typical Performance Curves

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

"ON" Resistance vs Supply Voltage
Typical Performance Curves — Contd.

**Average Supply Current vs Voltage and Frequency**

![Graph showing supply current vs frequency for different supply voltages.](7412-11)

**Average Supply Current vs Capacitive Load**

![Graph showing supply current vs frequency for different supply voltages.](7412-12)

**Rise/Fall Time vs Load**

![Graph showing rise/fall time vs load capacitance.](7412-13)

**Rise/Fall Time vs Supply Voltage**

![Graph showing rise/fall time vs supply voltage.](7412-14)
Typical Performance Curves — Contd.

Propagation Delay vs Supply Voltage

Rise/Fall Time vs Temperature

Delay vs Temperature
**Features**
- 100V High Side Voltage
- Rail to Rail Output
- 1 MHz Operation
- 1.0A Peak Current
- Matched Rise and Fall Times
- Direct Coupled
- No Start Up Ambiguity

**Applications**
- Uninterruptible Power Supplies
- DC-DC Converters
- Motor Control
- Power MOSFET Driver

**General Description**
The EL7501 provides a low cost solution to many high side drive applications. The EL7501 is DC coupled so there are no start up problems associated with AC coupled schemes. The EL7501 is driven by user supplied complementary signals.

**Connection Diagram**

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7501CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-Dip</td>
<td>MD0031</td>
</tr>
<tr>
<td>EL7501CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MD0027</td>
</tr>
</tbody>
</table>

---

**7501 Waveform Example**

---

**Figure 1**
Absolute Maximum Ratings ($T_A = 25^\circ C$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (VDD or LX to R– or R+)</td>
<td>100V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply (VDD to LX)</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Pins</td>
<td>$-0.3V$ below GND, $+0.3V$ above VDD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>2A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>2A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elanec performs most electrical tests using modern high-speed automatic test equipment, specifically the LT877 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_{J} = T_{C} = T_{A}$.

Test Level
I 100% production tested and QA sample tested per QA test plan QCX0002.
II $100\%$ production tested at $T_A = 25^\circ C$ and QA sample tested at $T_A = 25^\circ C$.
III $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.
IV QA sample tested per QA test plan QCX0002.
V Parameter is guaranteed (but not tested) by Design and Characterization Data.

DC Electrical Characteristics ($T_A = 25^\circ C$, $V_{DD} = 15V$, $C_{LOAD} = 1000$ pF, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DIFF}$ (Min)</td>
<td>Minimum Differential Input Signal to Switch Output</td>
<td>$1.0$</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DS,OFF}$</td>
<td>Output Leakage</td>
<td>$-10.0$</td>
<td>$-0.2$</td>
<td>$+0.2$</td>
<td>I</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$R_{OH}$</td>
<td>Pull-up Resistance</td>
<td>$5.0$</td>
<td>$10.0$</td>
<td>$10.0$</td>
<td>I</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$R_{OL}$</td>
<td>Pull-down Resistance</td>
<td>$5.0$</td>
<td>$10.0$</td>
<td>$10.0$</td>
<td>I</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>$1.0$</td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current Source/Sink</td>
<td>$50.0$</td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
</tr>
</tbody>
</table>

Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD}$</td>
<td>Supply Current into $V_{DD}$</td>
<td>$4.0$</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Operating Voltage</td>
<td>$4.5$</td>
<td>$15.0$</td>
<td>$15.0$</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

5-65
### AC Electrical Characteristics

(\(T_A = 25^\circ C, V_{DD} = 15V, C_{LOAD} = 1000 \text{ pF}, \text{unless otherwise specified}\))

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_R)</td>
<td>Rise Time</td>
<td>(C_L = 500 \text{ pF}) (C_L = 1000 \text{ pF})</td>
<td>15.0</td>
<td>20.0</td>
<td>40.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>(t_F)</td>
<td>Fall Time</td>
<td>(C_L = 500 \text{ pF}) (C_L = 1000 \text{ pF})</td>
<td>15.0</td>
<td>20.0</td>
<td>40.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{D\text{OFF}})</td>
<td>Turn Off Delay Time</td>
<td></td>
<td>90.0</td>
<td>140.0</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{D\text{ON}})</td>
<td>Turn On Delay Time</td>
<td></td>
<td>90.0</td>
<td>140.0</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

---

**Figure 2. EL7501 Test Circuit**

**Figure 3. EL7501 Alternate Drive Method**

---

5-66
Typical Performance Curves

Quiescent Supply Current vs Supply Voltage

Supply Voltage (V)

Output Rising Edge Delay Time vs Supply Voltage and Drive Voltage

Delay Time (ns)

Output Falling Edge Delay Time vs Supply Voltage and Drive Voltage

Delay Time (ns)

Supply Current vs DC Offset Voltage and VDD

Delay Time vs Temperature and Supply Voltage

Delay Time (ns)

Supply Voltage (V)

Temperature (C)
Typical Performance Curves — Contd.

Max. Power/Derating Curves
8-Pin Package

Input Threshold vs Supply Voltage

Input Current vs Input Voltage

Enable Threshold vs Supply Voltage

Peak Drive vs Supply Voltage

"On" Resistance vs Supply Voltage

Rise/Fall Time vs Load and Supply

Rise/Fall Time vs Temperature
Features
• 100V High Side Voltage
• Programmable Delay
• Direct Coupled
• No Start Up Ambiguity
• Rail to Rail Output
• 1 MHz Operation
• 1.0 Amp Peak Current
• Improved Response Times
• Matched Rise and Fall Times
• Low Supply Current
• Low Output Impedance
• Low Input Capacitance

Applications
• Uninterruptible Power Supplies
• Distributed Power Systems
• IGBT Drive
• DC-DC Converters
• Motor Control
• Power MOSFET Drive
• Switch Mode Power Supplies

General Description
The EL7661 provides a low cost solution to many full bridge applications. The EL7661 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from the DSET pins to VSS provides “dead time” programmability. Shorting the DSET pins to VDD gives the minimum delay (~100 ns).

Connection Diagram

Timing Diagram

*Pins 1, 9, 13, 15 must be open.
**EL7661C**

**100V Full Bridge Driver**

### Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

- **Supply (V_{HIA} and V_{HIB} to V_{SS})**
  - 100V
- **Supply (V_{DD} to GND)**
  - 16.5V
- **Input Pins**
  - \(-0.3V \text{ below } V_{SS}, \) +0.3V above \( V_{DD} \)
- **Operating Junction Temperature**
  - 125°C
- **Combined Peak Output Current**
  - 4A

### DC Electrical Characteristics

\( (T_A = 25^\circ C, V_{DD} = 15V, V_{SS} = 0V, C_{LOAD} = 1000 \text{ pF, unless otherwise specified}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IL} )</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>3.0</td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Logic &quot;1&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>1.8</td>
<td>0.8</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{HYS} )</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>IV</td>
<td>V</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Logic &quot;0&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( R_{OH} )</td>
<td>Pull-Up Resistance ( I_{OUT} = -100 \text{ mA} )</td>
<td></td>
<td>5.0</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( R_{OL} )</td>
<td>Pull-Down Resistance ( I_{OUT} = +100 \text{ mA} )</td>
<td></td>
<td>5.0</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( I_{PK} )</td>
<td>Peak Output Current</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>A</td>
</tr>
<tr>
<td>( I_{DC} )</td>
<td>Continuous Output Current Source/Sink</td>
<td></td>
<td>50.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
</tr>
</tbody>
</table>

### Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{DD} )</td>
<td>Supply Current into ( V_{DD} )</td>
<td>( R_{SET} = 5.1k )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Inputs ( = 5V )</td>
<td></td>
<td>15.0</td>
<td>I</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{HIA} )</td>
<td>Supply Current into ( V_{HIA} )</td>
<td></td>
<td>4.0</td>
<td>I</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{HIB} )</td>
<td>Supply Current into ( V_{HIB} )</td>
<td></td>
<td>4.0</td>
<td>I</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( V_{DD} )</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_4 = T_C = T_A \).
### AC Electrical Characteristics

\( T_A = 25^\circ C, \ V_{DD} = 15V, \ V_{SS} = 0V, \ C_{LOAD} = 1000 \ pF, \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_R )</td>
<td>Rise Time</td>
<td>( C_L = 500 \ pF ) \n( C_L = 1000 \ pF )</td>
<td>15.0</td>
<td>20.0</td>
<td>40.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_F )</td>
<td>Fall Time</td>
<td>( C_L = 500 \ pF ) \n( C_L = 1000 \ pF )</td>
<td>15.0</td>
<td>20.0</td>
<td>40.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_D ) ON HI</td>
<td>High Side Turn On Delay Time</td>
<td>( D_{SET} = V_{DD} ) \n( R_{SET} = 5.1k ) \n( R_{SET} = 200k )</td>
<td>50.0</td>
<td>75.0</td>
<td>100.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>75.0</td>
<td>125.0</td>
<td>200.0</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>750.0</td>
<td>1150.0</td>
<td>1500.0</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( t_D ) ON LO</td>
<td>Low Side Turn On Delay Time</td>
<td>( D_{SET} = V_{DD} ) \n( R_{SETLO} = 5.1k ) \n( R_{SETLO} = 200k )</td>
<td>50.0</td>
<td>75.0</td>
<td>100.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>75.0</td>
<td>125.0</td>
<td>200.0</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>750.0</td>
<td>1150.0</td>
<td>1500.0</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>( t_D ) OFF HI</td>
<td>High Side Turn Off Delay Time</td>
<td>( D_{SET} = V_{DD} )</td>
<td>100.0</td>
<td></td>
<td>150.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_D ) OFF LO</td>
<td>Low Side Turn Off Delay Time</td>
<td>( D_{SET} = V_{DD} )</td>
<td>100.0</td>
<td></td>
<td>150.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_D ) MISMATCH</td>
<td>( A_{HI} to A_{LO} ) Delay Mismatch</td>
<td>( D_{SET} = 200k )</td>
<td></td>
<td></td>
<td>+/-10.0</td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>( t_D ) MISMATCH</td>
<td>( B_{HI} to B_{LO} ) Delay Mismatch</td>
<td>( D_{SET} = 200k )</td>
<td></td>
<td></td>
<td>+/-10.0</td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>( t_D ) MISMATCH</td>
<td>( A_{HI} to B_{HI} ) Delay Mismatch</td>
<td>( D_{SET} = 200k )</td>
<td></td>
<td></td>
<td>+/-10.0</td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>( t_D ) MISMATCH</td>
<td>( A_{LO} to B_{LO} ) Delay Mismatch</td>
<td>( D_{SET} = 200k )</td>
<td></td>
<td></td>
<td>+/-10.0</td>
<td>I</td>
<td>%</td>
</tr>
</tbody>
</table>
### EL7661 Pin Description

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RAM</td>
<td>Internal circuit connection. This pin swings from VSS to VDD. This pin is out of phase with INA. Normally this pin should be unconnected to any external circuitry.</td>
</tr>
<tr>
<td>2</td>
<td>DSETLO</td>
<td>Connection for the delay setting resistor. This pin must be connected externally to the DSETHI pin. This pin is connected internally to a PMOS diode referenced to VDD.</td>
</tr>
<tr>
<td>3</td>
<td>INB</td>
<td>Digital input for the &quot;B&quot; drivers. Its polarity is non-inverting with respect to the &quot;B&quot; outputs.</td>
</tr>
<tr>
<td>4</td>
<td>BLO</td>
<td>&quot;B&quot; lo-side output. Swings from VSS to VDD.</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
<td>Positive supply for the lo-side circuitry.</td>
</tr>
<tr>
<td>6</td>
<td>ALO</td>
<td>&quot;A&quot; lo-side output. Swings from VSS to VDD.</td>
</tr>
<tr>
<td>7</td>
<td>INA</td>
<td>Digital input for the &quot;A&quot; drivers. Its polarity is non-inverting with respect to the &quot;A&quot; outputs.</td>
</tr>
<tr>
<td>8</td>
<td>DSETHI</td>
<td>Connection for the delay setting resistor. This pin must be connected externally to the DSETLO pin. This pin is connected internally to a PMOS diode referenced to VDD.</td>
</tr>
<tr>
<td>9</td>
<td>RBP</td>
<td>Internal circuit connection. This pin swings from VSS to VDD. It is in phase with INB. Normally this pin should be unconnected to any external circuitry.</td>
</tr>
<tr>
<td>10</td>
<td>LX2</td>
<td>Negative supply for the &quot;B&quot; hi-side driver.</td>
</tr>
<tr>
<td>11</td>
<td>BHI</td>
<td>&quot;B&quot; hi-side output. Swings from LX2 to VHB.</td>
</tr>
<tr>
<td>12</td>
<td>VHB</td>
<td>Positive supply for the &quot;B&quot; hi-side driver.</td>
</tr>
<tr>
<td>13</td>
<td>RBP</td>
<td>Internal circuit connection. This pin swings from VSS to VDD. It is out of phase with INB. Normally this pin should be unconnected to any external circuitry.</td>
</tr>
<tr>
<td>14</td>
<td>VSS</td>
<td>Negative supply for lo-side circuitry.</td>
</tr>
<tr>
<td>15</td>
<td>RAP</td>
<td>Internal circuit connection. This pin swings from VSS to VDD. It is in phase with INA. Normally this pin should be unconnected to any external circuitry.</td>
</tr>
<tr>
<td>16</td>
<td>LX1</td>
<td>Negative supply for the &quot;A&quot; hi-side driver.</td>
</tr>
<tr>
<td>17</td>
<td>AHI</td>
<td>&quot;A&quot; hi-side output. Swings from LX1 to VHA.</td>
</tr>
<tr>
<td>18</td>
<td>VHA</td>
<td>Positive supply for the &quot;A&quot; hi-side driver.</td>
</tr>
</tbody>
</table>
Typical Performance Curves

**Quiescent Supply Current vs Supply Current**

![Graph showing quiescent supply current vs supply current](image)

- TA = 25°C
- DSET = VDD

**Average Supply Current into VDD vs Voltage and Frequency**

![Graph showing average supply current into VDD vs voltage and frequency](image)

- CLOAD = 1000 pF
- DSET = VDD

**Average Supply Current into VHI vs Voltage and Frequency**

![Graph showing average supply current into VHI vs voltage and frequency](image)

- CLOAD = 1000 pF
- DSET = VDD

**Output Rising Edge Delay vs RSET and Supply Voltage**

![Graph showing output rising edge delay vs RSET and supply voltage](image)

- VDD = 5V
- VDD = 10V
- VDD = 12V
- VDD = 15V
- TA = 25°C
- CLOAD = 1000 pF

**Output Rising Edge Delay vs RSET and Supply Voltage (Detail)**

![Graph showing output rising edge delay vs RSET and supply voltage detail](image)

- VDD = 5V
- VDD = 10V
- VDD = 12V
- VDD = 15V
- TA = 25°C
- CLOAD = 1000 pF

**Output Falling Edge Delay vs Supply Voltage and Temperature**

![Graph showing output falling edge delay vs supply voltage and temperature](image)

- DSET = VDD
- TA = 25°C
- TA = 125°C
- TA = -55°C
Typical Performance Curves — Contd.

- **Power Dissipation vs Temperature**
- **Input Threshold vs Supply Voltage**
- **Input Current vs Input Voltage**

- **Peak Drive vs Supply Voltage**
- **"On" Resistance vs Supply Voltage**
- **Rise/Fall Time vs Load and Supply**
- **Rise/Fall Time vs Temperature**
Theory of Operation
The EL7661 consists of, among other things, 4 CMOS super inverter output stages. The super inverter configuration minimizes the possibility of simultaneous conduction of the two output complementary MOS devices. Each output stage can source or sink up to 1 amp of peak current. The state of the two output stages denoted "A\textsubscript{LO}" and "A\textsubscript{HI}" is determined by the input "IN\textsubscript{A}". In a like manner the state of the two output stages denoted "B\textsubscript{LO}" and "B\textsubscript{HI}" is determined by the input "IN\textsubscript{B}". The lo-side output stages, "A\textsubscript{LO}" and "B\textsubscript{LO}" have \textit{VSS} as their negative supply and \textit{VDD} as their positive supply. The negative supply of the "A\textsubscript{HI}" output stage is L\textsubscript{XA}. The positive supply of the "A\textsubscript{HI}" output stage is VH\textsubscript{IA}. Similarly, the positive and negative supplies of the "B\textsubscript{HI}" output stage are denoted V\textsubscript{HIB} and L\textsubscript{XB}. The hi-side supplies, L\textsubscript{XA}, L\textsubscript{XB}, V\textsubscript{HIA}, and V\textsubscript{HIB} can float with respect to \textit{VSS}. In fact the hi-side supplies can easily be 100V higher than \textit{VSS}. However, the differential voltage between V\textsubscript{HIA} and L\textsubscript{XA}, and between V\textsubscript{HIB} and L\textsubscript{XB}, should never exceed 15V.

The input signals, IN\textsubscript{A} and IN\textsubscript{B}, are level shifted from their quasi TTL levels to \textit{VSS} to \textit{VDD} voltages. After the level shift stage the rising edge of the signal is delayed some amount determined by the value of the resistor at the D\textsubscript{SET} pin. (The falling edge of the signal has no extra delay added to it at this stage.) The delayed signal then drives its respective output drivers. The signals which drive the hi-side drivers are level shifted up to the appropriate levels while the signals which drive the lo-side drivers have an additional delay added to mimic the delay inherent in the hi-side level shift circuitry.

The circuitry which produces the resistor controlled delay of the rising edge of the output reduces down to a simple RC time constant. The R is provided by the user and the C is built into the delay circuitry. Ideally the delay would have no dependency on supply voltage or temperature since the R and C are well controlled, however, due to nonidealities of the exact implementation, the delay times are a weak function of supply voltage and temperature.
Macromodel

****EL7661 model****
***top level circuit starts here***
*· a-input
*· b-input
*· a lo-side output
*· b lo-side output
*· a hi-side output
*· b hi-side output
*· a hi-side neg supply
*· b hi-side neg supply
*· lo-side neg supply
*· a hi-side pos supply
*· b hi-side pos supply
*· lo-side pos supply
*·
.subckt M7661 ina inb alo blo ahi bhi lxa lxb vss vhia vhib vdd

****top level subcircuit calls****
x dela ina outa vss delay
x delb inb outb vss delay
xalo alo outa vdd vss vss outstg
xblo blo outb vdd vss vss outstg
xahi ahi outa vhia lxa vss outstg
xbhi bhi outb vhib lxb vss outstg
.ends M7661

****put in value of rset resistor here****
.param rset = 50e3

****comparator subcircuit****
.subckt comp10 out inp inm vss
el out vss table (v(inp)–v(inm))*5000 (0,0,15,15)
rout out vss 10meg
rinp inp vss 10meg
rimm inm vss 10meg
.ends comp10
Macromodel — Contd.

****input, delay, and level shift subcircuit****

```
.subckt delay vin compout vss
vinref vinref vss 1.8
x1 n1 vin vinref vss comp10
rslow n1 n5 | rset |
rnom n5 n2 25k
cdelay n2 vss 7.5p
ddelay n4 n1 modd
rfast n4 n2 110k
rdiv1 vddint n3 1k
rdiv2 n3 vss 1k
x2 compout n3 n2 vss comp10
vddint vddint vss 15
.model modd d is = 1e-7
.ends delay
```

****5 ohm output stage subcircuit****

```
.subckt outstg out gate vhi lx vss
sp vhi out gate vss spmod
sn out 1x gate vss snmod
.model spmod vswitch ron = 5 roff = 2meg von = 2.5 voff = 4.5
.model snmod vswitch ron = 5 roff = 2meg von = 7.5 voff = 5.5
.ends outstg
```
Macromodel — Contd.

EL7661 Macromodel Schematic

- **V<sub>HIB</sub>**
- **V<sub>HI</sub>**
- **L<sub>x</sub>A**
- **B<sub>HI</sub>**
- **A<sub>HI</sub>**
- **V<sub>DD</sub>**
- **B<sub>LO</sub>**
- **R<sub>FAST</sub> 1k**
- **R<sub>NOM</sub> 110k**
- **R<sub>NOM</sub> 25k**
- **C<sub>DELAY</sub> 7.5pF**

- **IN<sub>A</sub>**
- **IN<sub>B</sub>**

[Image of the schematic diagram]
**Features**
- 100V High Side Voltage
- Programmable Delay
- Direct Coupled
- No Start Up Ambiguity
- Rail to Rail Output
- 1 MHz Operation
- Shutdown Function
- 1.0 Amp Peak Current
- Improved Response Times
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

**Applications**
- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

**General Description**
The EL7761 provides a low cost solution to many half bridge applications. The EL7761 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from DSET to GND provides "dead time" programmability. Shorting DSET to VDD gives the shortest delay (~100 ns).

The POL pin controls the polarity of the low side driver. The polarity of the upper driver is always inverting. The EN pin, when low, forces the high and low side outputs into their low state.

**Connection Diagram**

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7761CN</td>
<td>-40°C to +85°C</td>
<td>16-Pin</td>
<td>P-DIP</td>
</tr>
<tr>
<td>EL7761CS</td>
<td>-40°C to +85°C</td>
<td>16-Pin</td>
<td>SOIC</td>
</tr>
</tbody>
</table>

*Contact factory

**Polarity Table**

<table>
<thead>
<tr>
<th>POL</th>
<th>Polarity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>GND</td>
</tr>
<tr>
<td>Hi</td>
<td>X</td>
</tr>
</tbody>
</table>

*Inverting

Non-Inverting

**EL7761 Waveform Example**

\[
T_{D_{LO}} = T_{D_{HI}}
\]

POL = VDD

January 1996 Rev C
### Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply ((V_{HI} \text{ to } GND))</td>
<td>100V</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Supply ((V_{DD} \text{ to } GND))</td>
<td>16.5V</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3V below GND, +0.3V above (V_{DD})</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Peak Current per Output</td>
<td>2A</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td>-65(^\circ)C to +150(^\circ)C</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td></td>
<td></td>
<td>-40(^\circ)C to +85(^\circ)C</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td></td>
<td></td>
<td>125(^\circ)C</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Power Dissipation ((SOIC))</td>
<td></td>
<td></td>
<td>1100 mA</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>Power Dissipation ((PDIP))</td>
<td></td>
<td></td>
<td>1800 mA</td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

#### DC Electrical Characteristics \((T_A = 25^\circ C, V_{DD} = 15V, C_{LOAD} = 1000pF, \text{unless otherwise specified})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IH})</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>3.0</td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IH})</td>
<td>Logic &quot;1&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td>I</td>
<td>(\mu)A</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>1.8</td>
<td>0.8</td>
<td>I</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IL})</td>
<td>Logic &quot;0&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td>I</td>
<td>(\mu)A</td>
<td>V</td>
</tr>
<tr>
<td>(V_{HVS})</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>(V_{ENH})</td>
<td>Enable Threshold</td>
<td>Positive Edge</td>
<td>2.8</td>
<td>1.6</td>
<td>I</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>(V_{ENL})</td>
<td>Disable Threshold</td>
<td>Negative Edge</td>
<td>0.9</td>
<td>0.6</td>
<td>I</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>(V_{EN HYS})</td>
<td>Enable Hysteresis</td>
<td></td>
<td>0.7</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>(I_{DS \text{ OFF}})</td>
<td>Output Leakage ((GND \leq V_{OUT} \leq V_{DD}))</td>
<td></td>
<td>-10.0</td>
<td>0.2</td>
<td>10.0</td>
<td>I</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(R_{OH})</td>
<td>Pull-up Resistance (I_{OUT} = -100 \text{ mA})</td>
<td></td>
<td>5.0</td>
<td>10.0</td>
<td>I</td>
<td>(\Omega)</td>
<td>V</td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Pull-down Resistance (I_{OUT} = +100 \text{ mA})</td>
<td></td>
<td>5.0</td>
<td>10.0</td>
<td>I</td>
<td>(\Omega)</td>
<td>V</td>
</tr>
<tr>
<td>(I_{PK})</td>
<td>Peak Output Current</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{DC})</td>
<td>Continuous Output Current Source/Sink</td>
<td></td>
<td>50.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
</tr>
</tbody>
</table>

#### Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{DD})</td>
<td>Supply Current into (V_{DD}) (R_{SET} = 5.1k)</td>
<td>6.0</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{HI})</td>
<td>Supply Current into (V_{HI})</td>
<td>2.0</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{DD \text{ OFF}})</td>
<td>Supply Current into (V_{DD}) (V_{EN} = 0.6V)</td>
<td>750.0</td>
<td>I</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(V_{DD})</td>
<td>Operating Voltage</td>
<td>4.5</td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min./Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LITX?? Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_{J} = T_{C} = T_{A}\).
## AC Electrical Characteristics

(T<sub>A</sub> = 25°C, V<sub>DD</sub> = 15V, C<sub>LOAD</sub> = 1000pF, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Rise Time</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 500pF</td>
<td>15.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 1000pF</td>
<td>20.0</td>
<td>40.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;F&lt;/sub&gt;</td>
<td>Fall Time</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 500pF</td>
<td>15.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 1000pF</td>
<td>20.0</td>
<td>40.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;D ON HI&lt;/sub&gt;</td>
<td>High Side Turn On Delay Time</td>
<td>D&lt;sub&gt;SET&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>50.0</td>
<td>100.0</td>
<td>150.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;SET&lt;/sub&gt; = 5.1k</td>
<td>75.0</td>
<td>125.0</td>
<td>200.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;SET&lt;/sub&gt; = 400k</td>
<td>750.0</td>
<td>1150.0</td>
<td>1500.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;D ON LO&lt;/sub&gt;</td>
<td>Low Side Turn On Delay Time</td>
<td>D&lt;sub&gt;SET&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>50.0</td>
<td>100.0</td>
<td>150.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;SET&lt;/sub&gt; = 5.1k</td>
<td>75.0</td>
<td>125.0</td>
<td>200.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;SET&lt;/sub&gt; = 400k</td>
<td>750.0</td>
<td>1150.0</td>
<td>1500.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;D OFF HI&lt;/sub&gt;</td>
<td>High Side Turn Off Delay Time</td>
<td>D&lt;sub&gt;SET&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>100.0</td>
<td></td>
<td>150.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;D OFF LO&lt;/sub&gt;</td>
<td>Low Side Turn Off Delay Time</td>
<td>D&lt;sub&gt;SET&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>100.0</td>
<td></td>
<td>150.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;D MISMATCH&lt;/sub&gt;</td>
<td>High to Lo Side Turn On Delay Mismatch</td>
<td>R&lt;sub&gt;SET&lt;/sub&gt; = 400k</td>
<td>±10.0</td>
<td></td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
</tbody>
</table>

### Pin Description

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V&lt;sub&gt;HI&lt;/sub&gt;</td>
<td>Positive supply for the high side driver.</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>R&lt;sup&gt;-&lt;/sup&gt;</td>
<td>Internal connection between the low side and high side driver. This pin is normally unconnected.</td>
</tr>
<tr>
<td>4</td>
<td>POL</td>
<td>Controls the polarity of the low side driver.</td>
</tr>
<tr>
<td>5</td>
<td>IN&lt;sub&gt;HI&lt;/sub&gt;</td>
<td>Logic input for the high side driver.</td>
</tr>
<tr>
<td>6</td>
<td>IN&lt;sub&gt;LO&lt;/sub&gt;</td>
<td>Logic input for the low side driver.</td>
</tr>
<tr>
<td>7</td>
<td>D&lt;sub&gt;SET&lt;/sub&gt;</td>
<td>Connection for the delay adjust resistor.</td>
</tr>
<tr>
<td>8</td>
<td>EN</td>
<td>A high voltage on this pin enables the part.</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Negative supply of the low side driver and control circuitry.</td>
</tr>
<tr>
<td>10</td>
<td>N&lt;sub&gt;LO&lt;/sub&gt;</td>
<td>Low side driver output pull down.</td>
</tr>
<tr>
<td>11</td>
<td>P&lt;sub&gt;LO&lt;/sub&gt;</td>
<td>Low side driver output pull up.</td>
</tr>
<tr>
<td>12</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Positive supply of the low side driver and control circuitry.</td>
</tr>
<tr>
<td>13</td>
<td>R&lt;sup&gt;+&lt;/sup&gt;</td>
<td>Internal connection between the low side and high side driver. This pin is normally unconnected.</td>
</tr>
<tr>
<td>14</td>
<td>LX</td>
<td>Negative supply for the high side driver.</td>
</tr>
<tr>
<td>15</td>
<td>N&lt;sub&gt;HI&lt;/sub&gt;</td>
<td>High side driver output pull down.</td>
</tr>
<tr>
<td>16</td>
<td>P&lt;sub&gt;HI&lt;/sub&gt;</td>
<td>High side driver output pull up.</td>
</tr>
</tbody>
</table>
Typical Performance Curves

Quiescent Supply Current vs. Supply Voltage

Avg. Supply Current into VDD vs. Voltage and Frequency

Average Supply Current into VHI vs. Voltage and Frequency

Output Rising Edge Delay vs. RsET and Supply Voltage

Output Rising Edge Delay vs. RsET and Supply Voltage (Detail)

Output Falling Edge Delay vs. Supply Voltage and Temperature

Delay Times* vs. Supply Voltage and Temperature

*Minimum Rising and Falling Edge Delay Times
Typical Performance Curves — Contd.

Max. Power/Derating Curves

16 Pin Package

Input Threshold vs. Supply Voltage

Input Current vs. Input Voltage

Enable Threshold vs. Supply Voltage

Peak Drive vs. Supply Voltage

"On" Resistance vs. Supply Voltage

Rise/Fall Time vs.
Load and Supply

Rise/Fall Time vs.
Temperature
Features
• Programmable Delay
• 1 MHz Operation
• Shutdown Function
• 1.0 Amp Peak Current
• Matched Rise and Fall Times
• Low Supply Current
• Low Output Impedance
• Low Input Capacitance

Applications
• Uninterruptible Power Supplies
• Distributed Power Systems
• IGBT Drive
• DC-DC Converters
• Motor Control
• Power MOSFET Drive
• Switch Mode Power Supplies

General Description
The EL7861 provides 1.0A of peak current for many driver applications. The rising edge of the output can be delayed up to 1.5 \( \mu \text{s} \) from the corresponding input edge. A single resistor from \( \text{DSET} \) to GND sets the delay time. Connecting the \( \text{DSET} \) pin to \( \text{VDD} \) disables the delay block giving approximately 30 ns delay times. The circuit contains an enable feature as well as user definable polarity. The programmable delay is useful in applications requiring compensation for long switch turn off times and applications using resonant mode technology.

Connection Diagram

<table>
<thead>
<tr>
<th>POL</th>
<th>Polarity</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{VDD} )</td>
<td>Non-Inverting</td>
</tr>
<tr>
<td>GND</td>
<td>Inverting</td>
</tr>
</tbody>
</table>

7861 Waveform Example
\( \text{POL} = \text{VDD} \)

\( \text{PD} \) shorted to \( \text{ND} \)
### Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V(\text{DD}) to GND)</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3V below GND, +0.3V above V(\text{DD})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>2A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics \((T_A = 25°C, V\(\text{DD}\) = 15V, C\(\text{LOAD}\) = 1000 pF, unless otherwise specified)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IH}})</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>3.0</td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_{\text{IH}})</td>
<td>Logic &quot;1&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td>I</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{IL}})</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>1.6</td>
<td>0.8</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{IL}})</td>
<td>Logic &quot;0&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td>I</td>
<td>(\mu A)</td>
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<tr>
<td>(V_{\text{HYS}})</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
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<tr>
<td>(V_{\text{ENH}})</td>
<td>Enable Threshold</td>
<td>Positive Edge</td>
<td>2.8</td>
<td>1.6</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{ENL}})</td>
<td>Disable Threshold</td>
<td>Negative Edge</td>
<td>0.9</td>
<td>0.6</td>
<td></td>
<td>I</td>
<td>V</td>
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<tr>
<td>(V_{\text{HYS}})</td>
<td>Enable Hysteresis</td>
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<td>0.7</td>
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<td>V</td>
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<tr>
<td>(I_{\text{DS OFF}})</td>
<td>Output Leakage</td>
<td>GND (\leq V_{\text{OUT}} \leq V_{\text{DD}})</td>
<td>0.2</td>
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<tr>
<td>(R_{\text{OH}})</td>
<td>Pull-Up Resistance</td>
<td>(I_{\text{OUT}} = -100 \text{ mA})</td>
<td>5.0</td>
<td>10.0</td>
<td>I</td>
<td>(\Omega)</td>
<td></td>
</tr>
<tr>
<td>(R_{\text{OL}})</td>
<td>Pull-Down Resistance</td>
<td>(I_{\text{OUT}} = +100 \text{ mA})</td>
<td>5.0</td>
<td>10.0</td>
<td>I</td>
<td>(\Omega)</td>
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<tr>
<td>(I_{\text{PK}})</td>
<td>Peak Output Current</td>
<td></td>
<td>1.0</td>
<td></td>
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<td>IV</td>
<td>A</td>
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<tr>
<td>(I_{\text{DC}})</td>
<td>Continuous Output Current Source/Sink</td>
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<td>50.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
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### Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td>(I_{\text{DD}})</td>
<td>Supply Current into V(\text{DD})</td>
<td>(R_{\text{SET}} = 5.1k)</td>
<td>6.0</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>mA</td>
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<tr>
<td>(I_{\text{DD OFF}})</td>
<td>Supply Current into V(\text{DD})</td>
<td>(V_{\text{EN}} = 0.6V)</td>
<td></td>
<td>750.0</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
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<tr>
<td>(V_{\text{DD}})</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
**AC Electrical Characteristics** *(TA = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<td>t_{R}</td>
<td>Rise Time</td>
<td>CL = 500 pF</td>
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<td>15.0</td>
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<td>ns</td>
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<td></td>
<td></td>
<td>CL = 1000 pF</td>
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<td>20.0</td>
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<td>40.0</td>
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<td>t_{F}</td>
<td>Fall Time</td>
<td>CL = 500 pF</td>
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<td></td>
<td>15.0</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>CL = 1000 pF</td>
<td></td>
<td></td>
<td>20.0</td>
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<td>t_{D ON}</td>
<td>Turn On Delay Time</td>
<td>D\text{SET} = V_{DD}</td>
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<td></td>
<td>10.0</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>R\text{SET} = 5.1k</td>
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<td>25.0</td>
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<td></td>
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<td>R\text{SET} = 400k</td>
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<td>750.0</td>
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<td></td>
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<td>1500.0</td>
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<td>t_{D OFF}</td>
<td>Turn Off Delay Time</td>
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<td>ns</td>
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<td>50.0</td>
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</tbody>
</table>
Typical Performance Curves

Quiescent Supply Current vs Supply Voltage

Average Supply Current vs Voltage and Frequency

Delay Times vs Supply Voltage and Temp

Output Rising Edge Delay vs \( R_{SET} \) and Supply Voltage

Output Rising Edge Delay vs \( R_{SET} \) and Supply Voltage (Detail)

Output Rising Edge Delay Change vs Temperature

Output Falling Edge Delay vs \( R_{SET} \) and \( V_{DD} \)

Output Falling Edge Delay vs Temperature and \( R_{SET} \)
Typical Performance Curves — Contd.

Max. Power/Derating Curves 8-Pin Package

Input Threshold vs. Supply Voltage

Input Current vs Input Voltage

Enable Threshold vs Supply Voltage

Peak Drive vs Supply Voltage

"On" Resistance vs Supply Voltage

Rise/Fall Time vs Load and Supply

Rise/Fall Time vs Temperature
Features
• Programmable delay
• 1 MHz operation
• 1.0A peak current
• Matched rise/fall times
• Low power
• Rail to rail output
• Low output impedance
• Low input capacitance

Applications
• Uninterruptible power supplies
• IGBT driver
• DC-DC converters
• Motor control
• Power MOSFET drivers
• Switch mode power supplies

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7961CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL7961CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL7971CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL7971CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
<tr>
<td>EL7981CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
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<tr>
<td>EL7981CS</td>
<td>-40°C to +85°C</td>
<td>8-Lead SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

General Description
The EL7961/EL7971/EL7981 provides 1.0A peak current for many driver applications. The rising edge of the output can be delayed up to 1.5 μs from the input edge. A resistor from DSET to GND sets the delay time for both channel A and B. This programmable delay is useful in applications requiring compensation for long switch turn off times. Pulling DSET high disables the delay block giving approximately 30 ns delay times.

EL7961 - Non-Inverting
EL7971 - Inverting
EL7981 - Channel A - Inverting
Channel B - Non-Inverting

Connection Diagram

7961 Waveform Example

INa/B

OUTA

OUTB

3V

0V

VDD

0V

VDD

0V
# Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

- **Supply** \( (V_{DD} \text{ to } GND) \): 16.5V
- **Input Pins**: 
  - 0.3V below GND, +0.3V above \( V_{DD} \)
- **Operating Junction Temperature**: 125°C
- **Peak Output Current**: 2A
- **Ambient Operating Temperature**: 
  - SOIC: 125°C
  - PDIP: 125°C
- **Storage Temperature Range**: 
  - SOIC: -40°C to +85°C
  - PDIP: -65°C to +150°C
- **Power Dissipation**: 
  - SOIC: 570 mW
  - PDIP: 1050 mW

## Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

## Test Level

- **Test Procedure**
  - I: 100% production tested and QA sample tested per QA test plan QCX0002.
  - II: 100% production tested at \( T_A = 25^\circ C \) and QA sample tested at \( T_A = 25^\circ C \), \( T_{MAX} \) and \( T_{MIN} \) per QA test plan QCX0002.
  - III: QA sample tested per QA test plan QCX0002.
  - IV: Parameter is guaranteed (but not tested) by Design and Characterization Data.
  - V: Parameter is typical value at \( T_A = 25^\circ C \) for information purposes only.

## DC Electrical Characteristics \( (T_A = 25^\circ C, V_{DD} = 15V, C_{LOAD} = 1000 \text{ pF unless otherwise specified}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>3.0</td>
<td>2.4</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Logic &quot;1&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td>I</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>1.8</td>
<td>0.8</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Logic &quot;0&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td>I</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( V_{HYS} )</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ENH} )</td>
<td>Enable Threshold</td>
<td>Positive Edge</td>
<td>2.8</td>
<td>1.6</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ENL} )</td>
<td>Disable Threshold</td>
<td>Negative Edge</td>
<td>0.9</td>
<td>0.6</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>( V_{EN-HYS} )</td>
<td>Enable Hysteresis</td>
<td></td>
<td>0.7</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>( R_{OH} )</td>
<td>Pull-up Resistance</td>
<td>( I_{OUT} = -100 \text{ mA} )</td>
<td>5.0</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( R_{OL} )</td>
<td>Pull-down Resistance</td>
<td>( I_{OUT} = +100 \text{ mA} )</td>
<td>5.0</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( I_{PK} )</td>
<td>Peak Output Current</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>A</td>
</tr>
<tr>
<td>( I_{DC} )</td>
<td>Continuous Output Current Source/Sink</td>
<td></td>
<td>50.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
</tr>
</tbody>
</table>

## Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{DD} )</td>
<td>Supply Current into ( V_{DD} )</td>
<td>( R_{SET} = 5.1k ) ( \text{ Inputs} = 15V )</td>
<td>10.0</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{DD-OFF} )</td>
<td>Supply Current into ( V_{DD} )</td>
<td>( V_{EN} = 0V )</td>
<td>1.5</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{DD} )</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>15.0</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics (TA = 25°C, VDD = 15V, CLOAD = 1000 pF unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| t\(_R\)          | Rise Time                        | C\(_L\) = 500 pF  
                      |                   | C\(_L\) = 1000 pF | 15.0 | 20.0 | 40.0 | IV         | ns    |
| t\(_F\)          | Fall Time                        | C\(_L\) = 500 pF  
                      |                   | C\(_L\) = 1000 pF | 15.0 | 20.0 | 40.0 | IV         | ns    |
| t\(_D\)\(_ON\)   | Turn On Delay Time               | D\(_SET\) = VDD  
                      |                   | R\(_SET\) = 5.1k  
                      |                   | R\(_SET\) = 200k  | 10.0 | 30.0 | 30.0 | 50.0 | IV | ns |
| t\(_D\)\(_OFF\)  | Turn Off Delay Time              | D\(_SET\) = VDD  
                      |                   |                       | 30.0 | 50.0 | 50.0 | IV | ns |
| t\(_D\)\(_MISMATCH\) | Channel A to B 
                      |                   |                   | R\(_SET\) = 200k  |       | ±15.0 | I    | %    |
Typical Performance Curves

**Quiescent Supply Current vs Supply Voltage**

Supply Voltage (V) vs. Supply Current (mA)

- @7961
- @7971
- @7981

**Average Supply Current vs Voltage and Frequency**

Supply Voltage (V) vs. Supply Current (mA)

- @7961
- @7971
- @7981

**Delay Times vs Supply Voltage and Temperature**

Delay Time (ns) vs. Supply Voltage (V)

- @7961
- @7971
- @7981

**Output Rising Edge Delay vs \( R_{SET} \) and Supply Voltage**

Delay Time (ns) vs. \( R_{SET} \) (KΩ) at different Supply Voltages (V)

- 6V
- 10V
- 15V

**Output Rising Edge Delay vs Rising Edge Delay Percentage Change vs Temperature**

Delay Time (ns) vs. Temperature (°C)

- \( R_{SET} = 5.1K \)
- \( R_{SET} = 10K \)
- \( R_{SET} = 300K \)

**Output Falling Edge Delay vs \( R_{SET} \) vs \( V_{DD} \)**

Delay Time (ns) vs. \( R_{SET} \) (KΩ) at different Supply Voltages (V)

- 10V
- 12V
- 15V

**Output Falling Edge Delay vs Temperature and \( R_{SET} \)**

Delay Time (ns) vs. Temperature (°C)

- \( R_{SET} = 5.1K \)
- \( R_{SET} = 10K \)
- \( R_{SET} = 100K \)

**Output Rising Edge Delay Channel to Channel Mismatch vs \( R_{SET} \)**

Mismatch (ns) vs. \( R_{SET} \) (KΩ)

- \( -55°C \) to \( +125°C \)
- \( V_{DD} = 15V \)
- \( C_{LOAD} = 1000pf \)
Typical Performance Curves — Contd.

Max Power/Derating Curves

8-Pin Package

Input Threshold vs Supply Voltage

Input Current vs Input Voltage

Enable Threshold vs Supply Voltage

Peak Drive vs Supply Voltage

"On" Resistance vs Supply Voltage

Rise/Fall Time vs Load and Supply

Rise/Fall Time vs Temperature

Enable Threshold

Peak Drive

"On" Resistance

Rise/Fall Time
EL7962C/EL7972C/EL7982C
Dual Rising Edge Delay Driver

Features
- Programmable delay
- 1 MHz operation
- 1.0A peak current
- Matched rise and fall times
- Low supply current
- Rail-to-Rail output
- Low output impedance
- Low input capacitance

Applications
- Uninterruptible power supplies
- Distributed power systems
- IGBT drive
- DC-DC converters
- Motor control
- Power MOSFET drive
- Switch mode power supplies

General Description
The EL7962/72/82 provides 1.0A of peak current for many driver applications. The rising edge of the output can be delayed up to 1.5 μs from the corresponding input edge. A resistor from DSET_A to GND sets the delay time for channel A. Likewise a resistor from DSET_B to GND sets the delay time for channel B. Connecting the DSET_A pin to VDD disables the delay blocks, giving approximately 30 ns delay times for both channels. This programmable delay is useful in applications requiring compensation for long switch turn off times and applications using resonant mode technology.

EL7962 - both channels non-inverting
EL7972 - both channels inverting
EL7982 - channel A inverting, channel B non-inverting

Connection Diagram

7962 Waveform Example
T_D_A ≠ T_D_B

RSET_B > RSET_A → T_DB > T_DA
### Absolute Maximum Ratings \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply ((V_{DD} \text{ to GND}))</td>
<td>16.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3V below GND, +0.3V above (V_{DD})</td>
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<tr>
<td>Peak Current per Output</td>
<td>2A</td>
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</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
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</tr>
<tr>
<td>Power Dissipation</td>
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</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
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<td>Operating Junction Temperature</td>
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<td>Temperature Range</td>
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<tr>
<td>Important Note</td>
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</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_x = T_C = T_A\).

### DC Electrical Characteristics \((T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 \text{ pF}, \text{unless otherwise specified})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IH})</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>3.0</td>
<td>2.4</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IH})</td>
<td>Logic &quot;1&quot; Input Current</td>
<td></td>
<td>0.1</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>1.8</td>
<td>0.8</td>
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<td>V</td>
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<tr>
<td>(I_{IL})</td>
<td>Logic &quot;0&quot; Input Current</td>
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<td>0.1</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
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<tr>
<td>(V_{HVS})</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>(R_{OH})</td>
<td>Pull-up Resistance (I_{OUT} = -100 \text{ mA})</td>
<td></td>
<td>5.0</td>
<td>10.0</td>
<td></td>
<td>I</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(R_{OL})</td>
<td>Pull-down Resistance (I_{OUT} = +100 \text{ mA})</td>
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<td>5.0</td>
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<td>I</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(I_{PK})</td>
<td>Peak Output Current</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>IV</td>
<td>A</td>
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<tr>
<td>(I_{DC})</td>
<td>Continuous Output Current Source/Sink</td>
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<td>50</td>
<td></td>
<td></td>
<td>IV</td>
<td>mA</td>
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### Power Supply

<table>
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<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{DD})</td>
<td>Supply Current into (V_{DD}) (R_{SET} = 5.1k) Inputs = 15V</td>
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<td>12.0</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
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<tr>
<td>(V_{DD})</td>
<td>Operating Voltage</td>
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<td>4.5</td>
<td>15.0</td>
<td></td>
<td>I</td>
<td>V</td>
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</table>

5-95
## AC Electrical Characteristics (TA = 25°C, VDD = 15V, CLOAD = 1000 pF, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>tR</td>
<td>Rise Time</td>
<td>CL = 500 pF</td>
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<td></td>
<td>20.0</td>
<td>40.0</td>
<td>IV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 1000 pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tF</td>
<td>Fall Time</td>
<td>CL = 500 pF</td>
<td>15.0</td>
<td></td>
<td>20.0</td>
<td>40.0</td>
<td>IV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 1000 pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDON</td>
<td>Turn On Delay Time</td>
<td>DSET = VDD</td>
<td>10.0</td>
<td>30.0</td>
<td>50.0</td>
<td></td>
<td>IV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSET = 5.1k</td>
<td>30.0</td>
<td>60.0</td>
<td>120.0</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSET = 400k</td>
<td>750.0</td>
<td>1150.0</td>
<td>1500.0</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td>tDOFF</td>
<td>Turn Off Delay Time</td>
<td>DSET = VDD</td>
<td>30.0</td>
<td></td>
<td>50.0</td>
<td></td>
<td>IV</td>
</tr>
<tr>
<td>tDMISMATCH</td>
<td>Channel A to B Turn On Delay Mismatch</td>
<td>RSET = 400k</td>
<td>±10.0</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
</tr>
</tbody>
</table>
Typical Performance Curves

- **Quiescent Supply Current vs Supply Voltage**
- **Average Supply Current vs Voltage and Frequency**
- **Delay Times vs Supply Voltage and Temp.**
- **Output Rising Edge Delay vs \( R_{SET} \) and Supply Voltage**
- **Output Rising Edge Delay vs \( R_{SET} \) and Supply Voltage (Detail)**
- **Output Rising Edge Delay Percentage Change vs Temperature**
- **Output Falling Edge Delay vs \( R_{SET} \) vs \( V_{DD} \)**
- **Output Falling Edge Delay vs Temperature and \( R_{SET} \)**
- **Output Rising Edge Delay Channel to Channel Mismatch**
Typical Performance Curves — Contd.

Max Power/Derating Curves 8-Pin Package

Input Threshold vs Supply Voltage

Input Current vs Input Voltage

Enable Threshold vs Supply Voltage

Peak Drive vs Supply Voltage

"On" Resistance vs Supply Voltage

Rise/Fall Time vs Load and Supply

Rise/Fall Time vs Temperature
Variable Pulse Width Variable Frequency Pulse Generator

This application uses the "B" driver of the EL7972 as an oscillator to drive the "A" driver. The frequency is set using R1 and C1. The pulse width is set by adjusting R2. Capacitors C2, C3 and C4 are decoupling capacitors. A fixed pulse width output is available at pin 5 while the variable pulse width signal is available at pin 7. For these particular component values a maximum pulse width of 2 µs is available at pin 7.

The frequency is approximated by the relation:

\[ f(\text{Hz}) = \frac{(1.5) \sqrt{V_{\text{DD}}}}{(R1)(C1)} \]

The pulse width is approximated by the relation:

\[ T_{\text{width}} (\text{S}) = \left(4.5 \times 10^{-6}\right) \left(1 - \frac{R2}{500K}\right) \sqrt{V_{\text{DD}}} - 100 \text{ ns} \]

100V DC Stable High Switch

This application uses an EL7761 to drive the gate of an NMOS FET above the FET's source and drain voltage. This circuit would be useful in applications where the load must be energized continuously as in an automobile headlight circuit or a high side switch to a 48V bus in a distributed power application.

The low side driver self oscillates at a frequency determined by its input hysteresis in conjunction with R2 and C3. The output of the oscillator (pins 10 and 11) drive a charge pump which powers the high side drive section of the EL7761. A low voltage at the EN pin shuts the drive to the external FET off as well as shutting down the charge pump oscillator and putting the chip into a low supply current mode. Capacitors C1 and C4 are used to decouple the supplies. V_{\text{DD}} must be at least a diode drop higher than the desired enhancement of the external FET. The reverse breakdown of the zener diode should be less than 15V to avoid an overvoltage of the high side driver. Depending on the exact nature of the circuit a zener diode is not always necessary.
**Synchronous Buck Regulator Driver**

In this application one driver of the EL7981 is used to drive the main switch of a buck regulator while the other driver drives the synchronous switch. A transformer is used to obtain the high side switching voltage for M1. R1 sets the dead time delay between the on times of M1 and M2. The adjustable delay is perfect for devices with long turn off times such as IGBT's.

Set dead time with R1.
M1 and M2 can be IGBT's.

**Synchronous Buck Regulator**
Buck Regulator High Side Drive Using the EL7501

These circuits show two ways of using the EL7501 to drive the high side switch in a buck converter application. The first method uses resistors R1 and R2 to bias pin 1 in the middle of the drive voltage swing at pin 4. This allows the use of a single sided PWM drive. The high side voltage is pumped up from the V_DD supply.

The second method uses a complementary drive signal at pins 1 and 4 of the EL7501. It derives its high side supply voltage by charging capacitor C1 through resistor R1 and then using the external FET to pump that voltage above the high side supply.
Self Powered DC Stable 100V Half Bridge Driver

This circuit uses one driver of an EL7972 to provide low side drive and the other driver as a charge pump oscillator. The output of the charge pump oscillator drives a capacitor diode network to provide high side supply voltage to the EL7501. The EL7501 drives a high side external N-FET. Due to the addition of the charge pump this circuit will work at any driving frequency from DC to >1 MHz.

An EL7961C can be substituted if an enable feature is desired.

DC Functional Half Bridge Driver
IGBT Half Bridge Driver
This circuit shows the EL7981 being used to drive an IGBT half bridge. The high side IGBT is transformer coupled to the driver. The value of R1 is chosen so that the two IGBT's never conduct at the same time. If the IGBT's have different turn off characteristics then the EL7982 could be used instead of the EL7981. The EL7982 has independent control of each of its driver's rising edge delay.

IGBT Half Bridge Driver
Self Oscillating IGBT Driver
This circuit self oscillates at approximately 25 KHz. The on times of each driver depend on the values of R1, C1, R2 and C2. In order to ensure equal on times accurate component values may need to be used. The resistor, R3, controls the dead time between the on times of both drivers.

Diodes - 1N4148
R3 sets dead time
Approximately 25 KHz oscillation

Self Oscillating IGBT Driver, DC-DC Step Up (or Down)
40 Watt-12V Step Down Regulator Using a Synchronous Switch

This circuit shows how the EL7761 could be used as a half bridge driver for a step down converter. The circuit switches at 250 KHz.
Simple Undervoltage Lockout Circuit

By using a zener diode and a pull down resistor the user can implement a simple UVLO circuit. As $V_{DD}$ increases above the zener voltage the EN pin rises above ground. When EN reaches $V_{ton}$ the chip is enabled. As $V_{DD}$ is lowered such that the voltage at EN falls below $V_{toff}$, the chip is disabled. The threshold tolerances are as follows:

$1.0V < V_{ton} < 1.6V$

$0.3V < V_{ton} - V_{toff} < 1.0V$

$V_{turn-on} = V_Z + V_{ton}$

$V_{turn-off} = V_Z + V_{toff}$

![Simple UVLO Circuit for the EL7761](image1)

![Simple UVLO Circuit for the EL79X1](image2)
**Video Sync Pulse Generator**

The EL7501 inputs function outside the power supply rails, allowing a ground referenced TTL signal to control a ground to $-8V$ output swing. The output resistors can be adjusted to tailor the rise and fall times of the circuit.
Synchronous Switch Increases Boost Efficiency
The EL7501 plus a N-FET replaces the catch diode in a boost regulator. When the R+ pin is higher than the R− pin, the FET is turned on, effectively shorting out the parasitic diode of the FET. A small resistor may be added in series with the R− pin in order to "tune" the turn-on delay of the FET.
Resonant Gate Driver

Resonant gate driver can be used to boost the gate voltage swing while increasing driver efficiency. In Figure 1, an EL7501 is configured with (2) external "ring" diodes and resonating inductor L_R. For tutorial purposes, the power mosfet load was replaced by a 1000 pF capacitor (C_L). The "ring" diodes are fast switching diodes capable of withstanding the 1 amp peak current, such as the 1N914. Standard de-coupling techniques are applied with 5V applied to V_DD, the circuit delivers +10V to -5V output. In "5V only" systems, sufficient output swing is available so as to eliminate the need for costly "logic level" power FETs, and provides below ground swing for superior turn-off.

Principle of Operation

When the input drops below 2.4V, pin 7 pulls high, allowing current to flow from V_DD thru D1 and L_R, thus charging C_L. Initially the full voltage appears across the inductor, but as the current starts to flow, C_L begins to charge. When C_L reaches the supply voltage, current continues to flow as the inductor L_R reverses direction and continues to charge the capacitor beyond the supply voltage. When C_L reaches its peak, the "ring" diode disconnects, holding that potential across C_L. The peak voltage can be controlled by adjusting the circuit "Q". Typically this is accomplished by varying the size of inductor L_R, since the "on" resistance of the driver can limit the circuit "Q". This is governed by the expression:

\[ Q = \frac{\omega L}{R} \]

where:

\[ \omega = \frac{1}{\sqrt{LC}} \text{ or } Q = \frac{1}{R} \sqrt{\frac{L}{C}} \]

Thus, higher "Q", and higher voltage swing can be maintained by making \( \sqrt{L/C} \) large compared to R. (R ≈ 5Ω typ. for the EL7501.)

Similarly, when pin-6 pulls low, the output resonates below ground to provide good turn-off. Since charge is transferred mostly thru the inductor, rather than a resistor efficiency is much higher. The circuit performance is summarized below.

<table>
<thead>
<tr>
<th>Conditions: V_DD = 5V, F_C = 220 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L) Inductance</td>
</tr>
<tr>
<td>Case 1</td>
</tr>
<tr>
<td>Case 2</td>
</tr>
</tbody>
</table>

The power consumption was measured for Case 2, at 40 mW. Using "resistive" charging a power dissipation/consumption of 200 mW is anticipated, thus resulting in a (5) fold improvement in efficiency.

Figure 1. Resonant Gate Driver
MOS Driver with Under-Voltage Lock-Out

\[ UV \approx (1.5) \frac{R_1 + R_2}{R_1} \]

Over-Current Protected Driver

\[ I_p \approx \frac{0.6}{R_{\text{SENSE}}} \]

Recovery Time \( T_R \sim RC \)
MOS Driver with Simultaneous Conduction Lock-Out

![Diagram](image)

Truth Table

<table>
<thead>
<tr>
<th>$A_1$</th>
<th>$B_1$</th>
<th>$A_0$</th>
<th>$B_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
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</tr>
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<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1/0</td>
<td>0/1</td>
</tr>
</tbody>
</table>

MOS Driver with Over-Voltage Protection

![Diagram](image)

$0V \approx (1.5) \frac{R_1 + R_2}{R_1}$
Mosfet Driver Generates its own +12V supply

When you want to drive one power Mosfet, from a 5V or a 3.3V system, generating the one extra +12V supply can involve quite a large number of both active and passive components.

Here is a solution that uses the spare second Mosfet Driver channel to derive its own +12V supply. By using a driver with the drains brought out to separated pins, one can connect an inductor between the N-channel drain and the logic supply, without having the P-channel device connected.

In operation, it works as a standard flyback style switched mode circuit. When the output N-channel device is on, current starts flowing in the inductor, storing energy. When the N-channel device is turned off, the current has to continue flowing, so it flows through the diode D2 to charge up capacitors C1 and C2. As the cycle repeats, the voltage on C1 and C2 rises until the zener diode prevents further voltage rise. This is needed to prevent the drivers' derived supply from exceeding the parts' maximum voltage rating.

Since the objective was to minimize the number of external components and cost, additional components which would allow the circuit to self oscillate and regulate were omitted. The logic system was able to supply a drive pulse waveform to the supply generator. With the 5V system, I was using a 1.5 µs pulse every 9 µs. This gave a very solid +12.4V, and the system supply current went up by about 11 mA. The 3.3V system used a 300 kHz square wave, for a similar 12V derived supply, but with nearly 40 mA extra supply current. In both systems, when the Mosfet Driver was not being used, it could be "powered down" by simply stopping the pulses to the switching channel.

Any dual Mosfet Driver can be used, but if the drains of the output stage are not separated, there may be some protection and other parasitic devices that may prevent satisfactory operation. In these cases an external fet can be used to drive the inductor, provided a low threshold device is used. By altering the inductor value and the controlling pulses, enough power can be derived for further Mosfet Drivers or other peripheral devices requiring +12V.

Self Charge Pumping Mosfet Driver
Super Inverters

CMOS is often equated with low power, however dynamic losses can be significant, particularly as the frequency of operation increases. Losses can be attributed to the parasitic capacitance on all internal nodes which toggle (described by $P = CV^2f$), and from simultaneous conduction through CMOS gates during switching. Parasitic capacitance is reduced by shrinking feature sizes and using low overlap, self aligned silicon-gate process technology. Simultaneous conduction (shoot-thru) can be controlled or eliminated completely with "super-inverter" technology. A standard CMOS inverter is shown in Figure 2A. Here, with every transition, there is an interval during which both the NMOS and PMOS transistors are conducting and dissipating energy. Thus the integral of the instantaneous shoot-thru current, multiplied by the supply voltage and clock frequency describes the power loss.

$$P = 2fV \int_0^t I_S(t)dt$$

These losses can be significant, and are illustrated in Figure 2B. The super-inverter shown in Figure 3A overcomes the "shoot-thru" problem with "break before make" asymmetric drive, thereby controlling or eliminating simultaneous conduction. The designer can trade-off shoot-thru current for added propagation delay. The results demonstrated in Figure 3B represent about a $4 \times$ improvement. An added benefit is the reduced power supply bounce resulting from di/dt and stray inductance.

![Figure 2A. Standard CMOS Inverter](image1)

![Figure 2B. CMOS Inverter Switching Losses](image2)
Super Inverters — Contd.

![Super Inverter Circuit](image)

**Figure 3A. Super Inverter**

![Super Inverter Switching Losses Chart](image)

**Figure 3B. Super Inverter Switching Losses**

**Input Source Follower**

To accommodate moderately high source impedances, a source follower input stage similar to the circuit shown in Figure 4 is used. This eliminates both the "Miller" gate capacitance, and gate to source capacitance seen in typical designs. The "boot-strapping" effect eliminates all but the gate-drain capacitance. This feature allows direct drive from low current logic, without any degradation in performance.

![Input Source Follower Circuit](image)

**Figure 4. Low Input Capacitance Source Follower**
Precision Level Shifting
Generating rail to rail drive from a logic level input is accomplished with a Class AB push-pull amplifier and an internal 1.2V reference. This produces a well controlled threshold with minimal propagation delay. The known switch point can be used to generate under-voltage lock-out protection. Hysteresis is also introduced to boost the noise immunity.

3-State and Gated Inputs
Additional logic functions are also provided to insure greater flexibility. 3-State control is often useful in "Bridge" and "Bus" applications. Gated inputs can be used for chip enable/shut-down, latching, and various other functions.

Overall Performance
The resulting CMOS Drivers offer both functionality and performance. Figure 5 shows the switching characteristics into a 1000 pF load. Rise time, fall time, and delay are all matched to minimize pulse distortion, and are less than 20 ns. Figure 6 illustrates the waveform integrity at 5 MHz, into 1000 pF.

![Waveform Integrity](image1)

Ch. 1 = 2.000V/div
Ch. 2 = 4.000V/div
Timebase = 100 ns/div

Figure 6. 5 MHz Output into 1000 pF Load

![Step Response](image2)

Ch. 1 = 1.000V/div
Ch. 2 = 5.000V/div
Timebase = 20.0 ns/div

Figure 5. Step Response into 1000 pF Load
Application Specific Data Processing Products

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
## Laser Diode Driver

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Tr Typ</th>
<th>I\textsubscript{OUT} Max (Both Channels)</th>
<th>R\textsubscript{OUT} Typ (Both Channels)</th>
<th>Supply</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL6251C</td>
<td>2-Channel + Sense</td>
<td>2 ns</td>
<td>320 mA</td>
<td>7.5Ω</td>
<td>5V ±10%</td>
<td>24P-M †</td>
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</table>

## DC:DC Converters

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>I\textsubscript{peak}</th>
<th>V\textsubscript{OUT}</th>
<th>Accuracy</th>
<th>V\textsubscript{SUPPLY}</th>
<th>Package</th>
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<tbody>
<tr>
<td>EL7556C</td>
<td>Int Ref</td>
<td>6A</td>
<td>Variable</td>
<td>1%</td>
<td>6V</td>
<td>28P-M †</td>
</tr>
<tr>
<td>EL7560C</td>
<td>Ext Ref</td>
<td>12.4A</td>
<td>2.1V–3.5V</td>
<td>1%</td>
<td>6V</td>
<td>28P-M †</td>
</tr>
<tr>
<td>EL7561C</td>
<td>Int Ref</td>
<td>12.4A</td>
<td>2.1V–3.5V</td>
<td>1%</td>
<td>6V</td>
<td>28P-M †</td>
</tr>
<tr>
<td>EL7571C</td>
<td>Int Ref</td>
<td>12.4A</td>
<td>1.3V–3.5V</td>
<td>1%</td>
<td>4.5V–13.2V</td>
<td>20P-M †</td>
</tr>
</tbody>
</table>

† See Ordering Information section in this databook.
Features
• High-performance laser diode driver and power monitor
• Voltage-controlled read and write currents up to 320 mA total (160 mA read/160 mA write)
• 1.7 ns rise time
• 3.2 ns fall time
• Single +5V supply
• Power supply fault sensing for laser diode protection
• Laser diode power sense amplifier with two transimpedance levels compatible with read and write modes
• Uses external set resistors for both read and write transconductance

Applications
• Writeable optical drives

Ordering Information
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL6251CM</td>
<td>-40°C to +85°C</td>
<td>24 Pin SOL</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

General Description
The EL6251C is a Laser Power Amplifier which provides pulsed write/erase current as well as DC or pulsed read current to a common-cathode laser diode connected to output pins WROUT and RDOUT respectively. Separate pins are provided so that the read output may be inductively isolated from the write output and the laser diode. The levels of these currents are individually set by analog input voltages applied to the WRPWR and RDPWR pins respectively. Write output current pulses are achieved by a TTL "L" signal at the WROUTEN pin. Similarly, Read output pulses are achieved (if a simple DC level is not desired) by a TTL "L" signal at the RDOUTEN pin. Power-down of both the RDOUT and WROUT pins is also accomplished by applying a TTL "L" signal to the LSRMOD pin. Protection at low power supplies is also provided, with the RDOUT and WROUT outputs turning off when the supply voltage falls below about 4V. Laser Diode Protection is additionally provided since, when open, the LSRMOD floats low, and RDOUTEN and WROUTEN float high, thereby disabling any output current.

The EL6251C also contains all the necessary sense circuitry to produce an output voltage at the LSV pin proportional to the input current at the LSI pin, which is from a laser power-monitor photodiode. Two values of sense circuitry are available, selected by a TTL input on the WRSENS pin (floats high when open).

Three external resistors at pins RSENSE, RRDOUT, and RWROUT are used to accurately set the transimpedance of the sense amplifier, and the read and write transconductance. The output current at RDOUT and WROUT varies inversely with resistor value, while the transimpedance of the sense amplifier varies directly with the value of RSENSE.

Connection Diagram

![Connection Diagram](image-url)
### Absolute Maximum Ratings \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Voltage Applied to:</th>
<th>Power Dissipation (maximum)</th>
<th>See Curves</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}, V_{CCRD}, V_{CCWR})</td>
<td>(-0.5V) to (6.0V)</td>
<td>-</td>
</tr>
<tr>
<td>TTL Inputs</td>
<td>(-0.5V) to (V_{CC} + 0.5V)</td>
<td>-</td>
</tr>
<tr>
<td>(WRPWR) and (RDPWR)</td>
<td>(-0.5V) to (V_{CC} + 0.5V)</td>
<td>-</td>
</tr>
<tr>
<td>LSI</td>
<td>(-0.5V) to (2.5V)</td>
<td>-</td>
</tr>
<tr>
<td>(WROUT) and (RDOUT)</td>
<td>(-0.5V) to (V_{CC} + 0.5V)</td>
<td>-</td>
</tr>
<tr>
<td>LSV</td>
<td>(-0.5V) to (V_{CC} + 0.5V)</td>
<td>-</td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

### Electrical Characteristics

- \(V_{CC} = 5V\), \(RRDOUT = 10\ k\Omega\), \(RWROUT = 6.2\ k\Omega\), \(RDOUT\) and \(WROUT\) load = \(10\Omega\) to GND, \(RSENSE = 10\ k\Omega\), \(T_A = 25^\circ C\) unless otherwise specified.

### General

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CCF})</td>
<td>(V_{CC}) Fault Voltage</td>
<td>(Note 1)</td>
<td>3.3</td>
<td>3.8</td>
<td>4.1</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_S1)</td>
<td>Supply Current</td>
<td>(WRPWR = RDPWR = 2.88V, LSRMODE = H)</td>
<td>237</td>
<td>270</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>(I_S2)</td>
<td>Supply Current</td>
<td>(WRPWR = RDPWR = 0V, LSRMODE = H or L)</td>
<td>35</td>
<td>46</td>
<td>58</td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

### Logic Control Signals \((LSRMODE, WRSENS, RDOUTEN, WROUTEN)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IL})</td>
<td>Input Low Voltage</td>
<td></td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input High Voltage</td>
<td>(V_{IN} = 0V)</td>
<td>0.8</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IL})</td>
<td>Input Low Current</td>
<td></td>
<td>(-250)</td>
<td></td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{IH1})</td>
<td>Input High Current 1</td>
<td>(V_{IN} = 2.00V) ((\text{all inputs}))</td>
<td>0</td>
<td>0</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{IH2})</td>
<td>Input High Current 2</td>
<td>(V_{IN} = 5.00V) ((\text{excluding LSRMOD}))</td>
<td>0</td>
<td>10</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{IH3})</td>
<td>Input High Current 3</td>
<td>(V_{IN} = 5.00V) ((\text{LSRMODE only}))</td>
<td>400</td>
<td>500</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
</tbody>
</table>

**Note 1:** When \(V_{CC} < V_{CCF}\), \(WROUT\) and \(RDOUT\) are disabled while the Laser Sense Amplifier circuitry remains active.

### V To I Stages

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OFFSET})</td>
<td>(V) to (I) Offset Voltage</td>
<td>(RDPWR - RRDOUT, WRPWR - WROUT, RDPWR = WRPWR = 2.88V)</td>
<td>-11</td>
<td>-1</td>
<td>10</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(G_{S1})</td>
<td>Gain Scale 1</td>
<td>(RRDOUT = 3.6 k\Omega) (Note 2)</td>
<td>97</td>
<td>100</td>
<td>103</td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>(G_{S2})</td>
<td>Gain Scale 2</td>
<td>(RWROUT = 3.6 k\Omega) (Note 3)</td>
<td>97</td>
<td>100</td>
<td>103</td>
<td>I</td>
<td>%</td>
</tr>
</tbody>
</table>

6-4
**Electrical Characteristics — Contd.**

VCC = 5V, RRDOUT = 10 kΩ, RWROUT = 6.2 kΩ, RDDSOUT and WDOUT load = 10Ω to GND, RSENSE = 10 kΩ, TA = 25°C unless otherwise specified

### Laser Sense Amplifier Input (LSI Pin)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VLSI</td>
<td>Voltage at LSI Pin</td>
<td>WRSENS = 0.8V, ILSI = 100 μA (Note 4)</td>
<td>1.4</td>
<td>1.5</td>
<td>1.6</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>ILSI1</td>
<td>Input Current Range 1</td>
<td>WRSENS = 2.0V</td>
<td>0</td>
<td>1600</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>ILSI2</td>
<td>Input Current Range 2</td>
<td>WRSENS = 0.8V</td>
<td>0</td>
<td>200</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>CLSI</td>
<td>Input Capacitance</td>
<td></td>
<td>2</td>
<td>V</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

### Laser Sense Amplifier

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VMAX</td>
<td>Max. Output Voltage</td>
<td>RLOAD = 2 kΩ to GND, LSI = 1.6 mA, WRSENS = 2V</td>
<td>3.70</td>
<td>3.86</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>VMIN</td>
<td>Min. Output Voltage</td>
<td>RLOAD = 2 kΩ to GND, LSI = 1 μA, WRSENS = 2V</td>
<td>25</td>
<td>75</td>
<td>110</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>TCVMIN</td>
<td>Min. Output V Drift</td>
<td>RLOAD = 2 kΩ to GND, TMIN to TMAX</td>
<td>-300</td>
<td>300</td>
<td></td>
<td>IV</td>
<td>μV/°C</td>
</tr>
<tr>
<td>VLIN</td>
<td>Output Linearity</td>
<td>Best Fit Method, Measured at LSI = 10%, 50%, 90% of ILSI1, ILSI2.</td>
<td>-2</td>
<td>0.1</td>
<td>+2</td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>ZOUT</td>
<td>Output Impedance</td>
<td>ILOAD = ±1 mA</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>Ω</td>
</tr>
<tr>
<td>IOUT</td>
<td>Current Drive</td>
<td>VOUT from VMIN to VMAX</td>
<td>-1</td>
<td></td>
<td>+2</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>UOUT</td>
<td>Output Noise Voltage</td>
<td>BW = 3.5 MHz</td>
<td>0.7</td>
<td></td>
<td></td>
<td>V</td>
<td>mV RMS</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>RLOAD = 2 kΩ to GND</td>
<td>10</td>
<td>15</td>
<td></td>
<td>IV</td>
<td>V/μs</td>
</tr>
<tr>
<td>RM1</td>
<td>Transimpedance 1</td>
<td>WRSENS = 2.0V, Note 5, Note 6</td>
<td>2.393</td>
<td>2.467</td>
<td>2.541</td>
<td>I</td>
<td>kΩ</td>
</tr>
<tr>
<td>VO01</td>
<td>Output Offset Voltage 1</td>
<td>WRSENS = 2.0V, Note 5</td>
<td>-100</td>
<td>-54</td>
<td>10</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>RM2</td>
<td>Transimpedance 2</td>
<td>WRSENS = 0.8V, Note 5, Note 6</td>
<td>18.93</td>
<td>19.32</td>
<td>20.11</td>
<td>I</td>
<td>kΩ</td>
</tr>
<tr>
<td>VO02</td>
<td>Output Offset Voltage 2</td>
<td>WRSENS = 0.8V, Note 5</td>
<td>-25</td>
<td>+3</td>
<td>+25</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>TCRM</td>
<td>Transimpedance Drift</td>
<td></td>
<td>0</td>
<td>65</td>
<td>150</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>−3 dB Bandwidth</td>
<td>3</td>
<td>8</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
<tr>
<td>PKNG</td>
<td>Peaking</td>
<td></td>
<td>0</td>
<td>3</td>
<td></td>
<td>V</td>
<td>dB</td>
</tr>
<tr>
<td>TRECVR</td>
<td>Recovery Time</td>
<td>WRSENS L to H or H to L, Output Settling to ±20 mV, LSI = 100 μA</td>
<td>100</td>
<td>300</td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 2:** Output current (IOUTGS1) is measured with RRDOUT = 3.6 kΩ, RDPWR = 1.200V. This value is compared to the output current (IOUTNOM) with RRDOUT = 10 kΩ, RDPWR = 3.333V. GS1 = (IOUTNOM/IOUTGS1)

**Note 3:** Output current (IOUTGS2) is measured with RWROUT = 3.6 kΩ, WRPWR = 1.200V. This value is compared to the output current (IOUTNOM) with RWROUT = 6.2 kΩ, WRPWR = 2.067V. GS2 = (IOUTNOM/IOUTGS2)

**Note 4:** VLSI = (2 * Vbe) + (ILSI * 200 kΩ).

**Note 5:** The transfer function for the Laser Sense Amplifier is as follows:

\[
WRSENS = 2.0 \text{V:} \quad V_{LSI} = (I_{LSI} \times R_{M1}) + V_{O01}
\]
\[
WRSENS = 0.8 \text{V:} \quad V_{LSI} = (I_{LSI} \times R_{M2}) + V_{O02}
\]

**Note 6:**

\[
R_{M1} \approx 0.247 \times \text{RSENSE}
\]
\[
R_{M2} \approx 1.952 \times \text{RSENSE}
\]
Electrical Characteristics — Contd.

\( V_{CC} = 5V, \text{ RRDOUT} = 10 \, \text{k} \Omega, \text{ RWROUT} = 6.2 \, \text{k} \Omega, \text{ RDOUt and WRROUT load} = 10\Omega \text{ to GND}, \text{ RSENSE} = 10 \, \text{k} \Omega, T_A = 25^\circ \text{C} \)

unless otherwise specified

**Laser Current Amplifier Inputs (RDPWR and WRPWR Pins)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{IN} )</td>
<td>Input Resistance</td>
<td>RDPWR and WRPWR. Meas. at 0.576V, 2.88V</td>
<td>18</td>
<td>24</td>
<td></td>
<td>I</td>
<td>k\Omega</td>
</tr>
<tr>
<td>( I_{IB} )</td>
<td>Input Bias Current</td>
<td>( V_{IN} = 2.88V )</td>
<td>115</td>
<td>200</td>
<td></td>
<td>I</td>
<td>\mu A</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
<tr>
<td><strong>BW</strong></td>
<td>-3 dB Bandwidth</td>
<td>( V_{IN} = 2.88V )</td>
<td>40</td>
<td>70</td>
<td></td>
<td>V</td>
<td>MHz</td>
</tr>
</tbody>
</table>

**Laser Current Amplifier Outputs DC Performance (RDOUt and WRROUT pins)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{RDOUT1} )</td>
<td>RDOUT Output I 1</td>
<td>RDPWR = 2.88V</td>
<td>-61</td>
<td>-67</td>
<td>-74</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{RDOUT2} )</td>
<td>RDOUT Output I 2</td>
<td>RDPWR = 0.576V</td>
<td>-13</td>
<td>-16</td>
<td>-19</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{WROUT1} )</td>
<td>WROUT Output I 1</td>
<td>WRPWR = 2.88V</td>
<td>-89</td>
<td>-98</td>
<td>-107</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{WROUT2} )</td>
<td>WROUT Output I 2</td>
<td>WRPWR = 0.576V</td>
<td>-17</td>
<td>-21</td>
<td>-25</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( G_{MRD} )</td>
<td>RD Transconductance</td>
<td>( R_{load} = 10\Omega \text{ Note 7, Note 8, Note 9} )</td>
<td>0.0208</td>
<td>0.0224</td>
<td>0.0240</td>
<td>I</td>
<td>1/\Omega</td>
</tr>
<tr>
<td>( RDGAiN )</td>
<td>Read Current Gain</td>
<td>( RDGAiN = GMRD \times RRSROUT )</td>
<td>208</td>
<td>224</td>
<td>240</td>
<td>I</td>
<td>mA/mA</td>
</tr>
<tr>
<td>( IO_{OR} )</td>
<td>RD Out. Offset Current</td>
<td>Note 7</td>
<td>-7</td>
<td>-3.4</td>
<td>0</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( GM_{WR} )</td>
<td>WR Transconductance</td>
<td>( R_{load} = 10\Omega \text{ Note 7, Note 8, Note 9} )</td>
<td>0.0310</td>
<td>0.0334</td>
<td>0.0358</td>
<td>I</td>
<td>1/\Omega</td>
</tr>
<tr>
<td>( WRGAiN )</td>
<td>Write Current Gain</td>
<td>( WRGAiN = GMWR \times RWROUT )</td>
<td>192</td>
<td>207</td>
<td>222</td>
<td>I</td>
<td>mA/mA</td>
</tr>
<tr>
<td>( IO_{OR} )</td>
<td>WR Out. Offset Current</td>
<td>Note 7</td>
<td>-6</td>
<td>-2.0</td>
<td>+1</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( TCIout1 )</td>
<td>Output Current Drift</td>
<td>RDOUT and WROUT, Iout = 32 mA</td>
<td>100</td>
<td>500</td>
<td>800</td>
<td>IV</td>
<td>ppm/°C</td>
</tr>
<tr>
<td>( TCIout2 )</td>
<td>Output Current Drift</td>
<td>RDOUT and WROUT, Iout = 160 mA</td>
<td>200</td>
<td>900</td>
<td>1250</td>
<td>IV</td>
<td>ppm/°C</td>
</tr>
<tr>
<td>( IL_{IN} )</td>
<td>Output Curr. Linearity</td>
<td>RDPWR = WRPWR = 0.576V to 2.88V, Best Fit Method. Note 7.</td>
<td>-3</td>
<td>3</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>( IO_{OFF1} )</td>
<td>Output Off Current 1</td>
<td>WRPWR and RDPWR open.</td>
<td>-1.5</td>
<td>-0.6</td>
<td>0</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( IO_{OFF2} )</td>
<td>Output Off Current 2</td>
<td>WRPWR = RDPWR = 2.88V, WRROUTEN = RDOUTEN = 2V.</td>
<td>-1.5</td>
<td>-0.4</td>
<td>0</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>Output Impedance</td>
<td>Iout = 50 mA</td>
<td></td>
<td>750</td>
<td></td>
<td>V</td>
<td>\Omega</td>
</tr>
<tr>
<td>( C_{OUT} )</td>
<td>Output Capacitance</td>
<td>Iout = 50 mA</td>
<td>40</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
</tbody>
</table>

Note 7: The transfer function for each Laser Current Amplifier is calculated using a best-fit method at 3 points. The input voltages applied to WRPWR and RDPWR for the 3 points are 0.576V, 1.728V, and 2.88V. The transfer functions for \( I_{RDOUT} \) and \( I_{WRROUT} \) are defined as follows:

\[ I_{RDOUT} = (V_{RPWR} \times G_{MRD}) + IO_{OR} \]
\[ I_{WRROUT} = (V_{WRPWR} \times G_{MW}) + IO_{WR} \]

Note 8: \( G_{MRD} \approx 224/RRDOUT \text{ (Nominally)} \)
\( GM_{WR} \approx 207/RWROUT \text{ (Nominally)} \)

Note 9: Datasheet values are based on tester data which implies part is not warmed up, so \( T_j \) is similar to \( T_a \).

For precise values, see curves or use the temperature coefficient data.
Laser Current Amplifier Outputs AC Performance
(RDOUT and WROUT pins) \( V_{CC} = +5V \), \( RWROUT=RRDOUT=3.6 \, k\Omega \), \( RSENSE=10 \, k\Omega \), \( T_A=25°C \) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_r )</td>
<td>Output Curr. Rise Time</td>
<td>( WRPWR = RDPWR = 2.88V ) (10%-90%)</td>
<td>1.0</td>
<td>1.7</td>
<td>3.0</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Output Curr. Fall Time</td>
<td>( WRPWR = RDPWR = 2.88V ) (10%-90%)</td>
<td>2.2</td>
<td>3.2</td>
<td>4.2</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>OS</td>
<td>Output Curr. Overshoot</td>
<td>( WRPWR = RDPWR = 2.88V )</td>
<td>8</td>
<td>20</td>
<td></td>
<td>IV</td>
<td>%</td>
</tr>
<tr>
<td>( t_{PD2A} )</td>
<td>WROUTEN L-H Prop. Delay A</td>
<td>From WROUTEN 50% L-H to WROUT at 50% of Initial Value. ( I(WROUT) = 150mA )</td>
<td>2.9</td>
<td>6.0</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PD2B} )</td>
<td>WROUTEN L-H Prop. Delay B</td>
<td>From WROUTEN 50% L-H to WROUT at 50% of Initial Value. ( I(WROUT) = 30mA )</td>
<td>3.6</td>
<td>7.0</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PD3A} )</td>
<td>WROUTEN H-L Prop. Delay A</td>
<td>From WROUTEN 50% H-L to WROUT at 50% of Final Value. ( I(WROUT) = 150mA )</td>
<td>3.2</td>
<td>6.0</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PD3B} )</td>
<td>WROUTEN H-L Prop. Delay B</td>
<td>From WROUTEN 50% H-L to WROUT at 50% of Final Value. ( I(WROUT) = 30mA )</td>
<td>3.3</td>
<td>7.0</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

Pin Descriptions

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin Number</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>5–8, 17–20</td>
<td>Power Supply</td>
<td>Ground</td>
</tr>
<tr>
<td>LSRMOD</td>
<td>13</td>
<td>TTL Input</td>
<td>RDOUT and WROUT Output Current Enable. Outputs enabled when &quot;H&quot;.</td>
</tr>
<tr>
<td>VCCRD</td>
<td>3</td>
<td>Power Supply</td>
<td>+5V</td>
</tr>
<tr>
<td>VCCWR</td>
<td>22</td>
<td>Power Supply</td>
<td>+5V</td>
</tr>
<tr>
<td>VCC</td>
<td>24</td>
<td>Power Supply</td>
<td>+5V</td>
</tr>
<tr>
<td>LSV</td>
<td>2</td>
<td>Analog Output</td>
<td>Laser Sense Voltage. See Notes 5,6 for formula.</td>
</tr>
<tr>
<td>LSI</td>
<td>1</td>
<td>Analog Input</td>
<td>Laser Sense Current</td>
</tr>
<tr>
<td>WRSENS</td>
<td>12</td>
<td>TTL Input</td>
<td>I-to-V Sensitivity Selection. 0.25 * RSENSE when &quot;H&quot;, 2 * RSENSE when &quot;L&quot;</td>
</tr>
<tr>
<td>RSENSE</td>
<td>11</td>
<td>R Connection</td>
<td>Sense Amplifier Gain Control Resistor. Nominally 10 k\Omega to ground.</td>
</tr>
<tr>
<td>RDPWR</td>
<td>10</td>
<td>Analog Input</td>
<td>Voltage Input to Control RDOUT Current</td>
</tr>
<tr>
<td>RDOUT</td>
<td>4</td>
<td>Analog Output</td>
<td>Read Output Current. See Notes 7, 8 for formula.</td>
</tr>
<tr>
<td>RDOUTEN</td>
<td>23</td>
<td>TTL Input</td>
<td>RDOUT Enable. RDOUT is enabled when &quot;L&quot; and LSRMOD is &quot;H&quot;.</td>
</tr>
<tr>
<td>RRDOUT</td>
<td>9</td>
<td>R Connection</td>
<td>Read transconductance resistor. Nominally 3.6 k\Omega to ground.</td>
</tr>
</tbody>
</table>

Laser Driver (Write Channel)

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin Number</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRPWR</td>
<td>15</td>
<td>Analog Input</td>
<td>Voltage Input to Control WROUT Current</td>
</tr>
<tr>
<td>WROUT</td>
<td>21</td>
<td>Analog Output</td>
<td>Write Output Current. See Notes 7, 8 for formula.</td>
</tr>
<tr>
<td>WROUTEN</td>
<td>14</td>
<td>TTL Input</td>
<td>WROUT Enable. WROUT is enabled when &quot;L&quot; and LSRMOD is &quot;H&quot;.</td>
</tr>
<tr>
<td>RWROUT</td>
<td>16</td>
<td>R Connection</td>
<td>Write transconductance resistor. Nominally 3.6 k\Omega to ground.</td>
</tr>
</tbody>
</table>
Control Truth Table

<table>
<thead>
<tr>
<th>LSRMOD</th>
<th>WROUTEN</th>
<th>RDOUTEN</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Ir=ON, lw=ON</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Ir=OFF, lw=ON</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Ir=ON, lw=OFF</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>lw=lr=0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>lw=lr=0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>lw=lr=0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>lw=lr=0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>lw=lr=0</td>
</tr>
</tbody>
</table>

Typical Performance Curves

Read Current Gain vs Temperature (VRPWR = 2.88V, RRDOUT = 3.6 kΩ)

Write Current Gain vs Temperature (WWRPWR = 2.88V, RWROUT = 3.6 kΩ)

IS2 vs Temperature

VLSI vs Die Temperature (VLSI through 20 kΩ to 5.0V)

Turn-On Delay vs IOUT

Turn-Off Delay vs IOUT
Typical Performance Curves — Contd.

24-Pin Plastic Fuselead Maximum Power Dissipation vs Ambient Temperature

EL6251 Block Diagram

EL6251 Block Diagram

24-Pin Plastic Fuselead Maximum Power Dissipation vs Ambient Temperature

EL6251 Block Diagram

EL6251 Block Diagram

EL6251 Block Diagram

EL6251 Block Diagram
**Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Supply Voltage</td>
<td>5.0V ± 10%</td>
</tr>
<tr>
<td>RRDOUT Resistor</td>
<td>1.8 kΩ to 10 kΩ</td>
</tr>
<tr>
<td>RWROUT Resistor</td>
<td>1.8 kΩ to 10 kΩ</td>
</tr>
<tr>
<td>RSENSE Resistor</td>
<td>5.0 kΩ to 20.0 kΩ</td>
</tr>
<tr>
<td>Write Current</td>
<td>0 to 160 mA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read Current</td>
<td>0 to 160 mA</td>
</tr>
<tr>
<td>WROUT Applied Voltage</td>
<td>0V to VCC – 0.3 – (15*Iwrite)</td>
</tr>
<tr>
<td>RDOUT Applied Voltage</td>
<td>0V to VCC – 0.3 – (15*Iread)</td>
</tr>
<tr>
<td>RDPWR and WRPWR Input Range</td>
<td>0V to VCC – 1.5V</td>
</tr>
</tbody>
</table>

**Typical Circuit Configuration**

![Circuit Diagram](image)
Application Notes:

Due to the high values of current being switched rapidly on and off, it is important to ensure that the power supplies are well decoupled to ground. To this end, the EL6251C has three VCC pins, all of which should be connected, and users should ensure that supply inductance to these pins is minimized. Symptoms that could arise include poor rise/fall times, current ringing during switching, current overshoot, and poor settling response.

Oscillation can also occur due to capacitance on pins RR/DOUT and RW/ROUT. It is important to minimize any stray capacitance on these pins and use the suggested resistors to ground, otherwise current ringing when switching (or even sustained oscillation) may occur.

It is also important to minimize the lead inductance between the WROUT pin and the laser diode. If the read current is also to be switched, then the same caution applies as well. Too much inductance in series with WROUT will produce an underdamped ringing response on both the rising and falling edges of the current pulse. The ringing can sometimes be reduced with a parallel RC snubber right at the device output, but lack of headroom prevents the use of a series resistor on WROUT as an alternative.

Thermal Considerations:

The total device power consumption is highly dependent on the amount of current flowing through the laser diode, and may further be altered by any duty cycle effects. Despite this, the equation below is fairly accurate:

\[ P_D = ((I_{s2} + (1.1 \times I_{diode})) \times V_{CC}) - (I_{diode} \times V_{diode}) \]

where

- \(I_{s2}\) = Supply current when LSRMOD = 0 (46 mA typical)
- \(I_{diode}\) = Total current through the laser diode (Iread + Iwrite)
- \(V_{diode}\) = The voltage dropped across the laser diode
- \(V_{CC}\) = The EL6251C supply voltage

The die temperature will rise 40°C/W on a typical board where the EL6251C is soldered to a substantial groundplane, due to the 4 ground pins on either side of the device being attached to the mounting pad. Alternatively, the LSI pin acts as a good thermometer, by which the on-chip temperature may be monitored directly if so desired.
Features
- Precision internal 1% reference
- 3.3V @ 6 amps continuous
- Internal FETs
- > 90% Efficiency
- Synchronous switching
- User adjustable slope compensation
- Internal soft start
- Over temperature indicator
- Low current sleep mode
- Low parts count
- Pulse by pulse current limiting
- High efficiency at light load
- Operates up to 1 MHz
- 1% Output accuracy
- Sync function
- Power good signal
- Power-saver mode
- Intel P54 and P55 compatible
- VCC2DET Interface

Applications
- PC Motherboards
- Local high power CPU supplies
- 5V to 1.0V DC-DC conversion
- Portable electronics/instruments
- P54 and P55 regulators

Ordering Information
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7556CM</td>
<td>-40°C to +85°C</td>
<td>28-Pin SOIC</td>
<td>MDPO027</td>
</tr>
</tbody>
</table>

General Description
The EL7556C is the simplest, most cost effective method for powering modern high power CPUs which require a user adjustable output voltage. Although it is particularly designed to function with next generation CPUs, its simple design can provide low cost solutions for any 1.0V to 3.8V application from a 5V bus.

The circuit uses on chip resistorless current sensing for high efficiency, stable current mode control. An on chip temperature sensor resets the OT pin. The OT pin can be tied directly to the OUTEN pin for automatic overtemperature shutdown. The user can adjust the oscillator frequency as well as the slope compensation.

The EL7556C also incorporates the VCC2DET function to directly interface with the Intel P54 and P55 microprocessors. Depending on the state of VCC2DET pin, the output voltage is either set internally or adjustable using two external resistors. A power OK signal "PWRGD" pulls high when the regulator output is within ±10% of the desired voltages.

Connection Diagram
EL7556C
Adjustable CPU Power Supply Unit-6A

Absolute Maximum Ratings (TA = 25°C)
Storage Temperature Range -65°C to +150°C
Supply (VIN) 6V
Ambient Operating Temperature 0°C to +75°C
Output Pins
-0.3V below GND,
+0.3V above VDD

Operating Junction Temperature 125°C
Combined Peak Output Current 9A
Power Dissipation 2W

Storage Temperature Range -65°C to +150°C
Supply (VIN) 6V

Operating Junction Temperature 125°C
Combined Peak Output Current 9A
Power Dissipation 2W

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TJ = TC = TA.

Test Level Test Procedure
I 100% production tested and QA sample tested per QA test plan QCX0002.
II 100% production tested at TA = 25°C and QA sample tested at TA = 25°C.
III QA sample tested per QA test plan QCX0002.
IV Parameter is guaranteed (but not tested) by Design and Characterization Data.
V Parameter is typical value at TA = 25°C for information purposes only.

DC Electrical Characteristics TA = 25°C, VIN = 5V unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDX</td>
<td>Voltage Doubler Output</td>
<td>VDD = 5V, ILOAD = 20 mA</td>
<td>7.9</td>
<td>8.4</td>
<td>8.9</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>VREF</td>
<td>Reference Absolute Value</td>
<td>ILOAD = 0</td>
<td>1.150</td>
<td></td>
<td>1.250</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>VREFTC</td>
<td>Reference Voltage Tempo</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td>ppm</td>
</tr>
<tr>
<td>VREFLOAD</td>
<td>Reference Voltage Load Regulation</td>
<td>0 &lt; ILOAD &lt; 1 mA</td>
<td>-0.5%</td>
<td>0.5</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>FOsc</td>
<td>Oscillator Initial Accuracy</td>
<td>C0sc = 1000 pF</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>I</td>
<td>kHz</td>
</tr>
<tr>
<td>FOSCTC</td>
<td>Oscillator Tempco</td>
<td>0 &lt; TA &lt; 125°C</td>
<td>-0.1</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td>%/deg</td>
</tr>
<tr>
<td>FRAMP</td>
<td>Oscillator Ramp Amplitude</td>
<td>C0sc = 1000 pF</td>
<td>1.1</td>
<td>1.3</td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>MS</td>
<td>Soft Start Slope</td>
<td>F0sc = 500 kHz</td>
<td>0.1</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td>V/msec</td>
</tr>
<tr>
<td>VCC2DET</td>
<td>VCC2DET Pull Up Current</td>
<td></td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>LCSLOPE</td>
<td>CSLOPE Charging Current</td>
<td></td>
<td>10</td>
<td>14</td>
<td></td>
<td>I</td>
<td>µA</td>
</tr>
<tr>
<td>IDD</td>
<td>Supply Current</td>
<td>OUTEN = 4V</td>
<td>9</td>
<td>14</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>IDDOFF</td>
<td>Stdby Current</td>
<td>OUTEN = 0</td>
<td>9</td>
<td>15</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>NDS</td>
<td>Composite FET Resistance</td>
<td></td>
<td>15</td>
<td>25</td>
<td></td>
<td>I</td>
<td>mΩ</td>
</tr>
<tr>
<td>VOUT</td>
<td>Output Initial Accuracy</td>
<td>VCC2DET = High</td>
<td>3.465</td>
<td>3.5</td>
<td>3.535</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>ILMAX</td>
<td>Maximum Current</td>
<td>VOUT = 0</td>
<td>6.5</td>
<td>7.5</td>
<td></td>
<td>V</td>
<td>amps</td>
</tr>
<tr>
<td>VOUTTC</td>
<td>Output Tempo</td>
<td></td>
<td>-1</td>
<td>0</td>
<td>1</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>VOUTLINE</td>
<td>Output Line Regulation</td>
<td>Vout = 2.5</td>
<td>-1</td>
<td>1</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>VOUTLOAD</td>
<td>Output Load Regulation</td>
<td>4 &lt; VIN &lt; 5.5</td>
<td>-1</td>
<td>1</td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>VOUTTOT</td>
<td>Output Total Variation</td>
<td>1A &lt; ILOAD &lt; 6A</td>
<td>-2</td>
<td>2</td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
</tbody>
</table>
### EL7556C Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FB1</td>
<td>Voltage feedback pin for the buck regulator. Active when VCC2DET is low. Normally connected to a resistor divider externally.</td>
</tr>
<tr>
<td>2</td>
<td>CREF</td>
<td>Reference bypass pin. Use at least 0.1 μF bypass to ground.</td>
</tr>
<tr>
<td>3</td>
<td>CSLOPE</td>
<td>Slope compensation capacitor. A 10 μA current flows out of this pin. The voltage at this pin is reset to the reference voltage each clock period during the dead time.</td>
</tr>
<tr>
<td>4</td>
<td>COSC</td>
<td>Oscillator timing capacitor. The oscillator frequency is approximately: ( f_{OSC}(HZ) = \frac{0.0001}{C_{OSC}(F)} ). The duty cycle is approximately 4%.</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
<td>This pin supplies power to the internal control circuitry. It will draw some tens of milliamps when operating.</td>
</tr>
<tr>
<td>6</td>
<td>VIN</td>
<td>Positive power supply input to the buck regulator. This is one of two pins connected to the drain of a very large NMOS FET called the &quot;Main&quot; FET.</td>
</tr>
<tr>
<td>7</td>
<td>VSSP</td>
<td>Ground return to the buck regulator. This pin is connected to the source of a very large NMOS FET called the &quot;synchronous&quot; FET.</td>
</tr>
<tr>
<td>8</td>
<td>VIN</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>9</td>
<td>VSSP</td>
<td>Same as pin 7.</td>
</tr>
<tr>
<td>10</td>
<td>VSSP</td>
<td>Same as pin 7.</td>
</tr>
<tr>
<td>11</td>
<td>VSSP</td>
<td>Same as pin 7.</td>
</tr>
<tr>
<td>12</td>
<td>VSSP</td>
<td>Same as pin 7.</td>
</tr>
<tr>
<td>13</td>
<td>VCC2DET</td>
<td>VCC2DET interface. When High FB2 is selected. When low, FB1 is selected.</td>
</tr>
<tr>
<td>14</td>
<td>OUTEN</td>
<td>Enables the switching regulator. High is &quot;on&quot;. The reference, oscillator, and voltage doubler operate whenever the power supply qualified regardless of the state of this pin.</td>
</tr>
<tr>
<td>15</td>
<td>OT</td>
<td>Over temperature indicator. This pin is normally high. It pulls low when the die temperature exceeds 150°C. There is 10–20 degrees of hysteresis in the comparator.</td>
</tr>
<tr>
<td>16</td>
<td>PWRGD</td>
<td>This pin pulls high whenever the FB pin is within 7% of its programmed value.</td>
</tr>
<tr>
<td>17</td>
<td>TEST</td>
<td>Test pin. Must be connected to ground.</td>
</tr>
<tr>
<td>18</td>
<td>VSSP</td>
<td>Same as pin 7.</td>
</tr>
<tr>
<td>19</td>
<td>VSSP</td>
<td>Same as pin 7.</td>
</tr>
<tr>
<td>20</td>
<td>LX</td>
<td>This is the halfway point between the two large internal FETs. It drives the inductor of the buck regulator circuit. These are high current outputs.</td>
</tr>
<tr>
<td>21</td>
<td>LX</td>
<td>Same as pin 20.</td>
</tr>
</tbody>
</table>
EL7556C Pin Description — Contd.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>LX</td>
<td>Same as pin 20.</td>
</tr>
<tr>
<td>23</td>
<td>LX</td>
<td>Same as pin 20.</td>
</tr>
<tr>
<td>24</td>
<td>VHI</td>
<td>Positive supply for the high side driver. This pin is bootstrapped from LX pin with a 0.1 μF capacitor.</td>
</tr>
<tr>
<td>25</td>
<td>VSS</td>
<td>Ground return for the control circuitry.</td>
</tr>
<tr>
<td>26</td>
<td>C2V</td>
<td>Voltage doubler output. This pin requires at least a 1 μF capacitor to GND. The voltage on this pin will be 9V–10V depending on the load.</td>
</tr>
<tr>
<td>27</td>
<td>CP</td>
<td>Input for the charge pump bootstrap capacitor.</td>
</tr>
<tr>
<td>28</td>
<td>FB2</td>
<td>Voltage feedback pin. Active when VCC2DET is high. Normally connected to a resistor divider internally.</td>
</tr>
</tbody>
</table>

Applications Information

The EL7556 incorporates a VCC2DET function to directly interface with the Intel P54 and P55 microprocessors. When this pin is shorted to ground as in the P55 processor, the feedback path of EL7556 is internally switched to FB1. The regulator output is determined by the external resistor divider ratio, $V_{OUT} = 1.0 \times (1 + \frac{R3}{R4})$. When this pin is open as in the P54 processor, the feedback path of the EL7556 is switched to FB2. The regulator output is set internally to 3.5V nominal.
**Features**
- 3.3V @ 12.4 amps continuous
- Internal FETs
- > 90% efficiency
- Synchronous switching
- 4-bit digitally adjustable output voltage
- User adjustable slope compensation
- Internal soft start
- Over temperature indicator
- Low current sleep mode
- Low parts count
- Pulse by pulse current limiting
- High efficiency at light load
- Operates up to 1 MHz
- 1% output accuracy
- Sync function
- Power good signal

**Applications**
- PC motherboards
- Local high power CPU supplies

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7560CM</td>
<td>−40°C to +85°C</td>
<td>28-Pin SOIC</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

**General Description**

The EL7560C is the simplest, most cost effective method for powering modern high power CPUs which require a user adjustable output voltage. Although it is particularly designed to function with next generation CPUs, its simple design can provide low cost solutions for any 5V to 3V application.

The circuit uses on chip resistorless current sensing for high efficiency, stable current mode control. An on chip temperature sensor resets the OT pin. The OT pin can be tied directly to the OUTEN pin for automatic overtemperature shutdown. The user can adjust the oscillator frequency as well as the slope compensation.

The output voltage is adjustable using a 4-bit parallel interface. A power OK signal "PWRGD" pulls high when the FB pin is within −7% of the programmed value.

**Connection Diagram**

*See VID table on page 3
Note: AGND and PGND should be connected at C10
D3 is 1.235V reference
Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply ( (V_{IN}, V_{DD}) )</td>
<td>( V_{DD} = 5V, I_{LOAD} = 20 mA )</td>
<td>8.0</td>
<td>9</td>
<td>9.5</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Output Pins</td>
<td>(-0.3V ) below GND, (+0.3V ) above ( V_{DD} )</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>Instantaneous Peak Output Current</td>
<td>16A</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>Instantaneous Peak Output Current</td>
<td>16A</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>

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**DC Electrical Characteristics**

\( V_{DD} = V_{IN} = 5V, C_{OSC} = 1 \) nF, \( C_{SLOPE} = 68 \) pF, \( T_A = 25^\circ C \), unless otherwise specified.

\[ VDD = VIN = 5V, C_{OSC} = 1 \text{nF}, C_{SLOPE} = 68 \text{pF}, T_A = 25^\circ C, \text{unless otherwise specified} \]
**DC Electrical Characteristics**

\[ V_{DD} = V_{IN} = 5\text{V}, \ C_{OSC} = 1 \ \text{nF}, \ C_{SLOPE} = 68 \ \text{pF}, \ T_{A} = 25^\circ \text{C}, \] unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( O_{T_{OFF}} )</td>
<td>Over Temperature Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( O_{T_{HYS}} )</td>
<td>Over Temperature Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{PWRGD} )</td>
<td>Power Good Threshold with Respect to Desired Output Voltage</td>
<td>( \text{VID} = 0111 )</td>
<td>-9</td>
<td>-7</td>
<td>-5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DD-ON} )</td>
<td>Minimum ( V_{DD} ) for Startup</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DD-OFF} )</td>
<td>Maximum ( V_{DD} ) for Shutdown</td>
<td></td>
<td>3.75</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The oscillator and voltage doubler operate normally when \( V_{DD} \) exceeds \( V_{DD-ON} \) threshold, independent of the \( \text{OUTEN} \) logic level.

**Voltage Identification Codes**

<table>
<thead>
<tr>
<th>( V_{ID3} )</th>
<th>( V_{ID2} )</th>
<th>( V_{ID1} )</th>
<th>( V_{ID0} )</th>
<th>( V_{DC} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0, No CPU</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>2.1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2.2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2.3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2.4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2.5</td>
</tr>
<tr>
<td>1</td>
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<td>0</td>
<td>0</td>
<td>2.6</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2.7</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2.8</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>2.9</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>3.0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>3.1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3.2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3.3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3.4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3.5</td>
</tr>
</tbody>
</table>
## EL7560 Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Cp−</td>
<td>Negative input for the charge pump bootstrap capacitor. (Note 1)</td>
</tr>
<tr>
<td>2</td>
<td>Cp+</td>
<td>Positive input for the charge pump bootstrap capacitor. (Note 1)</td>
</tr>
<tr>
<td>3</td>
<td>C2V</td>
<td>Voltage doubler output. Pin requires at least a 1μF capacitor to GND. (Note 1)</td>
</tr>
<tr>
<td>4</td>
<td>VSS</td>
<td>Ground return for the control circuitry.</td>
</tr>
<tr>
<td>5</td>
<td>VHI</td>
<td>Positive supply for the high side driver. This pin is bootstrapped from the LX pin with a 0.1μF capacitor.</td>
</tr>
<tr>
<td>6</td>
<td>LX</td>
<td>Common connection between the two large internal FETs. External inductor connection.</td>
</tr>
<tr>
<td>7</td>
<td>LX</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>8</td>
<td>LX</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>9</td>
<td>LX</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>10</td>
<td>LX</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>11</td>
<td>TEST</td>
<td>This is test pin and <strong>must remain grounded at all times</strong></td>
</tr>
<tr>
<td>12</td>
<td>PWRGD</td>
<td>Pin pulls high when the FB pin is within −7% (typ) of its programmed value.</td>
</tr>
<tr>
<td>13</td>
<td>OT</td>
<td>Overtemperature indicator. Pulls low when the die temperature exceeds 135°C. Pin has 10 mA pull-up.</td>
</tr>
<tr>
<td>14</td>
<td>OT</td>
<td>A logic high on OUTEN enables the regulator (Note 1)</td>
</tr>
<tr>
<td>15</td>
<td>VID3</td>
<td>Bit 3(MSB) of the output voltage select DAC.</td>
</tr>
<tr>
<td>16</td>
<td>VID2</td>
<td>Bit 2 of the output voltage select DAC.</td>
</tr>
<tr>
<td>17</td>
<td>VID1</td>
<td>Bit 1 of the output voltage select DAC.</td>
</tr>
<tr>
<td>18</td>
<td>VID0</td>
<td>Bit 0 (LSB) of the output voltage select DAC.</td>
</tr>
<tr>
<td>19</td>
<td>VSSP</td>
<td>Ground return to the buck regulator.</td>
</tr>
<tr>
<td>20</td>
<td>VSSP</td>
<td>Same as pin 19.</td>
</tr>
<tr>
<td>21</td>
<td>VIN</td>
<td>Positive power supply input to the buck regulator.</td>
</tr>
<tr>
<td>22</td>
<td>VSSP</td>
<td>Same as pin 19.</td>
</tr>
<tr>
<td>23</td>
<td>VIN</td>
<td>Same as pin 21.</td>
</tr>
<tr>
<td>24</td>
<td>VDD</td>
<td>Pin supplies power to the internal control circuitry.</td>
</tr>
<tr>
<td>25</td>
<td>COSC</td>
<td>Oscillator timing capacitor. Oscillator Frequency is approximately: ( F_{OSC}(Hz) = 0.0001/C_{OSC}(F) ). The duty cycle is approximately 5%. (Note 1)</td>
</tr>
<tr>
<td>26</td>
<td>CSLOPE</td>
<td>Slope compensation capacitor.</td>
</tr>
<tr>
<td>27</td>
<td>CREF</td>
<td>External reference input pin.</td>
</tr>
<tr>
<td>28</td>
<td>FB</td>
<td>Voltage feedback pin for the buck regulator.</td>
</tr>
</tbody>
</table>
Typical Performance Curves

**IDD vs VDD**

- **Oscillator Frequency vs COSC**

- **Line Regulation (VID3:0 = 0000)**
  - $V_{IN} = 5V$
  - $T_A = 25^\circ C$

- **Load Regulation (VID3:0 = 0000)**
  - $V_{IN} = 5V$
  - $T_A = 25^\circ C$

- **Load Regulation (VID3:0 = 1101)**
  - $V_{IN} = 5V$
  - $T_A = 25^\circ C$
Typical Performance Curves — Contd.

**V\text{OUT} vs C\text{SLOPE}**

- Graph showing V\text{OUT} against C\text{SLOPE} (\text{pF})
- Legend includes markers for different slope values:
  - DV\text{out} (%)
  - Labeled curves for various slope levels

**Load and Line Regulation vs C\text{SLOPE}**

- Graph showing regulation against C\text{SLOPE} (\text{pF})
- Legend includes markers for different regulation levels:
  - DV\text{out} (%)
  - Load Reg (%)
  - Line Reg (%)

**R\text{DS}ON vs Temp**

- Graph showing R\text{DS}ON (\text{mA}) against temperature (°C)
- Equation: \( y = 0.1006x + 23.766 \)
- Legend includes markers for different temperature levels:
  - #1
  - #2
  - #3
  - Linear (#3)

**Efficiency vs Output Current**

- Graph showing efficiency against output current
- Legend includes markers for different voltage levels:
  - 3.5V
  - 2.1V
  - 1.1V

**Transient Load Step**

- 0.3 Amp → 12.4 Amp
- Graph showing transient response
- Parameters:
  - \( V_0 = 3.1 \)
  - \( I_0 = 0.3 \) to 12.4
- Waveform details:
  - \( V_{\text{OUT}} \)
  - \( 20 \text{mV/div} \)

**Switching Waveforms**

- \( I_{\text{LOAD}} = 2 \text{A} \)
- Waveform details:
  - \( V(LX) \)
  - \( V_{\text{OUT}} \)
  - \( 20 \text{mV/div} \)
  - \( 2 \text{V/div} \)
  - \( 1 \mu s \)
Figure 1. EL7560 Functional Block Diagram
Features
• 3.3V @ 12.4 amps continuous
• Internal FETs
• > 90% Efficiency
• Synchronous switching
• 4-Bit digitally adjustable output voltage
• User adjustable slope compensation
• Internal soft start
• Precision 0.5% reference
• Over temperature indicator
• Low current sleep mode
• Low parts count
• Pulse by pulse current limiting
• High efficiency at light load
• Operates up to 1 MHz
• 1% Output accuracy
• Sync function
• Power good signal

Applications
• PC Motherboards
• Local high power CPU supplies

Ordering Information
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7561CM</td>
<td>-40°C to +85°C</td>
<td>28-Pin SOIC</td>
<td>MDP0037</td>
</tr>
</tbody>
</table>

General Description
The EL7561C is the simplest, most cost effective method for powering modern high power CPUs which require a user adjustable output voltage. Although it is particularly designed to function with next generation CPUs, its simple design can provide low cost solutions for any 5V to 3V application.

The circuit uses on chip resistorless current sensing for high efficiency, stable current mode control. An on chip temperature sensor resets the OT pin. The OT pin can be tied directly to the OUTEN pin for automatic overtemperature shutdown. The user can adjust the oscillator frequency as well as the slope compensation.

The output voltage is adjustable using a 4-bit parallel interface. A power OK signal "PWRGD" pulls high when the FB pin is within 7% of the programmed value.

Connection Diagram

![Connection Diagram](image-url)
### Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (VIN)</td>
<td>$5.5\text{V}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Pins</td>
<td>$-0.3\text{V}$ below GND, $+0.3\text{V}$ above $V_{DD}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Momentary Peak Output Current</td>
<td>$16\text{A}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65^\circ\text{C}$ to $+150^\circ\text{C}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>$-40^\circ\text{C}$ to $+85^\circ\text{C}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$135^\circ\text{C}$</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Power Dissipation</td>
<td>$3\text{W}$</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

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### DC Electrical Characteristics

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<tr>
<th>Parameter</th>
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<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{2X}$</td>
<td>Voltage Doubler Output</td>
<td>$V_{DD} = 5\text{V}$, $I_{LOAD} = 20\text{mA}$</td>
<td>8.0</td>
<td>9</td>
<td>9.5</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Reference Absolute Value</td>
<td>$I_{LOAD} = 0$</td>
<td>1.150</td>
<td>1.250</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{REFTC}$</td>
<td>Reference Voltage Tempco</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>ppm/$^\circ\text{C}$</td>
<td>ppm/$^\circ\text{C}$</td>
</tr>
<tr>
<td>$V_{REFLOAD}$</td>
<td>Reference Voltage Load Regulation</td>
<td>$0 &lt; I_{LOAD} &lt; 0.5\text{mA}$</td>
<td>$-0.5$</td>
<td>0.5</td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td>$DAC_{LSB}$</td>
<td>DAC Resolution</td>
<td></td>
<td>0.095</td>
<td>0.105</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$F_{OSC}$</td>
<td>Oscillator Initial Accuracy</td>
<td>$C_{OSC} = 1000\text{pF}$</td>
<td>105</td>
<td>120</td>
<td>135</td>
<td>I</td>
<td>kHz</td>
</tr>
<tr>
<td>$F_{OSCTC}$</td>
<td>Oscillator Tempco</td>
<td>$0 &lt; T_A &lt; 125$</td>
<td>$C_{OSC} = 1000\text{pF}$</td>
<td>$\pm 0.1$</td>
<td>V</td>
<td>%/$^\circ\text{C}$</td>
<td>%/$^\circ\text{C}$</td>
</tr>
<tr>
<td>$V_{RAMP}$</td>
<td>Oscillator Ramp Amplitude</td>
<td>$C_{OSC} = 1000\text{pF}$</td>
<td>1.1</td>
<td>1.2</td>
<td>1.3</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>$M_{SS}$</td>
<td>Soft Start Slope</td>
<td>$F_{OSC} = 500\text{kHz}$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V/ms</td>
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<tr>
<td>$I_{VID}$</td>
<td>VID Pull Up Current</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>$\mu\text{A}$</td>
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<tr>
<td>$I_{CSLOPE}$</td>
<td>$C_{SLOPE}$ Charging Current</td>
<td></td>
<td>32</td>
<td>40</td>
<td>48</td>
<td>I</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply Current</td>
<td>OUTEN = 4V $F_{OSC} = 120\text{kHz}$</td>
<td>25</td>
<td>35</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDOFF}$</td>
<td>Stdby Current</td>
<td>OUTEN = 0</td>
<td>3</td>
<td>5</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$R_{DS}$</td>
<td>Composite FET Resistance</td>
<td></td>
<td>18</td>
<td></td>
<td></td>
<td>I</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$R_{DSNTC}$</td>
<td>$R_{DS}$ Tempco</td>
<td>$0 &lt; T_A &lt; 70^\circ\text{C}$</td>
<td>0.1</td>
<td></td>
<td></td>
<td>V</td>
<td>m$\Omega$/$^\circ\text{C}$</td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT}$</td>
<td>Output Initial Accuracy</td>
<td>$VID = 0111$</td>
<td>2.765</td>
<td>28</td>
<td>2.835</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RANGE}$</td>
<td>Output Voltage Range</td>
<td>$VID = 1110$ to $0000$</td>
<td>2.065</td>
<td>3.535</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{LMAX}$</td>
<td>Maximum Current</td>
<td>$V_{OUT} = 0$</td>
<td>12.5</td>
<td>15.0</td>
<td>V</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$V_{OUTTC}$</td>
<td>Output Tempco</td>
<td>$0 &lt; T_A &lt; 25^\circ C$</td>
<td>±1</td>
<td></td>
<td></td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td>$V_{OUTLINE}$</td>
<td>Output Line Regulation</td>
<td>$V_{OUT} = 2.8$</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$4.5 &lt; V_{DD} &lt; 5.5$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = V_{IN}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OUTLOAD}$</td>
<td>Output Load Regulation</td>
<td>$0.3A &lt; I_{LOAD} &lt; 12.4$</td>
<td>−1</td>
<td>1</td>
<td>I</td>
<td>IV</td>
<td>%</td>
</tr>
<tr>
<td>$V_{OUTTOT}$</td>
<td>Output Total Variation</td>
<td>−2</td>
<td>2</td>
<td>2</td>
<td>IV</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$OT_{OFF}$</td>
<td>Over Temperature Threshold</td>
<td></td>
<td>135</td>
<td></td>
<td></td>
<td>V</td>
<td>C</td>
</tr>
<tr>
<td>$OT_{HYS}$</td>
<td>Over Temperature Hysteresis</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
<td>C</td>
</tr>
<tr>
<td>$V_{PWRGD}$</td>
<td>Power Good Threshold with Respect</td>
<td>$VID = 0111$</td>
<td>±8</td>
<td>±15</td>
<td>I</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>to Desired Output Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DDON}$</td>
<td>Minimum $V_{DD}$ form Startup</td>
<td></td>
<td>4</td>
<td>I</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DDOFF}$</td>
<td>Maximum $V_{DD}$ for Shutdown</td>
<td></td>
<td>3.75</td>
<td>I</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### EL7561C Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$C_p^-$</td>
<td>Negative input for the charge pump bootstrap capacitor. (Note 1)</td>
</tr>
<tr>
<td>2</td>
<td>$C_p^+$</td>
<td>Positive input for the charge pump bootstrap capacitor. (Note 1)</td>
</tr>
<tr>
<td>3</td>
<td>$C_{2V}$</td>
<td>Voltage doubler output. Pin requires at least a 1 $\mu F$ capacitor to GND. (Note 1)</td>
</tr>
<tr>
<td>4</td>
<td>$V_{SS}$</td>
<td>Ground return for the control circuitry.</td>
</tr>
<tr>
<td>5</td>
<td>$V_{HI}$</td>
<td>Positive supply for the high side driver. This pin is bootstrapped from the LX pin with a 0.1 $\mu F$ capacitor.</td>
</tr>
<tr>
<td>6</td>
<td>LX</td>
<td>Common connection between the two large internal FETs. External inductor connection.</td>
</tr>
<tr>
<td>7</td>
<td>LX</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>8</td>
<td>LX</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>9</td>
<td>LX</td>
<td>Same as pin 6.</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>TEST</td>
<td>This is test pin and must remain grounded at all times</td>
</tr>
<tr>
<td>12</td>
<td>PWRGD</td>
<td>Pin pulls high when the FB pin is within ±10% (typ) of its programmed value.</td>
</tr>
<tr>
<td>13</td>
<td>$OT$</td>
<td>Overtemperature indicator. Pulls low when the die temperature exceeds 135°C. Pin has 10 mA pull-up.</td>
</tr>
<tr>
<td>14</td>
<td>OUTEN</td>
<td>A logic high on OUTEN enables the regulator (Note 1)</td>
</tr>
<tr>
<td>15</td>
<td>VID3</td>
<td>Bit 3(MSB) of the output voltage select DAC.</td>
</tr>
</tbody>
</table>
## EL7561 Pin Description — Contd.

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>VID2</td>
<td>Bit 2 of the output voltage select DAC.</td>
</tr>
<tr>
<td>17</td>
<td>VID1</td>
<td>Bit 1 of the output voltage select DAC.</td>
</tr>
<tr>
<td>18</td>
<td>VID0</td>
<td>Bit 0 (LSB) of the output voltage select DAC.</td>
</tr>
<tr>
<td>19</td>
<td>VSSP</td>
<td>Substrate connection.</td>
</tr>
<tr>
<td>20</td>
<td>VSSP</td>
<td>Ground return to the buck regulator.</td>
</tr>
<tr>
<td>21</td>
<td>VIN</td>
<td>Positive power supply input to the buck regulator.</td>
</tr>
<tr>
<td>22</td>
<td>VSSP</td>
<td>Same as pin 20.</td>
</tr>
<tr>
<td>23</td>
<td>VIN</td>
<td>Same as pin 21.</td>
</tr>
<tr>
<td>24</td>
<td>VDD</td>
<td>Pin supplies power to the internal control circuitry.</td>
</tr>
<tr>
<td>25</td>
<td>COSC</td>
<td>Oscillator timing capacitor. Oscillator Frequency is approximately: ( F_{osc}(\text{Hz}) = 0.0001 / C_{osc}(\text{F}) ). The duty cycle is approximately 5%. (Note 1)</td>
</tr>
<tr>
<td>26</td>
<td>C_SLOPE</td>
<td>Slope compensation capacitor.</td>
</tr>
<tr>
<td>27</td>
<td>C_REF</td>
<td>External reference input pin.</td>
</tr>
<tr>
<td>28</td>
<td>FB</td>
<td>Voltage feedback pin for the buck regulator.</td>
</tr>
</tbody>
</table>
Features
- Pentium® Pro Compatible, DAC controlled output voltage
- Greater than 90% efficiency
- 4.5V – 13.2V input range
- Fixed frequency, current mode control
- Adjustable oscillator with external sync. capability
- Synchronous switching
- Internal soft start
- User adjustable slope compensation
- Low current sleep mode
- Pulse by pulse current limiting
- 1% Output accuracy
- Power good signal

Applications
- Pentium Pro Voltage regulation modules (VRM's)
- PC Motherboards
- Synchronous rectification

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7571CM</td>
<td>-40°C to +85°C</td>
<td>20-Pin SOIC</td>
</tr>
</tbody>
</table>

General Description
The EL7571C is a flexible, high efficiency, PWM step down controller incorporating five bit DAC adjustable output voltage control which conforms to the Pentium Pro Voltage ID specification. The controller employs synchronous rectification to deliver efficiencies greater than 90% over a wide range of supply voltages and load conditions. A low power sleep mode minimizes quiescent current when the regulator is disabled. The on-board oscillator frequency is externally adjustable, or may be slaved to a system clock, allowing optimization of RFI performance in critical applications. For maximum flexibility, the control section may be powered from either 5V or 12V supplies.

Connection Diagram

Pentium® is a registered trademark of Intel Corporation.
Absolute Maximum Ratings \( (T_A = 25^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>-0.5V to 15V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pin Voltage</td>
<td>-0.3V below Ground, +0.3V above supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VHI</td>
<td>&lt; 30V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>2A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>SOIC 500 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality inspection. Elantec performs most electrical testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LXT77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_J = T_C = T_A \).

**DC Electrical Characteristics** \( T_A = 25^\circ C, V_{IN} = 5V \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>Input Voltage Range</td>
<td></td>
<td>4.5</td>
<td>13.2</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{UVLO_HI} )</td>
<td>Under Voltage Lockout High Threshold</td>
<td>Positive Going Input Voltage</td>
<td>3.6</td>
<td>4.4</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{UVLO_LO} )</td>
<td>Under Voltage Lockout Low Threshold</td>
<td>Negative Going Input Voltage</td>
<td>3.15</td>
<td>3.85</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Voltage</td>
<td>See VID Table</td>
<td>1.3</td>
<td>3.5</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{REF} )</td>
<td>Band Gap Voltage</td>
<td></td>
<td>1.26</td>
<td>1.29</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{ILIM} )</td>
<td>Current Limit Voltage</td>
<td>( V_{ILIM} = (V_{CS} - V_{REF}) )</td>
<td>135</td>
<td>165</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{TOP_LO} )</td>
<td>Power Down Input Low Level</td>
<td>( I_{IN} = \frac{10 \mu A}{V_{IN}} )</td>
<td>0</td>
<td>1.5</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{TOP_HI} )</td>
<td>Power Down Input High Level</td>
<td>( V_{IN} )</td>
<td>V_{IN}</td>
<td>V_{IN}</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{ID_LO} )</td>
<td>Voltage I.D. Input Low Level</td>
<td>0</td>
<td>1.5</td>
<td>I</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{ID_HI} )</td>
<td>Voltage I.D. Input High Level</td>
<td>( V_{IN} )</td>
<td>V_{IN}</td>
<td>V_{IN}</td>
<td>I</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OSC} )</td>
<td>Oscillator Voltage Swing</td>
<td>1</td>
<td>V</td>
<td>V</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{PWRGD_LO} )</td>
<td>Power Good Output Low Level</td>
<td>( I_{OUT} = 3.2 mA )</td>
<td>0.5</td>
<td>V</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics

$T_A = 25^\circ C, V_{IN} = 5V$ unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS_ON}$</td>
<td>HSD, LSD Switch On-Resistance</td>
<td>$I_{OUT} = -100\ mA$ ($V_{HI-LX}) &gt; 4.5V$</td>
<td></td>
<td></td>
<td></td>
<td>$I$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$R_{FB}$</td>
<td>FB Input Impedance</td>
<td></td>
<td>9.5</td>
<td></td>
<td></td>
<td>$V$</td>
<td>$k\Omega$</td>
</tr>
<tr>
<td>$I_{VIN}$</td>
<td>Quiescent Supply Current</td>
<td>$V_{OTEN} &gt; (V_{DD} - 0.5)$</td>
<td>1.5</td>
<td>3</td>
<td></td>
<td>$I$</td>
<td>$mA$</td>
</tr>
<tr>
<td>$I_{VIN_SLEEP}$</td>
<td>Supply Current in Sleep Mode</td>
<td>$V_{OTEN} &lt; 0.5V$</td>
<td>100</td>
<td>$I$</td>
<td></td>
<td>$I$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{SOURCE/SINK}$</td>
<td>Driver Output Current</td>
<td>Measured at HSD, LSD, ($V_{HI-LX}) &gt; 4.5V$</td>
<td>1</td>
<td></td>
<td></td>
<td>$IV$</td>
<td>$A$</td>
</tr>
<tr>
<td>$I_{RAMP}$</td>
<td>CSLOPE Ramp Current</td>
<td>High Side Switch Enabled</td>
<td>6</td>
<td>14</td>
<td></td>
<td>$I$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{OSC_CHARGE}$</td>
<td>Oscillator Charge Current</td>
<td>$1.2 &gt; V_{OSC} &gt; 0.2V$</td>
<td>50</td>
<td></td>
<td></td>
<td>$V$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{OSC_DISCHARGE}$</td>
<td>Oscillator Discharge Current</td>
<td>$1.2 &gt; V_{OSC} &gt; 0.2V$</td>
<td>1.6</td>
<td></td>
<td></td>
<td>$V$</td>
<td>$mA$</td>
</tr>
<tr>
<td>$I_{REF_MAX}$</td>
<td>$V_{REF}$ Output Current</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>$V$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{VID}$</td>
<td>VID Input Pull-Up Current</td>
<td></td>
<td>3</td>
<td>7</td>
<td></td>
<td>$I$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{OTEN}$</td>
<td>OTEN Input Pull-Up Current</td>
<td></td>
<td>3</td>
<td>7</td>
<td></td>
<td>$I$</td>
<td>$\mu A$</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

$T_A = 25^\circ C, V_{IN} = 5V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{OSC}$</td>
<td>Nominal Oscillator Frequency</td>
<td>$C_{OSC} = 400\ pF$</td>
<td>102</td>
<td></td>
<td>138</td>
<td>$I$</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency</td>
<td></td>
<td>100</td>
<td>500</td>
<td>1000</td>
<td>$IV$</td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{OTEN}$</td>
<td>Shutdown Delay</td>
<td>$V_{OTEN} = 0.8V$</td>
<td>100</td>
<td></td>
<td></td>
<td>$V$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SYNC}$</td>
<td>Sync. Pulse Width</td>
<td></td>
<td>10</td>
<td>50</td>
<td></td>
<td>$IV$</td>
<td>ns</td>
</tr>
<tr>
<td>$T_{START}$</td>
<td>Soft Start Period</td>
<td></td>
<td>100/$f_{CLK}$</td>
<td>$V$</td>
<td></td>
<td>$\mu s$</td>
<td></td>
</tr>
<tr>
<td>$D_{MAX}$</td>
<td>Maximum Duty Cycle</td>
<td></td>
<td>97</td>
<td></td>
<td></td>
<td>$V$</td>
<td>%</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Pin Name</td>
<td>Pin Type</td>
<td>Function</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>----------</td>
<td>----------</td>
<td>----------</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>OTEN</td>
<td>I</td>
<td>Chip enable input, internal pull-up (5 (\mu)A typical). Active high.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>CSLOPE</td>
<td>I</td>
<td>With a capacitor attached from CLSLOPE to GND, generates the voltage ramp compensation for the PWM current mode controller. Slope rage is determined by an internal 10 (\mu)A pull up and the CSLOPE capacitor value. (V_{CSLOPE}) is reset to ground at the termination of the high side cycle.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>COSC</td>
<td>I</td>
<td>Multi-function pin: with a timing capacitor attached, sets the internal oscillator rate (f_{CLK}); when pulsed low for a duration (t_{SYNC}) synchronizes device to an external clock.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>REF</td>
<td>O</td>
<td>Band gap reference output. Decouple to GND with 0.1 (\mu)F.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PWRGD</td>
<td>O</td>
<td>Power good, open drain output. Set low whenever the output voltage is not within (\pm 10%) of the programmed value.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>VID0</td>
<td>I</td>
<td>Bit 0 of the output voltage select DAC. Pull up sets input high when not driven.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>VID1</td>
<td>I</td>
<td>Bit 1 of the output voltage select DAC. Pull up sets input high when not driven.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>VID2</td>
<td>I</td>
<td>Bit 2 of the output voltage select DAC. Pull up sets input high when not driven.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>VID3</td>
<td>I</td>
<td>Bit 3 of the output voltage select DAC. Pull up sets input high when not driven.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>VID4</td>
<td>I</td>
<td>Bit 4 of the output voltage select DAC. Pull up sets input high when not driven.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>FB</td>
<td>I</td>
<td>Voltage regulation feedback input. Tie to (V_{OUT}) for normal operation.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>CS</td>
<td>I</td>
<td>Current Sense. Current feedback input of PWM controller and over current comparator input. Current Limit threshold set at (+150) mV with respect to FB. Connect sense resistor between CS and FB for normal operation.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>GND</td>
<td>S</td>
<td>Ground.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>GNDP</td>
<td>S</td>
<td>Power ground for low side FET Driver. Tie to GND for normal operation.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>LSD</td>
<td>O</td>
<td>Low side gate drive output.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>VINP</td>
<td>S</td>
<td>Input supply voltage for low side FET driver. Tie to VIN for normal operation.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>VIN</td>
<td>S</td>
<td>Input supply voltage for control circuit.</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>18</td>
<td>LX</td>
<td>I</td>
<td>Negative supply input of high side drive circuit.</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>19</td>
<td>HSD</td>
<td>O</td>
<td>High side gate drive output. Driver ground referenced to LX. Driver supply may be bootstrapped to enhance low controller input voltage operation.</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>20</td>
<td>VHI</td>
<td>I</td>
<td>Positive supply input of high side drive circuit.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Block Diagram
Application Specific
A.T.E./Comparators

élan
tec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
### Drivers - Bipolar

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>$V_O$</th>
<th>$I_O$</th>
<th>Slew Rate</th>
<th>$I_S$</th>
<th>Standby $I_S$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Min</td>
<td>Max</td>
<td>P = Pins</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>J = CerDIP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>M = SOL</td>
</tr>
<tr>
<td>EL2021C</td>
<td>3-State Output</td>
<td>$-6.1V$</td>
<td>$-5.9V$</td>
<td>$\pm 500mA$</td>
<td>$40V/\mu s$</td>
<td>$360V/\mu s$</td>
<td>$45mA$</td>
</tr>
<tr>
<td></td>
<td>Programmable Slew Rate,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Short Circuit Current Sense</td>
<td>to</td>
<td>to</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$+10.9V$</td>
<td>$+11.1V$</td>
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<tr>
<td>EL1056C</td>
<td>Adjustable Slew Rate, Wide Voltage Range,</td>
<td>$-12V$</td>
<td>$-12V$</td>
<td>$\pm 50mA$DC</td>
<td>$0.1V/\mu s$</td>
<td>$1.2V/\mu s$</td>
<td>$60mA$</td>
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<tr>
<td></td>
<td>Power Down</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>EL1056AC</td>
<td></td>
<td></td>
<td></td>
<td>$\pm 150mA$DC</td>
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</tr>
</tbody>
</table>

### Drivers - CMOS

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>$I_{peak}$</th>
<th>$R_{ON}$</th>
<th>$T_r/T_f$</th>
<th>$V_{supply}$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td>P = Pins</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N = PDIP</td>
</tr>
<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>S = SOIC</td>
</tr>
<tr>
<td><strong>POWER MOSFET DRIVERS</strong></td>
<td></td>
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</tr>
<tr>
<td>EL7134C</td>
<td>Single, 3-State</td>
<td>$4A$</td>
<td>3$\Omega$</td>
<td>$20ns/20ns$</td>
<td>$16.5V$</td>
<td>8P-N-S</td>
</tr>
<tr>
<td>EL7232C</td>
<td>Dual, 3-State</td>
<td>$2A$</td>
<td>6$\Omega$</td>
<td>$20ns/20ns$</td>
<td>$16.5V$</td>
<td>8P-N-S</td>
</tr>
</tbody>
</table>

**Special Function Drivers**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>$I_{peak}$</th>
<th>$R_{ON}$</th>
<th>$T_r/T_f$</th>
<th>$V_{supply}$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>P = Pins</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>N = PDIP</td>
</tr>
<tr>
<td></td>
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<td>S = SOIC</td>
</tr>
<tr>
<td>EL7154C</td>
<td>ATE/ $\pm 15V$ to $-5V$ Outputs,</td>
<td>$2A$</td>
<td>2.5$\Omega$</td>
<td>$20ns/20ns$</td>
<td>$16.5V$</td>
<td>8P-N-S</td>
</tr>
<tr>
<td></td>
<td>Level Shifter/3-State</td>
<td></td>
<td></td>
<td></td>
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</table>

### Comparators

<table>
<thead>
<tr>
<th>Part #</th>
<th>Features</th>
<th>Typ Prop Delay ($5mV$ Overdrive)</th>
<th>Typ Open Loop Gain</th>
<th>Input Common Mode Range</th>
<th>Typ Input Bias Current</th>
<th>Max Supply Current</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$20ns$</td>
<td></td>
<td>($V_{CC}$ = $\pm 15V$)</td>
<td>($V_{CC}$ = $\pm 5V$)</td>
<td>Output Active</td>
<td>P = Pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$\pm 12V$</td>
<td>$\pm 3V$</td>
<td>$\pm 100nA$</td>
<td>N = PDIP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(Min)</td>
<td>(Typ)</td>
<td>+11 mA/ -18 mA</td>
<td>M = SOL</td>
</tr>
<tr>
<td>EL2018C</td>
<td>Fast, High Voltage w/Latch 3-State Output</td>
<td>$20ns$</td>
<td>$40,000V/V$</td>
<td>$\pm 12V$</td>
<td>$\pm 3V$</td>
<td>+11 mA/ -18 mA</td>
<td>8P-N</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(92 dB)</td>
<td>(Min)</td>
<td>(Typ)</td>
<td>+7 mA/ -6.5 mA</td>
<td></td>
</tr>
<tr>
<td>EL2252C</td>
<td>50 MHz, Dual, High Voltage</td>
<td>$6ns$</td>
<td>$8,000V/V$</td>
<td>$-12V$, $+13V$</td>
<td>$17\mu A$</td>
<td>$+19mA/20mA$</td>
<td>14P-N</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(Both Comparators)</td>
<td>20P-M</td>
</tr>
</tbody>
</table>
Features
- Wide ±12V output levels
- 250 ps dispersion
- 3 ns delay times
- 1V/µs slewing rate—adjustable
- Low overshoot and aberrations in 50Ω systems
- 3-state output
- Power-down mode reduces output leakage to nanoamperes
- Overcurrent sense flag available to protect internal output devices
- Buffered analog inputs
- Differential logic inputs are compatible with ECL, TTL, and CMOS

Applications
- Memory testers
- ASIC testers
- Functional board testers
- Analog/digital incoming component verifiers
- Logic emulators

General Description
The EL1056 is designed to drive high-quality test signals into close or terminated loads. It has a dispersion of 250 ps or less—whether due to signal size or direction of edge. It can output a very wide 24V output span, encompassing all logic families as well as analog levels. The EL1056 is fabricated in Elantec's oxide isolated process, which eliminates the possibility of latch-up and provides a very durable circuit.

The output can be turned off in two ways; the OE pins allow the output to be put in a high-impedance state which makes the output look like a large resistance in parallel with 3 pF, even for back-driven signals with as much as 2.5V/µs slew rate. The E pins put the output in an even higher impedance state, guaranteed to 150 nA leakage in the EL1056A. This allows accurate measurements on the bus without disconnecting the EL1056 with a relay.

The EL1056 incorporates an output current sense which can warn the system controller that excessive output current is flowing. The trip point is set by two external resistors.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL1056CM</td>
<td>0°C to +75°C</td>
<td>24-Lead</td>
<td>MDP0027 Thermal SOL</td>
</tr>
<tr>
<td>EL1056ACM</td>
<td>0°C to +75°C</td>
<td>24-Lead</td>
<td>MDP0027 Thermal SOL</td>
</tr>
</tbody>
</table>

Connection Diagram

24-Lead Thermal SOL Package

Top View

*and Heat-spreader
Absolute Maximum Ratings ($T_A = 25°C$)

- $V_S$: Voltage between $V+$ and $V-$, $-33V$ to $+33V$
- $V-$: Supply Voltage, $-18V$
- $B+$: Supply Voltage, $V_{INH}$ to $V+$
- $B-$: Supply Voltage, $V-$ to $V_{INL}$
- $I_{SR}$: Input Current, $0$ mA to $3$ mA
- $V_{SR}$: Input Voltage, $0.3V$ to $+6V$
- $I_{OUT}$: Output Current, $-60$ mA to $+60$ mA
- $I_{SHUNT+}$: Input Voltage, $-0.3V$ to $+6V$
- $I_{SHUNT-}$: Supply Voltage, $B-$ to $V_{INH} + 0.3V$

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $I_{SHUNT+}, I_{SHUNT-} = 6.51$, no load. Data, $E$, and OE from $-1.6V$ to $-0.8V$. $I_{SR} = 800 \mu A$. $V_{INH} = 5V$, $V_{INL} = -1.6V$

DC Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>$(V+) + (B+) + (V-) + (B-)$ Supply Currents</td>
<td>52</td>
<td>60</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{S,\text{dis}}$</td>
<td>$(V+) + (B+) + (V-) + (B-)$ Supply Currents, Disabled</td>
<td>17</td>
<td>25</td>
<td>I</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{VINH}$</td>
<td>$I_{VINH}$</td>
<td>$-20$</td>
<td>$-3$</td>
<td>$20$</td>
<td>I</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{VINL}$</td>
<td>$I_{VINL}$</td>
<td>$-20$</td>
<td>$2$</td>
<td>$20$</td>
<td>I</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{DATA}$</td>
<td>$I_{DATA}$</td>
<td>$-30$</td>
<td>$-15$</td>
<td>$30$</td>
<td>I</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{OE}$</td>
<td>OE Input Current</td>
<td>$-30$</td>
<td>$-14$</td>
<td>$30$</td>
<td>I</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_E$</td>
<td>E Input Current</td>
<td>$-20$</td>
<td>$7$</td>
<td>$20$</td>
<td>I</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$V_{SR}$</td>
<td>Voltage at $I_{SR}$ Pin</td>
<td>$0$</td>
<td>$20$</td>
<td>$40$</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{SHUNT+}, V_{SHUNT-}$</td>
<td>Sense Threshold at Shunts</td>
<td>$160$</td>
<td>$200$</td>
<td>$250$</td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{SENSE}$</td>
<td>Sense Output Currents</td>
<td>$1$</td>
<td>$1.5$</td>
<td>$2$</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Output Offset, Data High, $V_{INH} = 0V$, $V_{INL} = -1.6V$</td>
<td>$-50$</td>
<td>$50$</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data Low, $V_{INL} = 0V$, $V_{INH} = 5V$</td>
<td>$-100$</td>
<td>$100$</td>
<td>I</td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>
**DC Electrical Characteristics — Contd.**

$T_A = 25°C, V_+ = B_+ = +15V, V_- = B_- = -10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω$, no load. Data, E, and OE from $-1.6V$ to $-0.8V$. $I_{SR} = 800 μA$. $V_{INH} = 5V, V_{INL} = -1.6V$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$</td>
<td>Gain Error Data High, $V_{INH}$ from 0V to 5V, $V_{INL} = -1.6V$, No Load</td>
<td>-1.5</td>
<td>-0.6</td>
<td>0</td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Data Low, $V_{INH} = 5V$, $V_{INL}$ from -5V to 0V, No Load</td>
<td>-1.5</td>
<td>-0.6</td>
<td>0</td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>$NL$</td>
<td>Gain Nonlinearity Data High, $V_{INH}$ from 0V to 10V, $V_{INL} = -1.6V$, No Load</td>
<td>0.04</td>
<td>0.06</td>
<td>V</td>
<td>V</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Data Low, $V_{INH} = 5V$, $V_{INL}$ from -10V to 0V, No Load</td>
<td>2.2</td>
<td>V</td>
<td>mV/V</td>
<td></td>
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<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio of $V_{OUT}$ with Respect to $B_+, B_-, Shunt +, or Shunt - Potential$</td>
<td>4.5</td>
<td>6</td>
<td>7.5</td>
<td>1</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{on, en}$</td>
<td>Output Resistance, Enabled, $I = ± 20 mA$</td>
<td>20K</td>
<td>100K</td>
<td>100K</td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{on, dis}$</td>
<td>Output Resistance, Output Disabled, $V_O = -1.6V$ to -5V, EL1056C</td>
<td>250</td>
<td>450</td>
<td>I</td>
<td>ps</td>
<td></td>
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<tr>
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<td>EL1056AC</td>
<td>250</td>
<td>450</td>
<td>I</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data Low, $V_{INH} = -1.6V$, No Load</td>
<td>80</td>
<td>V</td>
<td>ps</td>
<td></td>
<td></td>
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<tr>
<td>$I_{on, dis}$</td>
<td>Output Current, Output Disabled, $V_O = 0V$</td>
<td>-20</td>
<td>5</td>
<td>20</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{on, off}$</td>
<td>Output Leakage, E Low, (Shut-Down), $V_O = 0V$, EL1056C</td>
<td>-20</td>
<td>20</td>
<td>I</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EL1056AC</td>
<td>-150</td>
<td>150</td>
<td>I</td>
<td>nA</td>
<td></td>
</tr>
</tbody>
</table>

**AC Electrical Characteristics**

$T_A = 25°C, V_+ = B_+ = +15V, V_- = B_- = -10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω, R_L = 500Ω, 50Ω + 22 pF snubber included at output. Data, E, and OE from $-1.6V$ to $-0.8V$. $I_{SR} = 800 μA$. ECL swing is defined by $V_{INH} = -0.8V$ and $V_{INL} = -1.6V$, CMOS swing defined by $V_{INH} = 5V$ and $V_{INL} = 0V$. Propagation delay is measured at 0.4V movement of output.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{PD}$</td>
<td>Propagation Delay, CMOS Swing</td>
<td>1.0</td>
<td>3.0</td>
<td>4.5</td>
<td>I</td>
<td>ns</td>
</tr>
<tr>
<td>$Dis$</td>
<td>Propagation Delay Dispersion</td>
<td>250</td>
<td>450</td>
<td>I</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Due to Output Edge Direction</td>
<td>250</td>
<td>450</td>
<td>I</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>From ECL to CMOS Swings</td>
<td>80</td>
<td>V</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$SR$</td>
<td>Output Slew Rate, CMOS Swing, 20%–80%</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td>I</td>
<td>V/ns</td>
</tr>
<tr>
<td>$SR_{sym}$</td>
<td>Slew Rate Symmetry</td>
<td>3</td>
<td>10</td>
<td>I</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$TR$</td>
<td>Output Rise Time, ECL Swing, 20%–80%</td>
<td>2.2</td>
<td>V</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>$OS$</td>
<td>Output Overshoot</td>
<td>190</td>
<td>500</td>
<td>I</td>
<td>mV</td>
<td></td>
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<tr>
<td></td>
<td>CMOS Swing</td>
<td>65</td>
<td>500</td>
<td>V</td>
<td>mV</td>
<td></td>
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<tr>
<td></td>
<td>ECL Swing ($I_{SR} = 350 μA$)</td>
<td>65</td>
<td>500</td>
<td>V</td>
<td>mV</td>
<td></td>
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<tr>
<td>$T_{dis}$</td>
<td>Output Disable Delay Time</td>
<td>4.7</td>
<td>6.5</td>
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<td>ns</td>
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<tr>
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<td>I</td>
<td>ns</td>
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<td>Output Capacitance in Disable</td>
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<td>V</td>
<td>pF</td>
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<tr>
<td>$T_{off}$</td>
<td>Power-Down Delay Time</td>
<td>0.5</td>
<td>V</td>
<td>μs</td>
<td></td>
<td></td>
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<tr>
<td>$T_{on}$</td>
<td>Power-On Delay Time</td>
<td>90</td>
<td>V</td>
<td>ns</td>
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<tr>
<td>$C_{on, off}$</td>
<td>Output Capacitance in Power-Down</td>
<td>50</td>
<td>V</td>
<td>pF</td>
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<td>$T_{sense}$</td>
<td>Comparator Delay Time — Switching ON</td>
<td>1.5</td>
<td>V</td>
<td>μs</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Switching Off</td>
<td>0.4</td>
<td>V</td>
<td>μs</td>
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</table>
Typical Performance Curves

10V, CMOS, TTL, and ECL Outputs into 550Ω Load

CMOS and ECL Outputs As Seen at the End of an Unterminated Cable, Backmatched at Driver

CMOS Output at ISR = 100 μA, 200 μA, 400 μA, and 1000 μA

Propagation Delay vs ISR

Output Slewrate vs ISR (Two Samples)

Output Slewrate vs Die Temperature

Die Temperature (°C)
Typical Performance Curves — Contd.

**Propagation Delay Change with Die Temperature**

- $V_+, B_+ = 15V$
- $V_- , B_- = -10V$
- $R_L = 550\Omega$
- $I_{SR} = 1\ mA$

![Graph showing change in propagation delay with die temperature](image)

**Change in Propagation Delay with Power Supply Headroom**

- $R_L = 550\Omega$
- $V_{IH} = 5V$
- $V_{IL} = 0V$
- $I_{SR} = 1\ mA$

![Graph showing change in propagation delay with power supply headroom](image)

**Output Edge Dispersion vs Temperature**

- $V_+ = B_+ = 15V$
- $V_- = B_- = -10V$
- $I_{SR} = 1\ mA$
- $R_L = 550\Omega$
- 0.4V movement

![Graph showing output edge dispersion vs temperature](image)

**Edge Dispersion vs $I_{SR}$**

- 50% point of CMOS swing
- 0.4V movement of CMOS swing
- ECL swing

![Graph showing edge dispersion vs $I_{SR}$](image)

**Minimum Output Pulse Width**

- $D = 1, V_{INH} = 5V$
- $D = 0, V_{INL} = 0V$

![Graph showing minimum output pulse width](image)
Typical Performance Curves — Contd.

Tristate Turn-off Waveforms

![Tristate Turn-off Waveform](image)

Tristate Turn-on Waveforms

![Tristate Turn-on Waveform](image)

Power-Down Disable Waveforms

![Power-Down Disable Waveform](image)

Power-Down Enable Waveforms

![Power-Down Enable Waveform](image)

Supply Current vs $I_{SR}$

![Supply Current vs $I_{SR}$](image)

Total Supply Current vs Supply Voltage

![Total Supply Current vs Supply Voltage](image)
Typical Performance Curves — Contd.

 Mounted Thermal Resistance of Package vs Airflow Speed

![Graph showing Mounted Thermal Resistance vs Airflow Speed]

Package Power Dissipation vs Ambient Temperature

![Graph showing Package Power Dissipation vs Ambient Temperature]

Sense Comparator Delay vs Overdrive

![Graph showing Sense Comparator Delay vs Overdrive]

EL1056 Used in CMOS and TTL Systems

![Diagram of EL1056 schematic]

7-10
Applications Information

Functional Description
The EL1056 is a fully integrated pin driver for automatic test systems. Pin drivers are essentially pulse generators whose high and low levels can be externally programmed and accurately switched in time, as well as incorporating an output switch to disconnect the driver from a measurement bus. Additionally, the EL1056 has programmable slewrate.

Control Voltage Inputs
The analog level inputs are named \( V_{\text{INH}} \) and \( V_{\text{INL}} \), and the output replicates them as controlled by logic inputs. The analog inputs are buffered and have bandwidths of 35 MHz and slewrates of 25V/\( \mu \)s. For full slewrate, 4V of headroom should be given to the inputs, that is \( V_{\text{INH}} \) should be 4V less than \( V^+ \) or \( B^+ \), and \( V_{\text{INL}} \) should be 4V more positive than \( V^- \) or \( B^- \). At lower slewrates (\( I_{\text{SR}} = 500 \mu \)A or less), 3V of headroom will suffice. Insufficient headroom causes distorted output waveforms or delay errors in output transitions. \( V_{\text{INH}} \) may be lower in voltage than \( V_{\text{INL}} \), but the output will not follow the control logic correctly. Furthermore, \( V_{\text{INH}} \) should be 200 mV more positive than \( V_{\text{INL}} \) (the minimum output amplitude) for accurate switching.

Logic Inputs
The logic inputs are all differential types, with both NPN and PNP transistors connected to each terminal. They are optimized for differential ECL drive, which optimizes \( + \) to \( - \) edge delay time matching. Larger logic levels can introduce feedthrough glitches into the output waveform. For CMOS input logic levels, an ECL output waveform will show feedthrough when the input risetime is shorter than 8 ns, differential or single-ended. CMOS output swings show less aberration, and the EL1056 can tolerate a 4 ns single-ended risetime or 2 ns risetime for differential inputs. Attenuating CMOS or TTL inputs to 1 Vp-p will eliminate all logic feedthrough as shown in Figure 1.

Slewrate Control
The slewrate is controlled by the \( I_{\text{SR}} \) input. This is a current input and scales the output slewrate by a nominal 1.25V/ns/\( \mu \)A. The slewrate maintains calibration and symmetry to at least as slow as 0.2V/ns. The practical upper end of \( I_{\text{SR}} \) is 1 mA, and supply current increases with increasing \( I_{\text{SR}} \).

The \( I_{\text{SR}} \) control can be used to adjust individual pin drivers to a system standard, by adjusting the value of its series resistor. Slewrate can also be slowed to reduce output ringing and crosstalk.

With ECL output swings, there is not enough voltage excursion to incur slewrate delays to 50% logic threshold. The risetime, delays, and dispersions do not degrade with reasonably reduced \( I_{\text{SR}} \), and overshoot will reduce markedly. An \( I_{\text{SR}} \) of 350 \( \mu \)A produces a very good ECL output, and driver dissipation is also reduced.
Applications Information — Contd.
The $I_{SR}$ pin is connected to the emitter of a PNP transistor whose base is biased a diode below ground (see Figure 2). Thus, the $I_{SR}$ input looks like a low impedance for positive input currents, and is biased close to ground. A protection diode absorbs negative currents, and the input PNP will not conduct. In power-down mode, the PNP releases its current sink and the external circuit must not present more than 6V to the disabled $I_{SR}$ input, or emitter-base damage to the NPN will occur within the driver. A signal diode or zener can be used to clamp the $I_{SR}$ input for positive input voltages if the voltage on the $I_{SR}$ resistor is potentially greater than 6V when the driver is in power-down mode.

Output Stage—Tristate Mode
In tristate mode (OE low) the output transistors have their emitter-base junctions reverse-biased by a diode voltage. This turn-off voltage is in fact provided by an internal buffer whose input is connected to the output pin (see Figure 3). Transistors Q1–Q4 form the output buffer in normal mode. The tristate mode buffer Q5–Q8 replicates externally impressed voltages from the output pin onto the internal schottky switch node. They also turn off Q1–Q4 by a reverse diode voltage between bases and emitters, effectively bootstrapping the internal voltages, so that no transistor's base-emitter junction is reverse-biased by a damaging potential. Another benefit is that the capacitance seen at the output in tristate mode is reduced.

Because the tristate buffer's input is connected to the output terminal, the output is quite "alive" during tristate. For instance, the input bias current of the buffer is seen as the tristate "leakage", and its variation with applied voltage becomes tristate input impedance.

The tristate input current is like a current source, and it can drag an output to unpredictable voltages. It is not a danger to connect a tristated output that has drifted to, say, −6V to a logic pin of a device to be tested. The tristate output current will simply comply with whatever voltage the connected part normally establishes.

The tristate input impedance is also quite active over frequency. The output can oscillate when presented with resonant or inductive impedances. To prevent this, a snubber should be connected from output to ground, consisting of a resistor in series with a small capacitor. The snubber can also reduce the reflections of the coaxial line when driven from the far end, since the line appears to have an open termination during tristate. Typical values for the resistor are 50Ω to 75Ω, and 12 pF to 22 pF for the series capacitor. The effect of the snubber is to "de-Q" resonances at the output.

![Figure 2. $I_{SR}$ Pin Circuitry](image)
Applications Information — Contd.

Output Stage—Normal Mode
Capacitive loads can cause the output stage to ring. Little ringing occurs for loads less than 25 pF, but substantial ringing for more than 40 pF. Terminated transmission lines cause no ringing, and actually suppress it as a snubber does. A terminated line draws heavy DC current, however, and greatly raises dissipation.

Driving a back-terminated line also causes little ringing and does not cause DC dissipation. The series matching resistor between the EL1056 output and a back-terminated line also serves to isolate the driver from capacitive loads and short-circuits. The slewrate of the driver slows by about 10% when driving a 50Ω back-matched line, as seen at the end of the line. The snubber can be on either side of the back-match resistor. When placed on the line side it creates a high-frequency termination for the line when the driver is tristated, but it slows the output small-signal risetime by about 10% (although not slew-rate). When placed on the driver side of the back-match resistor, no speed reduction occurs in normal mode but the cable is more poorly terminated in tristate.

The transient currents that occur when driving capacitive or back-matched loads can be very high, approaching 100 mA. The driver is capable of outputting a peak of 140 mA, but long-term
Applications Information — Contd.

Load currents must be limited to 60 mA. Short-circuits can rapidly destroy the EL1056, although the part will survive for 20 ms periods. If there is the possibility of output load fault the overcurrent sense circuitry should be used to signal alarm to the controlling system, which should ultimately activate the tristate mode to relieve the output stage. Driving large static currents also raises internal dissipation and should be part of the thermal budget.

The collectors of the output transistors are connected to the Shunt terminals, and the output stage drivers' collectors are connected to the B+ and B− terminals (see Figure 4). The Shunt lines can have transient currents as high as 120 mA and are separated from the V+ and V− terminals to keep switching noise out of the control and logic circuitry. A bypass capacitor should be connected to the B+ and B− terminals.

Figure 4. Output Stage in Normal Mode
Applications Information — Contd.

Overcurrent Protection
The sense comparators are available to alert the test system’s controller that the driver is outputting excessive current. Shunt resistors are connected from B+ to Shunt+ and B− to Shunt−. When the internal comparators sense more than a nominal 200 mV drop on the shunts, they cause a 1.5 mA current to be sunk from the Sense terminal. The comparators are of “slow attack, fast decay” design, so that transient load currents will not trigger a sense output; only a sustained overcurrent will.

The sense resistors must not be inductive, and the skin resistance of long, narrow connections between Shunt and B+ or B− can cause transient voltages that produce output overshoot (but not ringing).

The Sense output is simply a switched current source connected to V−. It can be used to interface to CMOS, TTL, or ECL inputs. For CMOS and TTL, it can be connected to a pull-up resistor to +5V of 10K value. This establishes a logic high value, and a clamp diode (internal to TTL) establishes a low level of −0.6V. For ECL, a gate should be available to provide a static logic high level. An 820Ω pull-up resistor is wired to that output. The logic low will be more negative than usual for ECL, but this will cause no problem. In all cases, multiple Sense outputs may be connected together from many drivers to effect a wired-or function.

A further protection scheme is to provide a series resistor from B+ to V+ and B− to V−. The resistor serves to limit the output fault current by allowing B+ and B− voltages to sag under heavy load. This also reduces the dissipation on the output transistors for valid loads. Because B+ and B− are separately bypassed, these voltages will sustain under transient loads and dynamics will not be affected.

Output Accuracy
The accuracy of the output voltage depends on several factors. The first is the gain error from VINH or VINL to the output, unloaded. The gain error is nominally −0.6%, and has a few tenths of a percent variation between parts. The second is supply rejection. If the B+, B−, Shunt+, or Shunt− voltages are different from those used by Elantec to test the part, there will be about 2.2 mV systematic shift in output offset per volt of supply variation. The V+ and V− supplies have much less influence on output error. Finally, there is a random VOS error as specified in the data table.

Of course, the finite output impedance of the EL1056 will cause additional output error when the driver is loaded.

Power-Down
The EL1056 incorporates a power-down feature that drastically reduces power consumption of an unused driver and also drops the output leakage current to nanoamperes (“A” grade only). The output is not a low capacitance in this mode, however, and transients driven from the cable can momentarily turn on the output transistors. Power-down is intended to allow the switching of accurate DC meters onto the bus without having to relay out the driver’s leakage current. It takes about 40 μs for the output leakage to sag to nanoamperes, but this is still much faster than relays or voltmeters.

Power-down is controlled by the E and E differential inputs. There is no problem with logic amplitude or slewrated, and input resistor networks are not needed.
Power Down — Contd.

Supply and Input Bypassing
The V+, B+, V-, and B- leads should be bypassed very closely with 0.1 µF capacitors, preferably chip type. There should be a wide ground plane between bypasses, and this can be the heatsink copper. It is wise to also have a 4.7 µF tantalum bypass capacitor within a couple of inches to the driver.

The logic inputs are active device bases, and can oscillate if presented with inductive lines. A local resistor of 1000Ω or less to ground will suffice in de-Q'ing any resonance. A 100 pF or larger capacitor can also serve as a bypass.

Thermal Considerations
The package of the EL1056 includes two fused leads on each side which are connected to the internal die mounting metal. Heat generated in the die flows through the mounting pad to the fused leads, and then to the circuit-board copper, achieving a thermal resistance to air around 40°C/W. Characterization curves show the thermal resistance versus airflow rate. Consult the EL1056 Demonstration Board literature for a suggested board pattern. Note that thicker layers of copper than we used improves the thermal resistance further, to a limit of 22°C/W for an “infinite heatsink” directly soldered to the fused leads.

As a practical limit, the die temperature should be kept to 125°C rather than the allowable 150°C to retain optimum timing accuracies.
EL2018C
Fast, High Voltage Comparator with Transparent Latch

Features
- Fast response time—20 ns
- Wide input differential voltage range—24V to ±15V supplies
- Precision input stage—
  \( V_{OS} = 1 \text{ mV} \)
- Low input bias current—
  \( I_B = 100 \text{ nA} \)
- Low input offset current—
  \( I_{OS} = 30 \text{ nA} \)
- ±4.5V to ±18V supplies
- 3-State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain—40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

Applications
- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- “Go/no-go” detector

General Description
The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec’s proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec’s processing, see QRA1: *Elantec’s Processing—Monolithic Products.*

Connection Diagram

8-Pin Plastic DIP

Top View
**Absolute Maximum Ratings** \( (T_A = 25\, ^\circ C) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tbody>
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<td>( V_S )</td>
<td>Supply Voltage</td>
<td>±18V</td>
<td></td>
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<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>( V_{IN} )</td>
<td>Input Voltage</td>
<td>+( V_S ) to −( V_S )</td>
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<td></td>
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<td>( \Delta V_{IN} )</td>
<td>Differential Input Voltage</td>
<td>Limited only by Power Supplies</td>
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<td>( I_{IN} )</td>
<td>Input Current (Pins 1, 2 or 3)</td>
<td>±10 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>( I_{INS} )</td>
<td>Input Current (Pins 5 or 6)</td>
<td>±5 mA</td>
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<td></td>
<td></td>
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<td>nA</td>
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<td>( P_D )</td>
<td>Maximum Power Dissipation</td>
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**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \( T_{J} = T_{C} = T_{A} \).

**DC Electrical Characteristics** \( V_S = \pm 15V \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>25, ^\circ C</td>
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<td>5</td>
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<td>I</td>
<td>mV</td>
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<td></td>
<td>(Note 1) ( V_{CM} = 0V, V_O = 1.4V )</td>
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<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>25, ^\circ C</td>
<td>100</td>
<td>400</td>
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<td>I</td>
<td>nA</td>
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<td></td>
<td>( V_{CM} = 0V )</td>
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<td></td>
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<td></td>
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<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td>25, ^\circ C</td>
<td>30</td>
<td>150</td>
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<td>I</td>
<td>nA</td>
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<td>( V_{CM} = 0V )</td>
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<tr>
<td>( CMRR )</td>
<td>Common Mode Rejection Ratio</td>
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<td>85</td>
<td>105</td>
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<td>I</td>
<td>dB</td>
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<td></td>
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<td>( PSRR )</td>
<td>Power Supply Rejection Ratio</td>
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<td>100</td>
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<td>I</td>
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<tr>
<td>( V_{CM} )</td>
<td>Common Mode Input Range</td>
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<td>±12</td>
<td>±13</td>
<td></td>
<td>I</td>
<td>V</td>
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<td>( Av )</td>
<td>Voltage Gain</td>
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<td>40</td>
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<td>I</td>
<td>V/mV</td>
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<td>( V_{OUT} = 0.8V to 2.0V )</td>
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<tr>
<td>( VOL )</td>
<td>Output Voltage Logic Low</td>
<td>25, ^\circ C</td>
<td>−0.05</td>
<td>0.15</td>
<td>0.4</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 0 ) mA to 8 mA</td>
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7-18
**DC Electrical Characteristics** $V_S = \pm 15V$ unless otherwise specified — Contd.

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<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<td>$V_{oh}$</td>
<td>Output Voltage Logic High</td>
<td>$V_S = \pm 15V$</td>
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<td>4.0</td>
<td>4.65</td>
<td>I</td>
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<td>$T_{MIN}$, $T_{MAX}$</td>
<td>3.5</td>
<td>4.65</td>
<td>III</td>
<td>V</td>
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<td>$25^\circ C$</td>
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<td>V</td>
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<td>$V_S = \pm 5V$</td>
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<td>III</td>
<td>V</td>
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<td>$V_{odi1}$</td>
<td>$V_{OUT}$ Range, Disabled, $I_{OL} = -1\ mA$</td>
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<td>$25^\circ C$</td>
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<td></td>
<td>$V_S = \pm 5V$</td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>4.65</td>
<td></td>
<td>II</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_S = \pm 5V$</td>
<td>$25^\circ C$</td>
<td>3.5</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>$V_{odi2}$</td>
<td>$V_{OUT}$ Range, Disabled, $I_{OL} = 1\ mA$</td>
<td>$V_S = \pm 5V$ to $\pm 15V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ALL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{inh}$</td>
<td>LE or CS Inputs</td>
<td>Logic High Input Voltage</td>
<td>$25^\circ C$</td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>2.2</td>
<td></td>
<td></td>
<td>III</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{inl}$</td>
<td>LE or CS Inputs</td>
<td>Logic Low Input Voltage</td>
<td>$25^\circ C$</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>III</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{in}$</td>
<td>LE or CS Inputs</td>
<td>Logic Input Current</td>
<td>$V_{IN} = 0V$ to $5V$</td>
<td>$25^\circ C$</td>
<td>$\pm 200$</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>$\pm 300$</td>
<td></td>
<td></td>
<td>III</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{s+ en}$</td>
<td>Positive Supply Current Enabled</td>
<td></td>
<td>$25^\circ C$</td>
<td>8.4</td>
<td>12</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>13</td>
<td></td>
<td></td>
<td>III</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{s+ dis}$</td>
<td>Positive Supply Current Disabled</td>
<td></td>
<td>$25^\circ C$</td>
<td>4.7</td>
<td>6</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>7</td>
<td></td>
<td></td>
<td>III</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{s- en}$</td>
<td>Negative Supply Current Enabled</td>
<td></td>
<td>$25^\circ C$</td>
<td>13.0</td>
<td>17</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>18</td>
<td></td>
<td></td>
<td>III</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{s- dis}$</td>
<td>Negative Supply Current Disabled</td>
<td></td>
<td>$25^\circ C$</td>
<td>5.0</td>
<td>6.5</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>$T_{MIN}$, $T_{MAX}$</td>
<td>6.5</td>
<td></td>
<td></td>
<td>III</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
## AC Electrical Characteristics

\( V_S = \pm 15V, T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{pd} )</td>
<td>Propagation Delay, 5 mV Overdrive</td>
<td>20</td>
<td>40</td>
<td></td>
<td>III</td>
<td>ns</td>
</tr>
<tr>
<td>( T_s )</td>
<td>Setup Time</td>
<td>6</td>
<td>12</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( T_h )</td>
<td>Hold Time</td>
<td>-2</td>
<td>0</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{un} )</td>
<td>Unlatch Time</td>
<td>23</td>
<td>40</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{mpw} )</td>
<td>Minimum Clock Pulse Width</td>
<td>12</td>
<td></td>
<td></td>
<td>V</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{en} )</td>
<td>Output 3-State Enable Delay</td>
<td>40</td>
<td>70</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{ds} )</td>
<td>Output 3-State Disable Delay</td>
<td>150</td>
<td>300</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: \( V_{OUT} = 1.4V \).
Note 2: \( V_{CM} = 12V \) to \(-12V\).
Note 3: \( V_S = \pm 5V \) to \( \pm 15V \).
Note 4: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

### Typical AC Performance Curves

#### Propagation Delay (\( - \))
5 mV Overdrive

- **Output Load Capacitance**
- **Temperature**

#### Propagation Delay vs Overdrive

- **Temperature**
- **Output Step**

#### Propagation Delay vs Temperature

- **Overdrive**
- **Enabled/Disabled**

#### Enabled/Disabled Time

- **Temperature**
- **Performance**
Typical AC Performance Curves — Contd.

- **Input Bias Current vs Differential Input Voltage**
  - $I_B$ vs $V_{DIFF}$
  - $T_J = 25^\circ C$

- **Input Bias Current vs Temperature**
  - $I_B$ vs $T_J$

- **Open-Loop Gain vs Frequency**
  - $A_{OL}$ vs $F_{REQUENCY}$

- **CMRR vs Frequency**
  - $CMRR$ vs $F_{REQUENCY}$

- **$V_O/V_I$ Transfer Characteristic**
  - $V_O$ vs $V_{IN}$

- **$V_{OUT}$ vs Temperature**
  - $V_{OUT}$ vs $T_J$

---

2018-4
Typical Performance Curves — Contd.

**$V_{OH}$ vs Positive Supply Voltage**

- $V_{OH}$ DISABLE
- $I_{SINK} = 1\, mA$
- $V_{OH}$ ENABLE
- $I_{SOURCE} = 0\, mA$
- $V_{OH}$ ENABLE
- $I_{SOURCE} = 8\, mA$

**$V_{OL}$ vs Positive Supply Voltage**

- $V_{OL}$ENABLE
- $I_{SINK} = 8\, mA$
- $V_{OL}$DISABLE
- $I_{SINK} = 1\, mA$

**Supply Current vs Temperature**

- $V_S = \pm 15\, VOLTS$
- $I_S$ ENABLED
- $I_S$ DISABLED

**Supply Current vs Supply Voltage**

- $I_S$ ENABLED
- $I_S$ DISABLED

---

8-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature

- $T_J\, MAX = 150^\circ C$
- $Q_C = 50^\circ C/W$
- $Q_J = 95^\circ C/W$

- Infinite Heat Sink
- Free Air
- No Heat Sink

---

2018-5
Application Hints

Device Overview

The EL2018 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Dielectric Isolation Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2018 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.1 μF monolithic ceramic recommended) close to the power supply leads. Good ground plane construction techniques enhance stability, and the lead from pin 1 to ground should be short.

Front End

The EL2018 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V). The transfer function of the EL2018 is linear, and the output is stable when in the linear region.

The large common mode range (±12V minimum) and differential voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.
Application Hints — Contd.

Recovery from Large Overdrives
Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device.

Input Slew Rate
All comparators have input slew rate limitations. The EL2018 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators.

Latch
The EL2018 contains a "transparent" latch. A "transparent" latch acts as an amplifier when the LE input is low and it "latches" and holds the value it had just before the LE transition from low to high.

It is possible to make an oscillation resistant design by putting a short duration "0" on the LE input whenever you wish to make a comparison. This gates the comparator on only for a brief instant, long enough to compare, but not long enough to oscillate. The minimum duration of this pulse is specified by the minimum clock width parameter in the AC electrical tables.

The CS input may be left floating and still produce a guaranteed logic "0" input (active). Floating the LE input will normally produce a logic "0" input also, but operation is not guaranteed.

Proper RF technique suggests that these inputs be grounded or pulled to ground if they are not used.

Output Stage
The output stage of the EL2018 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2018 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature
The EL2018 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in a large ATE system where there may be 1000 comparators, but only 10% are in use at any one time.

Due to the power saving feature and linear output stage, the EL2018 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2018 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

System Design Considerations
The most common problem users have with high speed comparators is oscillations due to output to input feedback. This can be avoided by using a ground plane, proper supply bypassing, and routing the inputs and outputs away from each other. Since the EL2018 has a gain bandwidth product of about 40 GHz, layout and bypassing are important to a successful system design. A unique alternative to the EL2018 is the EL2019, with its edge triggered master/slave flip flop.

Device Functions
The various operating states of the EL2018 are described in the function table on page 7.
Typical Applications

Using the Power Down/3-State Feature

Using the EL2108 in the Transparent Mode (Latch Not Used)

A Wide Input Range Window Comparator

VIN Range +12V to −12V with $V_S = \pm 15V$
**Equivalent Schematic**

![Equivalent Schematic Diagram]

**Burn-In Circuit**

![Burn-In Circuit Diagram]

Pin numbers are for DIP packages.
All packages use the same schematic.
EL2018 Macromodel

* Connections: + input
+ input
- input
+ V
- V
LE
CS
output

.subckt M2018 2 3 8 4 6 5 7

* Input Stage
i1 8 10 700μA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200μA
i3 12 4 200μA

* 2nd Stage & Flip Flop
i4 8 24 700μA
i4 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp

* Output Stage
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qn 2
r8 21 7 60
r7 20 19 4K
q17 19 16 26 qn 5
q18 0 15 26 qn 5
q22 20 20 30 qn 5
EL2018 Macromodel — Contd.

q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp

* Power Supply Current
*
ips 8 4 4mA
*

* Models
*
.model qn npn (is = 2e-15 bf = 400 tf = 0.05nS cje = 0.3pF cjc = 0.2pF ccs = 0.2pF)
.model qp pnp (is = 0.6e-15 bf = 60 tf = 0.3nS cje = 0.5pF cjc = 0.5pF ccs = 0.4pF)
.model ds d(is = 2e-12 tt = 0.05nS eg = 0.62V vj = 0.58)
.model sw vswitch (von = 0.4V voff = 2.5V)
.ends
Features
- Comparator cannot oscillate
- Fast response—5 ns data to clock setup, 20 ns clock to output
- Wide input differential voltage range—24V on ±15V supplies
- Wide input common mode voltage range—±12V
- Precision input stage—$V_{OS} = 1.5$ mV
- Low input bias current—100 nA
- Low input offset current—30 nA
- ±4.5V to ±18V supplies
- 3 State TTL compatible output
- No supply current glitch during switching
- 103 dB voltage gain (Low input uncertainty $\approx 30 \mu$V)
- 50% power reduction in shutdown mode
- Input and flip-flop remain active in shutdown mode

General Description
The EL2019 offers a new feature previously unavailable in a comparator before—a master/slash edge triggered flip-flop. The comparator output will only change output state after a positive going clock edge is applied. Thus the output can't feed back to the input and cause oscillation. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end ensures speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate current glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and master slave flip-flop remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see QRA1: Elantec's Processing-Monolithic Products.

Ordering Information
- Part No. Temp. Range Pkg. Outline #
  - EL2019CN -40°C to +85°C P-DIP MDP0006

Connection Diagrams
**Absolute Maximum Ratings** \((T_A = 25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_S)</td>
<td>Supply Voltage</td>
<td>(±)18V</td>
<td>(I_{OP}) Peak Output Current</td>
<td>50 mA</td>
<td></td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Input Voltage</td>
<td>(+V_S) to (-V_S)</td>
<td>(I_O) Continuous Output Current</td>
<td>25 mA</td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{IN})</td>
<td>Differential Input Voltage</td>
<td>Limited only by Power Supplies</td>
<td>(T_A) Operating Temperature Range</td>
<td>(-40°C) to (+85°C)</td>
<td></td>
</tr>
<tr>
<td>(I_{IN})</td>
<td>Input Current (Pins 1, 2 or 3)</td>
<td>(±10) mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{INS})</td>
<td>Input Current (Pins 5 or 6)</td>
<td>(±5) mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(P_D)</td>
<td>Maximum Power Dissipation (Note 3 - See Curves)</td>
<td>1.25W</td>
<td></td>
<td></td>
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</tr>
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</table>

**Absolute Maximum Ratings** (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{IN})</td>
<td>Input Current (Pins 1, 2 or 3)</td>
<td>(±10) mA</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>(I_{INS})</td>
<td>Input Current (Pins 5 or 6)</td>
<td>(±5) mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(P_D)</td>
<td>Maximum Power Dissipation (Note 3 - See Curves)</td>
<td>1.25W</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:** All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

**Test Level**

- **I**: 100% production tested and QA sample tested per QA test plan QCX0002.
- **II**: 100% production tested at \(T_A = 25°C\) and QA sample tested at \(T_A = 25°C\), \(T_{MAX}\) and \(T_{MIN}\) per QA test plan QCX0002.
- **III**: QA sample tested per QA test plan QCX0002.
- **IV**: Parameter is guaranteed (but not tested) by Design and Characterization Data.
- **V**: Parameter is typical value at \(T_A = 25°C\) for information purposes only.

**DC Electrical Characteristics** \(V_S = \pm 15V\), unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(V_{CM} = 0V, V_O Transition Point)</td>
<td>(25°C)</td>
<td>Min Typ Max</td>
<td>I mV</td>
</tr>
<tr>
<td>(I_B)</td>
<td>Input Bias Current</td>
<td>(V_{CM} = 0V, Pin 2 or 3)</td>
<td>(25°C)</td>
<td>Min Typ Max</td>
<td>I nA</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input Offset Current</td>
<td>(V_{CM} = 0V)</td>
<td>(25°C)</td>
<td>Min Typ Max</td>
<td>I nA</td>
</tr>
<tr>
<td>(CMRR)</td>
<td>Common Mode Rejection Ratio (Note 1)</td>
<td>(25°C)</td>
<td>75 90</td>
<td>I dB</td>
<td></td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power Supply Rejection Ratio (Note 2)</td>
<td>(25°C)</td>
<td>75 95</td>
<td>I dB</td>
<td></td>
</tr>
<tr>
<td>(V_{CM})</td>
<td>Common Mode Input Range</td>
<td>(25°C)</td>
<td>(±12)</td>
<td>I V</td>
<td></td>
</tr>
<tr>
<td>(V_{Uncer})</td>
<td>Input Uncertainty Range</td>
<td>(25°C)</td>
<td>30</td>
<td>III V</td>
<td></td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Output Voltage Logic Low</td>
<td>(\text{LOL} = 8 \text{ mA and IOL} = 0 \text{ mA})</td>
<td>(25°C)</td>
<td>Min Typ Max</td>
<td>I V</td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>Output Voltage Logic High</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics \( V_S = \pm 15V \), unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{ODIS1} )</td>
<td>( V_{OUT} ) Range, Disabled, ( I_{OL} = -1 ) mA</td>
<td>25°C</td>
<td>4.65</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_S = \pm 15V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_S = \pm 15V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_S = \pm 5V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{ODIS2} )</td>
<td>( V_{OUT} ) Range, Disabled, ( I_{OL} = +1 ) mA</td>
<td>All</td>
<td>-0.3</td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_S = \pm 15V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_S = \pm 5V ) to +15V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{INH} )</td>
<td>Clock or CS Inputs Logic High Input Voltage</td>
<td>25°C</td>
<td>2</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IN} )</td>
<td>Clock or CS Inputs Logic Input Current</td>
<td>25°C</td>
<td>( \pm 200 )</td>
<td>I</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>( V_{IN} = 0V ) and ( V_{IN} = 5V )</td>
<td></td>
<td>( \pm 300 )</td>
<td>III</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{INL} )</td>
<td>Clock or CS Inputs Logic Low Input Voltage</td>
<td>25°C</td>
<td>0.8</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{S+EN} )</td>
<td>Positive Supply Current Enabled</td>
<td>25°C</td>
<td>8.8</td>
<td>13</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{S+DIS} )</td>
<td>Positive Supply Current Disabled</td>
<td>25°C</td>
<td>4.9</td>
<td>6</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{S-EN} )</td>
<td>Negative Supply Current Enabled</td>
<td>25°C</td>
<td>14.5</td>
<td>17</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{S-DIS} )</td>
<td>Negative Supply Current Disabled</td>
<td>25°C</td>
<td>6.4</td>
<td>8.0</td>
<td>I</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics \( V_S = \pm 15V \), \( T_A = 25°C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Limits</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_S )</td>
<td>Setup Time 5 mV Overdrive</td>
<td>12</td>
<td>20</td>
<td>II</td>
</tr>
<tr>
<td>( T_H )</td>
<td>Hold Time</td>
<td>-3</td>
<td>0</td>
<td>IV</td>
</tr>
<tr>
<td>( T_{OP} )</td>
<td>Clock to Output Delay</td>
<td>20</td>
<td>25</td>
<td>IV</td>
</tr>
<tr>
<td>( T_{OPMIN} )</td>
<td>Minimum Clock Width</td>
<td>7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( T_{EN} )</td>
<td>Output 3-State Enable Delay</td>
<td>40</td>
<td>70</td>
<td>IV</td>
</tr>
<tr>
<td>( T_{DIS} )</td>
<td>Output 3-State Disable Delay</td>
<td>150</td>
<td>300</td>
<td>IV</td>
</tr>
</tbody>
</table>

Note 1: \( V_{CM} = +12V \) to \(-12V\).
Note 2: \( V_S = \pm 5V \) to \( \pm 15V \).
Note 3: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.
Typical AC Performance Curves

- **Delay Time vs Input Overdrive**
  - TJ = 25°C, STEP = 100mV
  - CK to output +
  - CK to output -
  - Setup Time

- **Delay Time vs Supply Voltage**
  - CK to output +
  - Setup Time

- **Delay Time vs Temperature**
  - CK to output +
  - CK to output -
  - Setup Time

- **Clock to Output Delay vs Load Capacitor**
  - CK to output +
  - CK to output -

- **Minimum Clock Width vs Temperature**
  - Overdrive 5mV
  - Minimum CK Width

- **Enabled/Disabled Times vs Temperature**
  - TPLZ
  - TPLZ
  - TPHZ
  - TPHZ
Typical AC Performance Curves — Contd.

- **Input Bias Current vs Differential Input Voltage**
  - $T_J = 25^\circ C$
  - $I_{B^+} - I_{B^-}$

- **Input Bias Current vs Temperature**
  - $I_B$
  - $I_{OS}$

- **Input Bias Current vs Common Mode Voltage**
  - $T_J = 25^\circ C$
  - $V_{DIFF} = 0$

- **$V_0/V_1$ Transfer Characteristics**
  - $V_{IN} (100 \mu V/\text{DIV})$
  - (NORMALIZED TO $V_{OS} = 0$)

- **Supply Current vs Supply Voltage**
  - $-I_S$ ENABLED
  - $+I_S$ ENABLED
  - $-I_S$ DISABLED
  - $+I_S$ DISABLED

- **Supply Current vs Temperature**
  - $-I_S$ ENABLED
  - $+I_S$ ENABLED
  - $-I_S$ DISABLED
  - $+I_S$ DISABLED

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Typical AC Performance Curves — Contd.

- **VOUT vs Temperature**
  - VS = ±15V
  - VOH DISABLED
  - VOH ENABLED SOURCING 0mA
  - VOH DISABLED SOURCING 0mA
  - VOH SENDING 8mA
  - VOL SINKING 0mA

- **VOL vs Positive Supply Voltage**
  - VOL ENABLE
  - ISINK = 8mA
  - VOL ENABLE
  - ISINK = 0mA
  - VOL DISABLE
  - ISOURCE = 1mA

- **VOL SINKING**
  - 8mA

- **VOL SINKING**
  - 0mA

- **8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature**
  - TJ MAX = 150°C
  - θJA = 50°C/W
  - θJC = 95°C/W
  - INFINITE HEAT SINK
  - FREE AIR
  - NO HEAT SINK

Temperature (°C)

- Power Dissipation (W)
- POSITIVE SUPPLY VOLTAGE (V)
- TEMPERATURE (°C)
Typical AC Performance Curves — Contd.

- Clock to Output Delay vs Clock Time Constant
- Set-up Time vs Clock Time Constant
- PSRR vs Clock Time Constant
- Hold Time vs Clock Time Constant
- Relative V_{OS} Shift vs Clock Time Constant

Graphs showing performance metrics such as clock to output delay, set-up time, PSRR, hold time, and relative V_{OS} shift.
Timing Diagram

Note: Since the hold time is negative the input is a don't care at the clock time. This ensures that clock noise will not affect the measurement.

Function Table

<table>
<thead>
<tr>
<th>Inputs (Time n-1)</th>
<th>Internal Q (Time n)</th>
<th>Notes</th>
<th>Output (Time n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+ IN - IN CS CLK</td>
<td>+ - H L H L H</td>
<td>Normal Comparator Operation</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>- + L L L L H</td>
<td>With &quot;D&quot; Flip-Flop</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>+ - H H L L H</td>
<td>Normal Comparator Operation</td>
<td>High Z</td>
</tr>
<tr>
<td></td>
<td>- + H H H L H</td>
<td>With &quot;D&quot; Flip-Flop; Power Down Mode</td>
<td>High Z</td>
</tr>
<tr>
<td>X X L H</td>
<td>Qn-1 L H</td>
<td>Data Retained in Flip-Flop</td>
<td>Qn-1</td>
</tr>
<tr>
<td>X X L L</td>
<td>Qn-1 L H</td>
<td>Data Retained in Flip-Flop</td>
<td>Qn-1</td>
</tr>
<tr>
<td>X X L F</td>
<td>Qn-1 L H</td>
<td>Data Retained in Flip-Flop</td>
<td>Qn-1</td>
</tr>
<tr>
<td>X X H H</td>
<td>Qn-1 L H</td>
<td>Data Retained in Flip-Flop, Output Power Down Mode</td>
<td>High Z</td>
</tr>
<tr>
<td>X X H L</td>
<td>Qn-1 L H</td>
<td>Data Retained in Flip-Flop, Output Power Down Mode</td>
<td>High Z</td>
</tr>
<tr>
<td>X X H F</td>
<td>Qn-1 L H</td>
<td>Data Retained in Flip-Flop, Output Power Down Mode</td>
<td>High Z</td>
</tr>
</tbody>
</table>
Application Hints

Device Overview
The EL2019 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. The EL2019 has an internal master/slave flip-flop between the input and output. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Process, which is immune to power sequencing and latch up problems.

Power Supplies
The EL2019 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.01 μF monolithic ceramic recommended) within ¼ inch of the power supply leads. Good ground plane construction techniques improve stability, and the lead from pin 1 to ground should be short.

Front End
The EL2019 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V).

The large common mode range (±12V minimum) and differential voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

Recovery from Large Overdrives
Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device, or the supply voltage be raised to encompass the input signal in the common mode range.

Input Slew Rate
All comparators have input slew rate limitations. The EL2019 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators. This shows up as an increased set-up time.

Master Slave Flip-Flop
The built-in Master/Slave Flip-Flop only allows the output to change when a positive edge is received on the clock input. This feature has some major benefits to the user. First, the device cannot oscillate due to feedback from the output to the inputs. Second, the device must make a decision when it receives a clock input, and the difference between deciding on a "0" or a "1" is limited only by the input circuit noise, both internal and external to the EL2019. With low impedance sources and a good layout this uncertainty can be less than 30 μV/RMS. Since a 30 μV change on the input can cause a 4V change on the output this works out to an effective gain of 103 dB, more than adequate for a 16-bit analog to digital converter.

The hold time of the EL2019 is worst case 0 ns, and typically −3 ns. This means that the analog signal is sampled typically 3 ns before the clock time and, worst case, concurrent with the clock.

The EL2019 is sensitive to a large clock edge rates. More than a 500 V/μs edge rate at the clock input will induce VOS shifts, reduce PSRR, and cause the device to operate incorrectly at low temperatures and low supply voltages. A good method to control the clock edge rate is to place a resistor in series and a capacitor to ground in parallel with the clock input. Generally, any time constant 10 ns or greater will suffice.

Elantec tests the EL2019 with a nominal 20 ns time constant, using a series 330Ω resistor and 61 pF of capacitance to ground (including strays). All clocks are generated by Schottky TTL and have a 0.25V to 3.5V swing.
Application Hints — Contd.

Output Stage
The output stage of the EL2019 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2019 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature
The EL2019 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in large ATE systems where there may be 1000 comparators, but only 10% are in use at any one time.

The EL2019 will work properly with the chip select input (pin 5) floating, however, good R.F. technique would be to ground this input if it is not used.

Due to the power saving feature and linear output stage, the EL2019 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2019 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

Typical Applications
A Wide Input Range Window Comparator

The EL2019 makes an excellent comparator in most analog to digital converters, due to its high gain and fast response. Most 2504 based A to D designs can be modified to use the EL2019 simply by using an inverted clock to the EL2019 as shown below. This results in improved performance due to less jitter of the transition voltages.
Burn-In Circuit

Pin numbers are for DIP packages. All packages use the same schematic.

Equivalent Schematic
EL2019 Macromodel

* Connections: + input
  * | -input
  * | + V
  * | - V
  * | Cpin
  * | CS
  * | output

.subckt M2019 2 3 8 4 6 5 7

* Input Stage
i1 8 10 700μA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200μA
i3 12 4 200μA

* 2nd Stage & Flip Flop
i4 8 24 700μA
i5 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp
i5 8 40 500μA
q11 41 17 40 qp
q12 42 6 40 qp
q13 43 16 41 qp
q14 44 15 41 qp
q15 44 43 42 qp
q16 43 44 42 qp
r5 43 4 1K
r6 44 4 1K

* Output Stage
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
EL2019 Macromodel — Contd.

s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qp 2
r8 21 7 60
r7 20 19 4K
q17 19 44 26 qn 5
q18 0 43 26 qn 5
q22 20 20 30 qn 5
q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp
*
* Power Supply Current
*
ips 8 4.4mA
*
* Models
*
.model qn npn (is = 2e-15 bf = 400 tf = 0.05nS cje = 0.3pF cjc = 0.2pF ccs = 0.2pF)
.model qp pnp (is = 0.6e-15 bf = 60 tf = 0.3nS cje = 0.5pF cjc = 0.5pF ccs = 0.4pF)
.model ds d(is = 2e-12 tt = 0.05nS eg = 0.62V vj = 0.58)
.model sw vswitch (von = 0.4V voff = 2.5V)
.ends
EL2021C
Monolithic Pin Driver

Features
• Wide range of programmable analog output levels
• 0.5 Ampere output drive with external transistors
• Programmable Slew Rate
• Low overshoot with large capacitive loads-stable with 500 pF
• 3-state output
• Power-down capability
• Wide supply range
• Overcurrent sense

Applications
• Loaded circuit board testers
• Digital testers
• Programmable 4-quadrant power supplies

Ordering Information
Part No. Temp. Range Package Outline#
EL2021CJ 0°C to +75°C CerDIP MDP0031

General Description
The EL2021 is designed to drive programmed voltages into difficult loads. It has the required circuitry to be used as the pin driver electronics in board test systems. Capable of overpowering logic outputs, the part can accurately drive independently set high and low levels with programmed Slew Rates into reactive loads. It can also be placed into high impedance to monitor the load without having to disconnect. Previous board testers had multiplexing schemes to reduce the number of pin drivers required. With the small size and power consumption of the monolithic EL2021, a driver per node with little or no multiplexing becomes practical. Since only a few pins of “bed-of-nails” board testers need be active at any given time, the power-down feature saves substantial power in large systems.

Block Diagram

Truth Table

<table>
<thead>
<tr>
<th>E</th>
<th>OE</th>
<th>Data</th>
<th>VOUT</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>VCL</td>
<td>Active</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>VCH</td>
<td>Active</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>High-Z</td>
<td>Third State</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Undefined</td>
<td>Power-down</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings \((T_A = 25\, ^\circ C)\)

\[
\begin{array}{|l|l|l|}
\hline
V+ & Supply Voltage & -0.3V \text{ to } +16V \\
V- & Supply Voltage & 0.03V \text{ to } -16V \\
B+, B- & Supply Voltages & V- \text{ to } V+ \\
Sense+ & Input Voltages & \left(-2V + B+\right) \text{ to } \left(0.3V + B+\right) \\
Sense- & Input Voltages & \left(-0.3V + B-\right) \text{ to } \left(2V + B-\right) \\
E, VSR, & & \\
OE, Data & Input Voltages & \left(-0.3 \text{ to } +6V\right) \\
V_{CH}, V_{CL} & Input Voltages & B- \text{ to } B+ \text{ and } V- \text{ to } V+ \\
\hline
\end{array}
\]

Output Current \(-10 \text{ mA to } +10 \text{ mA}\)

Output Currents \(-45 \text{ mA to } +45 \text{ mA}\)

 Junction Temperature \(150\, ^\circ C\)

Operating Ambient \(0\, ^\circ C \text{ to } 75\, ^\circ C\)

Storage Temperature \(-65\, ^\circ C \text{ to } +150\, ^\circ C\)

Power Dissipation \((T_A = 25\, ^\circ C)\) \(1.8W\)

DC Electrical Characteristics \((T_A = 25\, ^\circ C, V+ = 15, V- = -10V, B+ = V_{CH} + 3.6V, B- = V_{CL} - 3.6V, \text{ No Load. Data and OE levels are: } L = 2.0V \text{ and } H = 3.0V \text{ (CMOS thresholds). } E \text{ levels are: } L = 1.5V \text{ and } H = 3.5V. \text{ All tests done using 2N2222 and 2N2907 output transistors with Beta}>40 \text{ at } I_C = 400 \text{ mA and Beta}>27 \text{ at } I_C = 500 \text{ mA and } V_{CE} = 3.1V. OE \text{ and } E \text{ low.})\\

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IS</td>
<td>V+, -Supply Currents</td>
<td>(V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = H or L)</td>
<td>15</td>
<td>25</td>
<td>30</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{CH} = 11V, V_{CL} = -6V, VSR = 5V, Data = H or L)</td>
<td>21</td>
<td>33</td>
<td>45</td>
<td>IV</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{CH} = -6V, V_{CL} = 11V, VSR = 2.5V, Data = H or L)</td>
<td>15</td>
<td>25</td>
<td>30</td>
<td>IV</td>
<td>mA</td>
</tr>
<tr>
<td>IS, disabled</td>
<td>V+, -Supply Currents</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, Data = H or L, E = H)</td>
<td>0</td>
<td>0.5</td>
<td>2.5</td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>IVCH</td>
<td>VCH Input Current</td>
<td>(V_{CH} = -1V \text{ to } +7.5V, VCL = 0V, VSR = 5V, Data = H or L)</td>
<td>-20</td>
<td>5</td>
<td>20</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>IVCL</td>
<td>VCL Input Current</td>
<td>(V_{CL} = -3.5V \text{ to } +3.5V, VCH = 0V, VSR = 5V, Data = H or L)</td>
<td>-20</td>
<td>-5</td>
<td>20</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>IData</td>
<td>Data Input Current</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0 or 5V)</td>
<td>-50</td>
<td>5</td>
<td>50</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>IOE</td>
<td>OE Input Current</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, OE = 0V or 5V)</td>
<td>-20</td>
<td>5</td>
<td>20</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>IE</td>
<td>E Input Current</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, E = 0V or 5V)</td>
<td>-20</td>
<td>2</td>
<td>20</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>IVSR</td>
<td>VSR Input Current</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 0V or 5V)</td>
<td>-20</td>
<td>2</td>
<td>20</td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(\pm I_{sense})</td>
<td>Sense Input Currents</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0V or 5V)</td>
<td>-20</td>
<td>5</td>
<td>20</td>
<td>IV</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_B+, I_B-)</td>
<td>B+, B- Input Currents</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 5V)</td>
<td>-20</td>
<td>5</td>
<td>20</td>
<td>IV</td>
<td>(\mu A)</td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 System. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

Test Level Test Procedure
I 100% production tested and QA sample tested per QA test plan QCX0002.
II 100% production tested at \(T_A = 25\, ^\circ C\) and QA sample tested at \(T_A = 25\, ^\circ C\), \(T_{MAX}\) and \(T_{MIN}\) per QA test plan QCX0002.
III QA sample tested per QA test plan QCX0002.
IV Parameter is guaranteed (but not tested) by Design and Characterization Data.
V Parameter is typical value at \(T_A = 25\, ^\circ C\) for information purposes only.
### DC Electrical Characteristics

**TA = 25°C, V+ = 15, V− = −10, B+ = VCH, B− = VCL, No Load. Data and OE levels are: L = 2.0V and H = 3.0V.**

#### DC Electrical Characteristics Table

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VO</td>
<td>Output Voltage</td>
<td>(V_+ = 14.5V, V_- = -9.5V)</td>
<td>-50</td>
<td>50</td>
<td>1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = L,)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Current = -100 mA, 0 mA, or +100 mA</td>
<td>-300</td>
<td>300</td>
<td>1</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Current = -500 mA or +500 mA</td>
<td>-600</td>
<td>600</td>
<td>1</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = H,)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Current = -100 mA, 0 mA, or +100 mA</td>
<td>4.95</td>
<td>5.05</td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Current = -400 mA or +400 mA</td>
<td>4.7</td>
<td>5.3</td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Current = -500 mA or +500 mA</td>
<td>4.4</td>
<td>5.6</td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{CH} = 11V, V_{CL} = 0V, VSR = 1V, I_{OUT} = 0, Data = L,)</td>
<td>-6.1</td>
<td>-5.9</td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{CH} = 11V, V_{CL} = 0V, VSR = 1V, I_{OUT} = 0, Data = H,)</td>
<td>10.9</td>
<td>11.1</td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{sense}+</td>
<td>+ Sense Threshold</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, R_{sense} = 1\Omega, Data = H,)</td>
<td>400</td>
<td>450</td>
<td>600</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>I_{sense}−</td>
<td>− Sense Threshold</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, R_{sense} = 1\Omega, Data = L,)</td>
<td>-400</td>
<td>-450</td>
<td>-600</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>VO, sense</td>
<td>Sense Out Levels</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, Data L or H,)</td>
<td>0</td>
<td>0.6</td>
<td>1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Current = -350 mA or +350 mA</td>
<td>3.5</td>
<td>5.0</td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{OUT, TRI}</td>
<td>High-Impedance Output Leakage</td>
<td>(V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, Data = L, OE = H,)</td>
<td>-100</td>
<td>5</td>
<td>100</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>Output Voltage = -2.5V or +7.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

**DC test conditions apply except where noted. For AC tests, \(R_L = 1k, C_L = 200\ pF. Delay times are measured from OE or Data crossing 2.5V, \(V_{CH} = 5V, V_{CL} = 0.\)**

#### AC Electrical Characteristics Table

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR +</td>
<td>+ Slew Rate</td>
<td>Data L to H, Output from 0.5V to 4.5V, VSR = 1V</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>1</td>
<td>V/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VSR = 3V</td>
<td>150</td>
<td>240</td>
<td>360</td>
<td>1</td>
<td>V/μs</td>
</tr>
<tr>
<td>SR −</td>
<td>− Slew Rate</td>
<td>Data H to L, Output from 4.5V to 0.5V, VSR = 1V</td>
<td>-80</td>
<td>-100</td>
<td>-120</td>
<td>1</td>
<td>V/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VSR = 3V</td>
<td>-150</td>
<td>-240</td>
<td>-360</td>
<td>1</td>
<td>V/μs</td>
</tr>
<tr>
<td>SRSYM</td>
<td>Slew Rate Symmetry</td>
<td>(\frac{(SR +) - (SR−)}{(SR +) + (SR−)})</td>
<td>-10</td>
<td>10</td>
<td>1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VSR = 1V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VSR = 2V</td>
<td>-20</td>
<td>20</td>
<td>1</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tpd</td>
<td>Propagation Delay</td>
<td>Data L to H, Output to 0.2V, VSR = 2.5V</td>
<td>6.5</td>
<td>9</td>
<td>11.5</td>
<td>1</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Data H to L, Output to 4.8V, VSR = 2.5V</td>
<td>6.5</td>
<td>9</td>
<td>11.5</td>
<td>1</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Ts</td>
<td>Settling Time</td>
<td>VSR = 5V, Data L to H, Output 4.5V to 5V ± 0.2V</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>1</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>VSR = 5V, Data H to L, Output 0.5V to ± 0.2V</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>1</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS</td>
<td>Overshoot</td>
<td>VSR = 1V, Data L to H or H to L</td>
<td>-300</td>
<td>300</td>
<td>300</td>
<td>1</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>VSR = 1V, OE H to L, Data = L, R_L to 5V</td>
<td>-300</td>
<td>300</td>
<td>300</td>
<td>1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VSR = 1V, OE H to L, Data = H, R_L to 0V</td>
<td>-300</td>
<td>300</td>
<td>300</td>
<td>1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Tpda</td>
<td>Propagation Delay, High-Z to Active</td>
<td>VSR = 2.5V, OE H to L, C_L = 50 pF</td>
<td>50</td>
<td>I</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>R_L to 5V, Data = L, Output to 3.5V</td>
<td>50</td>
<td>I</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>R_L to 0V, Data = H, Output to 1.5V</td>
<td>50</td>
<td>I</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tpdh</td>
<td>Propagation Delay, Active to High-Z</td>
<td>VSR = 2.5V, OE L to H, C_L = 50 pF</td>
<td>50</td>
<td>I</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data = L, R_L to 5V, Output to 0.5V</td>
<td>50</td>
<td>I</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data = H, R_L to 0V, Output to 4.5V</td>
<td>50</td>
<td>I</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Pin Description Table

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>System ground.</td>
</tr>
<tr>
<td>2</td>
<td>E</td>
<td>Enable control input. A logic low allows normal operation; a logic high puts the device into power down mode. No output levels are defined in powerdown nor does the output behave as a high impedance.</td>
</tr>
<tr>
<td>3</td>
<td>( \overline{\text{OE}} )</td>
<td>Output Enable input. A logic low sets the output to low-impedance driver mode; a logic high places the output into a high-impedance state.</td>
</tr>
<tr>
<td>4</td>
<td>( V_{\text{CL}} )</td>
<td>Lower analog control input. When ( \text{Data} = \overline{\text{OE}} = \overline{E} = L ), the ( V_{\text{CL}} ) level is output as ( V_{\text{OUT}} ) (assuming ( V_{\text{CL}} &lt; V_{\text{CH}} )).</td>
</tr>
<tr>
<td>5</td>
<td>( B^- )</td>
<td>System power supply. The EL2021 uses this pin as a negative output current monitor connection. Little current is drawn from this pin, transient or static.</td>
</tr>
<tr>
<td>6</td>
<td>( I_{\text{sense}}^- )</td>
<td>Negative output current monitor input.</td>
</tr>
<tr>
<td>7</td>
<td>( V^- )</td>
<td>Negative power supply. Because all negative output drive currents come from this pin (as much as 60 mA transiently), good bypassing is essential.</td>
</tr>
<tr>
<td>8</td>
<td>( \text{Drive}^- )</td>
<td>Output to external npn transistor base.</td>
</tr>
<tr>
<td>9</td>
<td>( V_{OUT} )</td>
<td>High-current input and output, depending on ( \overline{\text{OE}} ).</td>
</tr>
<tr>
<td>10</td>
<td>( \text{Drive}^+ )</td>
<td>Output to external npn transistor base.</td>
</tr>
<tr>
<td>11</td>
<td>Sense Out</td>
<td>Logic output which signals that a high + or ( - ) output current is flowing.</td>
</tr>
<tr>
<td>12</td>
<td>( V^+ )</td>
<td>Positive power supply. Like ( V^- ), it should be well bypassed.</td>
</tr>
<tr>
<td>13</td>
<td>( I_{\text{sense}}^+ )</td>
<td>Positive output current monitor input.</td>
</tr>
<tr>
<td>14</td>
<td>( B^+ )</td>
<td>System power supply, similar to ( B^- ).</td>
</tr>
<tr>
<td>15</td>
<td>( V_{\text{CH}} )</td>
<td>Higher analog control input. When ( \text{Data} = H ) and ( \overline{\text{OE}} = \overline{E} = L ), the ( V_{\text{CH}} ) level is output as ( V_{\text{OUT}} ) (assuming ( V_{\text{CH}} &gt; V_{\text{CL}} )).</td>
</tr>
<tr>
<td>16</td>
<td>VSR</td>
<td>Slew rate control input. A 1V level on this pin causes the output to slew at 100 V/( \mu )s, 0.5V causes a slew rate of 50 V/( \mu )s, etc.</td>
</tr>
<tr>
<td>17</td>
<td>Data</td>
<td>Output level control input. This pin digitally selects ( V_{\text{CL}} ) or ( V_{\text{CH}} ) as the output voltage when ( \overline{\text{OE}} = \overline{E} = L ).</td>
</tr>
<tr>
<td>18</td>
<td>N/C</td>
<td>Not Connected.</td>
</tr>
</tbody>
</table>
Typical Performance Curves

- **Family of output waveshapes. ECL, TTL, CMOS, HCMOS with CI = 50 pF, VSR = 1V.**
- **Family of output waveshapes. ECL, TTL, CMOS, HCMOS with CI = 200 pF, VSR = 1V.**
- **Family of output waveshapes with 5 MHz data rate. CI = 50 pF, VSR = 4V.**
- **Family of output waveshapes from active H, L to high-impedance H, L.**
- **Family of output waveshapes from high-impedance H, L to active H, L.**
- **Family of + output edges, 0V to 5V for VSR = 0.5V, 1V, 2V, 3V, 5V.**
- **Family of – output edges, 5V to 0V or VSR = 0.5V, 1V, 2V, 3V, 5V.**
Typical Performance Curves — Contd.

- Overshoot vs VSR
- Slew Rate vs VSR
- VOUT vs Load Current
- Supply Current vs Supply Voltage
- Tri-State Leakage vs Output Voltage
- Supply Current vs VSR
- Power Dissipation vs Temperature
Applications Information

Output Stage

To meet the requirements of low output impedance, wide bandwidth, and large capacitive load driving capability, the EL2021 has a fairly exotic output stage. Figure 1 shows a simplified schematic of the circuit, only applicable in normal, low impedance mode. External transistors are used to handle the large load currents and peak power dissipations. Since there is no need for good AC crossover distortion performance in a pin driver, the output transistors are operated class C. That is, for small output currents, neither output transistor will conduct bias current, and when load currents do flow, one of the devices is off. This is accomplished by biasing the output transistors from Schottky diodes D1 and D2. In operation, the diode forward voltage is about 0.4V, whereas the "on" output transistor will have a V_{BE} of 0.6V. This leaves only 0.2V across the "off" transistor's base-emitter junction, not nearly enough to cause bias currents to flow in it. Schottky diodes have a temperature drift similar to silicon transistors, so the class C bias maintains over temperature. One caution is that the diodes are in the IC package and are thermally separate from the transistors, so there can exist temperature differences between packages that can cause thermal runaway. Runaway is avoided as long as the external transistors are not hotter than the EL2021 package by more than 80°C. The only way runaway has been induced as of this writing is to use “freeze spray” on the IC package while the output transistors are very hot.

This circuit allows the external transistors to run from B+ and B− supplies that are of less voltage than V+ and V− to conserve power. Reducing B± supplies also reduces dissipations in the output devices themselves. B+ is typically made K volts more than V_{CH} and B− made K volts more negative than V_{CL}. Ideally K is made as small as possible to minimize output transistor dissipation, but two factors limit how small K can be. These factors are both related to the fact that transistors have two collector resistance numbers: "hard" and "soft" saturation resistance. As a transistor begins to saturate at high collector currents and small collector-emitter voltages, minority carriers begin to be generated from the base-collector junction. These carriers act as more collector dopant and actually reduce effective collector resistance. At conditions of heavy saturation, the collector is flooded with minority carriers and exhibits minimum collector resistance. In this way, small geometry transistors like the 2N2222 and 2N2907 devices have excellent collector-emitter voltage drops at high currents, but are actually still in heavy saturation for 1V-2V drops. This “soft” saturation shows up as reduced beta at high currents and moderate V_{CE}’s as well as very poor AC performance. A transistor may exhibit an f_t of only 2 MHz in soft saturation when, like the 2N2222, it gives 300 MHz in non-saturated mode. The EL2021 requires the output transistors to have an f_t of at least 200 MHz to prevent degradation in overshoot, slew rate into heavy loads, and tolerance of heavy output capacitance. With a K of 3.2V and 1Ω collector resistors, almost all 2N2222 and 2N2907 devices perform well, but we have obtained devices from some vendors where the beta does indeed fall prematurely at reduced V_{CE} and high currents. It is important to characterize the external devices for the service that the EL2021 will be expected to provide.

The output stage of the EL2021 does not ring appreciably into a capacitive load in quiescent conditions, but it does ring while it slews. This is an unusual characteristic, but the output slews monotonically and the slew “ripple” does not cause problems in use. The slew ripple does cause a similar “ripple” in the overshoot-vs-VSR characteristic: the overshoot may decrease for slightly increasing VSR, then increase again for larger VSR’s again. The overshoot-vs-VSR graphs...
Applications Information — Contd. presented in this data sheet thus reflect the range of overshoot rather than one particular device’s wavy curve.

The typical 2N2222 and 2N2907 will deliver 750 mA into a short-circuit. This puts four watts of dissipation into the 2N2222 for \( V_{\text{CH}} = 5 \) V. The npn can dissipate this power for a few tenths of a second as long as a metal-base TO-39 package is used. The small or non-metal-based packages have short thermal time constants and high thermal resistances, so they should withstand shorts for only a few milliseconds. The Sense Out signal should be used to control OE or reduce \( V_{\text{CH}} \) and \( V_{\text{CL}} \) to relieve the output devices from overcurrent conditions.

Transistors such as the MJE200 and MJE210 have very much improved collector resistances and high-current beta compared to the 2N2222 and 2N2907. Their \( f_t \)'s are almost as good and sustain at higher currents, and high-current output accuracy will improve. They allow a K of 2V to reduce dissipations further, but short-circuit currents will be as much as two amperes! The geometries of these transistors are larger, and the added transistor capacitances will slow the maximum \( Slew \) Rates that the EL2021 can provide.

If transistors with \( f_t \)'s less than 200 MHz are used, the EL2021 will need to be overcompensated. This is accomplished by connecting equal capacitors from the Drive pins to ground. These capacitors will range from 10 pF to 50 pF. The overcompensation will slow the maximum slew rate, but it will improve the overshoot and reactive load driving capability, and can be considered a useful technique.

Figure 2 shows the equivalent output stage schematic when the circuit is in high-impedance mode \((OE = H)\). The external transistors have their base-emitter junctions each reverse-biased by a Schottky diode drop. A buffer amplifier copies the output voltage to give a bootstrapped bias for the Schottky stack. This scheme guarantees that the external transistors will be off for any output level, and the output leakage current is simply the bias current of the buffer.

The circuit works properly for AC signals up to 500 V/\( \mu \)s. Above this slew rate, the buffer cannot keep up and the external transistors may turn on transiently. Because of the bootstrap action, the output capacitance is less than 10 pF up to 10 MHz of small-signal bandwidth and 300 V/\( \mu \)s slew rate, increasing beyond these values. Adding overcompensation capacitors will degrade the slew rate that the output can withstand before current is drawn.

It is sometime necessary to provide a "snubber" network-a series R and C—to provide a local R.F. impedance for the buffer to look into. 330\( \Omega \) and 56 pF should serve. Also, it is well to provide some DC path to ground (47k for instance) to bias the output stage when no actual circuit is connected to the EL2021 in high-impedance mode.

Power Supplies
In typical operation, \( V_+ \) and \( V_- \) can be as much as \( \pm 15 \) V and as little as \( V_{\text{CH}} + 3 \) V and \( V_{\text{CL}} - 3 \) V, respectively. When driving heavy output currents, however, it is wise to have 5V of headroom above \( V_{\text{CH}} \) and below \( V_{\text{CL}} \) to ensure no saturation of devices within the EL2021 and attendant waveshape distortions. Thus, for \( V_{\text{CH}} = 5 \) V and \( V_{\text{CL}} = -2 \) V, minimum operating voltages are +10, −7V. It is very important to bypass the supply terminals with low-inductance
Applications Information — Contd.
capacitors to ground, since the full base drive
currents of the output transistors are derived
from these supplies. Because the pulse currents
can reach 60 mA, the capacitors should be at least
a microfarad; 4.7 μF tantalum are ideal and re-
quire no small bypasses in parallel.

B+ and B− can be any voltage within V+ and
V− and some amount previously discussed
above VCH and below VCL. If VCH or VCL ex-
ceeds B+ or B−, very large internal fault cur-
tents can flow when the EL2021 attempts to
bring an output transistor's base beyond the col-
lector voltage. The bypassing care of the V±
lines apply to the B± lines, as well as the fact
that ampere currents can occur. Large (100 μF–
500 μF) capacitors should be used to bypass per-
haps every tenth EL2021.

The VCH, VCL, Data and OE lines should be
driven locally so as to not pick up magnetic inter-
ference from the output. The inductance of inter-
connects to these lines can allow coupling to
cause waveshape anomalies or even oscillations.
If long lines are unavoidable, local 1k resistors or
50 pF–100 pF capacitors to ground can also serve
the purpose.

Data Pin
The slew rate of the input to the Data pin should
be kept less than 1000 V/μs. Some feedthrough
can occur for large Slew Rates which will distort
the output waveshape. A 1k–2k resistor in series
with the data pin will reduce feedthrough.

Current Sense
The output current is sensed by comparing the
voltage dropped across the external shunt resis-
tors to an internal 0.45V reference. The center of
the trip level is adjusted for the particular output
transistor betas listed in the data specifications.
Transistors with less beta at high currents will
cause the sense comparators to trip at slightly
higher output currents. The 1Ω shunt resistors
should be non-inductive. The family of wire-
wound resistors called "non-inductive" are too in-
ductive for these shunts.

The response of the Sense Out can be thought of
as slow attack and fast decay. A continuous over-
current condition must last for at least 2 μs be-
fore Sense Out will go high, but will clear to low
only about 200 ns after the overcurrent is with-
drawn. This allows transient currents due to
slewling capacitive load not to generate a flag. On
the other hand, the output transistors will not be
damaged with only a 2 μs system reaction time
to a short-circuit.

Construction Practices
The major cautions in connecting to the EL2021
involve magnetic rather than capacitive parasitic
concerns. The circuits can output as much as
100 A/μs. Even with normal Slew Rates and moder-
lately large capacitive loads, the dI/dT can
cause magnetic fields in harmless looking wires
to fill adjacent lines with noise, and sometimes
ringing or even sustained feedback. Thus, rules
for wiring the EL2021 are:

(a) Keep leads short and large. Short wires are
less inductive, as are wires with large surface
area. The large surface area also reduces skin
resistance at high frequencies, important at
high currents (at 100 MHz, current penetrates
only a few microns in metals).

(b) Use a ground plane. Due to inductance and
skin effect, "ground" voltages will be differ-
et only inches apart on a copper ground
plane. Individual wires do not create ground
at high frequencies. The common "star"
ground is a very bad idea for high-current and
high-frequency circuits.

(c) Dress all wires against the ground plane. The
magnetic fields that the wires would have
generated will be intercepted by the ground
plane and absorbed, thus reducing the wire's
effective inductance. The capacitance added
by this method is not important to EL2021
operation.

(d) The external transistors should have short in-
terconnects to the EL2021, the collector
shunt resistors, and the bypass capacitors. As
previously stated, the shunt resistors must
not be wire wound because of their induct-
ance.
Applications Information — Contd.
(e) The bypass capacitors should have low series resistance and inductance, but should not have a high Q. This may seem contradictory, but a 4.7 μF tantalum capacitor seems to work the best. An electrolytic capacitor should be added to help bolster the supply levels in the 0.1 μs–1 μs after a transition. No small capacitors are needed in parallel with the tantalums. The bypasses’ ground returns are best connected to the area of ground inside the package outline to reduce the circulating current path length, if possible.

Typical Applications

Using the EL2021 without External Transistors
By connecting both drive pins to the output pin, the EL2021 can be used as a stand-alone driver, not requiring the external transistors. The EL2021 is good for more than 50 mA in this mode. The output impedance rises to 12Ω, however, and the current sense and high-impedance mode are not available. The ripple seen in slew edges using the external transistors is largely absent from the standalone waveshapes; and overshoot is markedly improved at VSR > 1V, especially with large capacitive loads.
**Features**
- Fast response—7 ns
- Inputs tolerate large overdrives with no speed nor bias current penalties
- Propagation delay is relatively constant with variations of input Slew Rate, overdrive, temperature, and supply voltage
- Output provides proper CMOS or TTL logic levels
- Hysteresis is available on-chip
- Large voltage gain—8000 V/V
- Not oscillation-prone
- Can detect 4 ns glitches
- MIL-STD-883 Rev. C compliant

**Applications**
- Pin receiver for automatic test equipment
- Data communications line receiver
- Frequency counter input
- Pulse squarer

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Package</th>
<th>Outline #</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL2252CN</td>
<td>0°C to +75°C</td>
<td>14-Pin DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL2252CM</td>
<td>0°C to +75°C</td>
<td>20-Lead SOL</td>
<td>MDP0037</td>
</tr>
</tbody>
</table>

**General Description**

The EL2252 dual comparator replaces the traditional input buffer + attenuator + ECL comparator + ECL to TTL translator circuit blocks used in digital equipment. The EL2252 provides a quick 7 ns propagation delay while complying with ±10V inputs. Input accuracy and propagation delay is maintained even with input signal Slew Rates as great as 4000 V/μs. The EL2252 can run on supplies as low as −5.2V and +9V and comply with ECL and CMOS inputs, or use supplies as great as ±18V for much greater input range.

The EL2252 has a /TTL pin which, when grounded, restricts the output $V_{OH}$ to a TTL swing to minimize propagation delay. When left open, the output $V_{OH}$ increases to a valid CMOS level.

The comparators are well behaved and have little tendency to oscillate over a variety of input and output source and load impedances. They do not oscillate even when the inputs are held in the linear range of the device. To improve output stability in the presence of input noise, an internal 60 mV of hysteresis is available by connecting the HYS pin to V−.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1; "Elantec's Processing, Monolithic Integrated Circuits".

**Connection Diagrams**

![Connection Diagrams](image-url)
**Absolute Maximum Ratings** \((T_A = 25^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(25^\circ C)</td>
<td>1</td>
<td>9</td>
<td></td>
<td>I</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{CM+})</td>
<td>Positive Common-Mode Input Range</td>
<td>Full</td>
<td>10</td>
<td>13</td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CM-})</td>
<td>Negative Common-Mode Input Range</td>
<td>Full</td>
<td>-9</td>
<td>-12</td>
<td></td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>Current into (+) IN, (-) IN, HYS or /TTL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DC Electrical Characteristics** \(V_S = \pm 15V; \text{HYS and /TTL grounded}; T_A = 25^\circ C \text{ unless otherwise specified}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>(25^\circ C)</td>
<td>0.2</td>
<td>1</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_B)</td>
<td>Input Bias Current at Null</td>
<td>(25^\circ C)</td>
<td>6</td>
<td>16</td>
<td></td>
<td>I</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input Offset Current</td>
<td>(25^\circ C)</td>
<td>2</td>
<td></td>
<td></td>
<td>III</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(R_{IN, \text{diff}})</td>
<td>Input Differential Resistance</td>
<td>(25^\circ C)</td>
<td>30</td>
<td></td>
<td></td>
<td>V</td>
<td>k\Omega</td>
</tr>
<tr>
<td>(R_{IN, \text{comm}})</td>
<td>Input Common-Mode Resistance</td>
<td>(25^\circ C)</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>M\Omega</td>
</tr>
<tr>
<td>(C_{IN})</td>
<td>Input Capacitance</td>
<td>(25^\circ C)</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
<td>pF</td>
</tr>
</tbody>
</table>

---

**Important Note:**
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore \(T_J = T_C = T_A\).

**Test Level**

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at (T_A = 25^\circ C) and QA sample tested at (T_A = 25^\circ C), (T_{MAX}) and (T_{MIN}) per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at (T_A = 25^\circ C) for information purposes only.</td>
</tr>
</tbody>
</table>
### DC Electrical Characteristics

$V_S = \pm 15V$; HYS and /TTL grounded; $T_A = 25^\circ C$ unless otherwise specified — Contd.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Temp</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio (Note 1)</td>
<td>Full</td>
<td>70</td>
<td>95</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-Supply Rejection Ratio (Note 2)</td>
<td>Full</td>
<td>70</td>
<td>90</td>
<td></td>
<td>II</td>
<td>dB</td>
</tr>
<tr>
<td>$V_{HYS}$</td>
<td>Peak-to-Peak Input Hysteresis with HYS connected to $V^-$</td>
<td>$25^\circ C$</td>
<td></td>
<td>60</td>
<td></td>
<td>V</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output, CMOS Mode</td>
<td>Full</td>
<td>4.0</td>
<td>4.6</td>
<td>5.1</td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>TTL Mode</td>
<td></td>
<td></td>
<td>2.4</td>
<td>2.7</td>
<td>3.2</td>
<td>II</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output, $I_1 = 0$</td>
<td>Full</td>
<td>-0.2</td>
<td>0.2</td>
<td>0.8</td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_1 = 5$ mA</td>
<td>Full</td>
<td>-0.2</td>
<td>0.4</td>
<td>0.8</td>
<td>II</td>
<td>V</td>
</tr>
<tr>
<td>$I_S^+$</td>
<td>Positive Supply Current</td>
<td>Full</td>
<td>16</td>
<td>19</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S^-$</td>
<td>Negative Supply Current</td>
<td>Full</td>
<td>17</td>
<td>20</td>
<td></td>
<td>II</td>
<td>mA</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

$V_S = \pm 15V$; $C_L = 10$ pF; $T_A = 25^\circ C$; TTL output threshold is 1.4V, CMOS output threshold is 2.5V; unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{PD^{+}}, T_{PD^-}$</td>
<td>Input to Output Propagation Delay, $0 &lt; V_{IN} &lt; 5V$, 500 mV Overdrive, $2000 V/\mu s$ Input Slew Rate, TTL Output Swing</td>
<td>6</td>
<td>9</td>
<td></td>
<td>III</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>CMOS Output Swing</td>
<td>8</td>
<td></td>
<td>V</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{PD^{+}}, T_{PD^-}$</td>
<td>Input to Output Propagation Delay, $-2V &lt; V_{IN} &lt; -1V$, 500 mV Overdrive, 2 ns Input Rise Time, TTL Output Swing</td>
<td>5</td>
<td>9</td>
<td></td>
<td>III</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>CMOS Output Swing</td>
<td>9</td>
<td></td>
<td>V</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{PD}SYM$</td>
<td>Propagation Delay Change between Positive and Negative Input Slopes</td>
<td>1.25</td>
<td></td>
<td>V</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: Two tests are performed with $V_{CM} = 0V$ to $-9V$ and $V_{CM} = 0V$ to $10V$.

Note 2: Two tests are performed with $V^+ = 15V$, $V^-$ changed from $-10V$ to $-15V$; $V^- = -15V$, $V^+$ changed from $10V$ to $15V$. 

7-54
AC Test Circuit

Breadboard - AC Test Circuit

Burn-In Circuit

Breadboard - Burn-In Circuit
**Typical Performance Curves**

1. **Input Bias Current vs Small Overdrives**
   - INVERTING INPUT
   - NON-INVERTING INPUT

2. **Input Bias Current vs Large Overdrives**
   - GROUNDED INPUT
   - DRIVEN INPUT

3. **Bias Current vs Temperature—Inputs Balanced**

4. **Input Hysteresis Voltage vs Temperature**

5. **Input/Output Transfer Function—HYS Open**

6. **Input/Output Transfer Function—HYS Connected to V**

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2252-3

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2252-4
Typical Performance Curves — Contd.

Supply Current vs Supply Voltage

Supply Current vs Temperature ($V_S = \pm 15V$)

Output Delay—0.5V Overdrive

Output with 50 MHz CMOS Input

Output with 50 MHz ECL Input
Typical Performance Curves — Contd.

4 ns TTL Glitch Detection

Gain vs Frequency

Propagation Delay vs Temperature, CMOS Input

Propagation Delay vs Temperature, ECL Input

Propagation Delay vs Overdrive, CMOS Input

Propagation Delay vs Input Slew Rate, CMOS Input
Typical Performance Curves — Contd.

**Propagation Delay vs Power Supply Voltage**

- CHANGE IN PROPAGATION (ns/°C)
  - 5 6 7 8 9 10 11 12 13 14 15
  - POWER SUPPLY (V)

**Load Capacitance**

- CHANGE IN PROPAGATION DELAY (ns)
  - 0 1 2 3 4 5
  - LOAD CAPACITANCE (pF)

**Maximum Power Dissipation**

- 14-Lead Plastic DIP
  - INFINITE HEAT SINK
  - FREE AIR, NO HEAT SINK
  - POWER DISSIPATION (W)
  - TEMPERATURE (°C)

- 20-Lead SOL
  - FREE AIR, NO HEAT SINK, BOARD MOUNT
  - POWER DISSIPATION (W)
  - TEMPERATURE (°C)
Applications Information
The EL2252 is very easy to use and is relatively oscillation-free, but a few items must be attended. The first is that both supplies should be bypassed closely. 1 μF tantalums are very good and no additional smaller capacitors are necessary. The EL2252 requires V− to be at least 5V to preserve AC performance. V+ must be at least 6V for a TTL output swing, 8V for CMOS outputs.

The input voltage range will be referred to the more positive of the two inputs. That is, bringing an input as negative as V− will not cause problems; it's the other input's level that must be considered. The typical input range is +13/−12V when the supplies are ±15V. This range diminishes over temperature and varies with processing; it is wise to set power supplies such that V+ is 5V more positive than the most positive input signal and V− more negative than 6V below the most negative input. ±12V supplies will easily encompass all CMOS and ECL logic inputs. If the input exceeds the device's common-mode input capability, the EL2252 propagation delay and input bias current will increase. Fault currents will occur with inputs a diode below V− or above V+. No damage nor VOS shift will occur even when fault currents within the absolute maximum ratings.
Applications Information — Contd.

One of the few ways in which oscillations can be induced is by connecting a high-Q reactive source impedance to the EL2252 inputs. Such sources are long wires and unterminated coaxial lines. The source impedance should be de-Q’ed. One method is to connect a series resistor to the EL2252 input of around 100Ω value. More resistance will calm the system more effectively, but at the expense of comparator response time. Another method is to install a "snubber" network from comparator input to ground. A snubber is a resistor in series with a small capacitor, around 100Ω and 33 pF. Each physical and electrical environment will require different treatments, although many need none.

The major use of the HYS pin is to suppress noise superimposed on the input signal. By shorting the HYS pin to V− a ±30 mV hysteresis is placed around the VOS of the comparator input. Leaving the pin open, or more appropriately, grounding the HYS pin removes all hysteresis. Connecting a resistor between HYS and V− allows an adjustment of the peak-to-peak hysteresis level. Unfortunately, an external resistor cannot track the internal devices properly, so temperature and unit-to-unit variations of hysteresis are increased. The relationship between the resistor and resulting hysteresis level is not linear, but a 1.5k resistor will approximately halve the nominal value.

The time delay of the EL2252 will increase by about 0.7 ns when using full hysteresis.

The EL2252 is specifically designed to be tolerant of large inputs. It will exhibit very much increased delay times for input overdrives below 100 mV. If very small overdrives must be sensed, the EL2018 or EL2019 comparators would be good choices, although they lose accuracies with signal input Slew Rates above 400 V/μs. The EL2252 keeps its timing accuracy with input Slew Rates between 100 V/μs and 4000 V/μs of input Slew Rate.

The output stage drives tens of pF load capacitances without increased overshoot, but propagation delay increases about 1 ns per 10 pF. The output circuit is not a traditional TTL stage, and using an external pullup resistor will not change the VOH. In general setting the output swing to TTL (by grounding the /TTL pin) will optimize overall propagation delay and ±swing symmetry.
EL2252C Macromodel

* Connections:
  + input
  - input
  +V
  -V
  HYS
  TTL

*subckt M2252 2 3 14 7 4 5 13

* Application Hints:
  
  * Connect pin 4 to ground through 1000 MΩ resistor to inhibit
  * Hysteresis; to invoke Hysteresis, connect pin 4 to V-
  
  * Connect pin 5 to ground to invoke TTL VOH; pin 5 may left open
  * for CMOS VOH
  
  * To facilitate .OP, set it1 = 200, it12 = 200, set node 27 to 13.8V,
  * and node 30 to -12V.

*Input Stage

*  
i1 22 7 1.7mA
r1 14 20 300
r2 14 21 300
q1 20 2 22 qn
q2 21 3 22 qn
q3 20 26 23 qn
q4 21 25 23 qn
q13 25 27 20 qp
q14 26 27 21 qp
v1 14 27 1.2V
r3 23 24 1.4k
d1 24 4 ds
r4 25 33 700
r5 26 33 700
q16 33 33 34 qn
q17 34 34 37 qn
v4 37 7 1.2V

*  
2nd Stage

*  
i2 30 7 3mA
i3 14 28 1.5mA
q7 0 35 28 qp
v2 44 0 1.2V
s1 44 35 5 0 swa
s2 45 35 5 0 swb
rs2 14 5 10k
EL2252C Macromodel — Contd.

v3 45 0 2.5V
q5 0 26 30 qn
d6 28 25 30 qn
d3 0 28 ds
  *
  * Output Stage
  *
i4 14 38 1mA
q8 38 38 39 qn
q9 32 32 39 qp
q10 7 28 32 qp
d11 14 38 40 qn 2
q12 7 28 13 qp 2
d6 40 13 50
c1 28 0 3pF
  *
  * Models
  *
.model qn npn (is = 2e-15 bf = 120 tf = 0.2nS cje = 0.2pF cjc = 0.2pF ccs = 0.2pF)
.model qp npn (is = 0.6e-15 bf = 60 tf = 0.2nS cje = 0.5pF cjc = 0.3pF ccs = 0.2pF)
.model ds d(is = 3e-12 tt = 0.05nS eg = 0.72V vj = 0.58)
.model swa vswitch (von = 0v voff = 2.5V)
.model swb vswitch (von = 2.5 voff = 0V)
.ends
Features
• 3-State output
• 3V and 5V Input compatible
• Clocking speeds up to 10 MHz
• 20 ns Switching/delay time
• 4A Peak drive
• Isolated drains
• Low output impedance—2.5Ω
• Low quiescent current—5 mA
• Wide operating voltage—4.5V–16V

Applications
• Parallel bus line drivers
• EPROM and PROM programming
• Motor controls
• Charge pumps
• Sampling circuits
• Pin drivers

General Description
The EL7134C 3-state driver is particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 4A peak drive capability, makes the EL7134C an excellent choice when driving high speed capacitive lines.

Connection Diagram

Truth Table

<table>
<thead>
<tr>
<th>3-State</th>
<th>Input</th>
<th>P-Out</th>
<th>N-Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>HIGH</td>
<td>Open</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Open</td>
<td>LOW</td>
</tr>
</tbody>
</table>

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Supply (V+ to Gnd)</th>
<th>Operating Junction Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>±0.3 V to +0.3 V above V+</td>
<td>125°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Peak Output Current</th>
<th>SOIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 A</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Storage Temperature Range</th>
<th>PDIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>–65°C to +150°C</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ambient Operating Temperature</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>–40°C to +85°C</td>
<td></td>
</tr>
</tbody>
</table>

Important Note:

All parameters having Min/Max speciﬁcations are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level | Test Procedure
--- | ---
I | 100% production tested and QA sample tested per QA test plan QCX0002.
II | 100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$.
III | $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.
IV | QA sample tested per QA test plan QCX0002.
V | Parameter is guaranteed (but not tested) by Design and Characterization Data.

DC Electrical Characteristics $T_A = 25°C$, $V+ = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td>$V_{IH} = V+$</td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>$V_{IH} = V+$</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td>$V_{IL} = 0V$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>$V_{IL} = 0V$</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{HVS}$</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
</tbody>
</table>

Output

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{OH}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100 mA$</td>
<td>1.5</td>
<td>4</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{OL}$</td>
<td>Pull-Down Resistance</td>
<td>$I_{OUT} = +100 mA$</td>
<td>2</td>
<td>4</td>
<td></td>
<td>I</td>
<td>Ω</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Leakage Current</td>
<td>$V+/GND$</td>
<td>0.2</td>
<td>10</td>
<td></td>
<td>I</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>4.0</td>
<td>4.0</td>
<td></td>
<td>V</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>200</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>Power Supply Current</td>
<td>$V+ =$</td>
<td>1</td>
<td>2.5</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

\[ T_A = 25^\circ C, V = 15V \text{ unless otherwise specified} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_R )</td>
<td>Rise Time</td>
<td>( C_L = 1000 \text{ pF} ) ( C_L = 2000 \text{ pF} )</td>
<td>7.5</td>
<td>10</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Fall Time</td>
<td>( C_L = 1000 \text{ pF} ) ( C_L = 2000 \text{ pF} )</td>
<td>10</td>
<td>13</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{D\text{-ON}} )</td>
<td>Turn-On Delay Time</td>
<td></td>
<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{D\text{-OFF}} )</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

#### Timing Table

- **Input**: 0 V, 2.5 V, 5 V
- **Output**: 10%, 90%

#### Standard Test Configuration

- Inputs: 1, 2, 3, 4, 5, 6
- Output: 7
- Capacitors: 4.7 \( \mu F \), 2000 pF

#### Simplified Schematic

- Inputs: 1, 2
- Outputs: 7 (P-Out), 8 (N-Out)
- '3-State' device

---

7-66
Typical Performance Curve

Max Power/Derating Curves

Switch Threshold vs Supply Voltage

Input Current vs Voltage

Peak Drive vs Supply Voltage

Quiescent Supply C

"ON" Resistance vs Supply Voltage
Typical Performance Curve — Contd.
Typical Performance Curve — Contd.

- Propagation Delay vs Supply Voltage
- Rise/Fall Time vs Temperature
- Delay vs Temperature
Features
- Comparatively low cost
- 3-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5 mA
- Wide operating voltage—4.5V–16V
- Isolated P-channel device
- Separate ground and VL pins

Applications
- Loaded circuit board testers
- Digital testers
- Level shifting below GND
- IGBT drivers
- CCD drivers

General Description
The EL7154C 3-state pin driver is particularly well suited for ATE and level shifting applications. The 4A peak drive capability, makes the EL7154C an excellent choice when driving high speed capacitive lines.

The p-channel MOSFET is completely isolated from the power supply, providing a high degree of flexibility. Pin (7) can be grounded, and the output can be taken from pin (8) when a "source follower" output is desired. Then n-channel MOSFET has an isolated drain, but shares a common bus with pre-drivers and level shifter circuits. This is necessary to ensure that the n-channel device can turn off effectively when VL goes below GND. In some power-FET and IGBT applications, negative drive is desirable to insure effective turn-off. The EL7154 can be used in these applications by returning VL to a moderate negative potential.

Connection Diagram

Nominal Operating Voltage Range

<table>
<thead>
<tr>
<th>Pin</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>VL</td>
<td>-3</td>
<td>0</td>
</tr>
<tr>
<td>VDD-VL</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>VH-VL</td>
<td>2</td>
<td>15</td>
</tr>
<tr>
<td>VDD-VH</td>
<td>-0.5</td>
<td>15</td>
</tr>
<tr>
<td>VDD</td>
<td>5</td>
<td>15</td>
</tr>
</tbody>
</table>

Truth Table

<table>
<thead>
<tr>
<th>3-State</th>
<th>Input</th>
<th>POUT</th>
<th>NOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>HIGH</td>
<td>Open</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Open</td>
<td>LOW</td>
</tr>
</tbody>
</table>

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047, #5,352,578, #5,352,389, #5,351,012, #5,374,898
Absolute Maximum Ratings

Supply (VDD to VL, V+ to VH, VL to GND),

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ to VH</td>
<td>16.5 V</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>VL to GND</td>
<td>0 V</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>Input Pins</td>
<td>-0.3 V below VL to +0.3 V above VDD</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>4 A</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td></td>
</tr>
</tbody>
</table>

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore TJ = TC = TA.

DC Electrical Characteristics

T_A = 25°C, VDD = +12V, VH = +12V, VL = -3V, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>VIH</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>IIH</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>VIH = VDD</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td>VIH</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>IIH</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>VIL = 0V</td>
<td>0.1</td>
<td>10</td>
<td>I</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td>V_HVS</td>
<td>Input Hysteresis</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>Output</td>
<td>R_OH</td>
<td>Pull-Up Resistance</td>
<td>I_OUT = -100 mA</td>
<td>1.5</td>
<td>4</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>R_OL</td>
<td>Pull-Down Resistance</td>
<td>I_OUT = +100 mA</td>
<td>2</td>
<td>4</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>IOUT</td>
<td>Output Leakage Current</td>
<td>VDD/GND</td>
<td>0.2</td>
<td>10</td>
<td>I</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td>IPK</td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>4.0</td>
<td></td>
<td>V</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>IDC</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>200</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
</tbody>
</table>

Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IS</td>
<td>Power Supply Current</td>
<td>Inputs = VDD</td>
<td>1</td>
<td>2.5</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>VS</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td></td>
<td>16</td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>IG</td>
<td>Current to GND (Pin 4)</td>
<td></td>
<td>1</td>
<td></td>
<td>10</td>
<td>I</td>
<td>uA</td>
</tr>
<tr>
<td>IH</td>
<td>Off Leakage at VH</td>
<td>Pin 8 = 0V</td>
<td>1</td>
<td></td>
<td>10</td>
<td>I</td>
<td>uA</td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

$T_A = 25°C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 100$ pF</td>
<td>4</td>
<td>20</td>
<td>25</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 2000$ pF</td>
<td>4</td>
<td>20</td>
<td>25</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-1}$</td>
<td>Turn-Off Delay Time</td>
<td>$C_L = 2000$ pF</td>
<td>20</td>
<td>25</td>
<td>25</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-2}$</td>
<td>Turn-On Delay Time</td>
<td>$C_L = 2000$ pF</td>
<td>10</td>
<td>25</td>
<td>25</td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-1}$</td>
<td>3-State Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-2}$</td>
<td>3-State Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

#### Timing Table

Timing Table

![Timing Table Diagram](image)

#### Standard Test Configuration

![Standard Test Configuration Diagram](image)
Typical Performance Curves

Max Power/Derating Curves

- 8-Lead PDIP
- 8-Lead SO
- $\theta_{JA} = 95^\circ C/W$
- $\theta_{JA} = 175^\circ C/W$
- Max $T_J = 125^\circ C$

Input Current vs Voltage

- $I_N$ vs $V_{IN}$
- 2.500/div (V)
- 10.00
- 2.000
- 0
- $V_+ = 20.0$
- $V_+ = 5.0$

Quiescent Supply Current

- Case:
  - A - All Inputs = 0
  - B - 1 Input = 0
  - C - All Inputs = $V_{DD}$

Peak Drive vs Supply Voltage

- $V$ - Supply
- I-Sink
- N-CHANNEL
- 4.0A
- 2.0A
- 1.0A
- 0
- P-CHANNEL

"ON" Resistance vs Supply Voltage

- Measured at 100 mA
- Pull Down
- Pull Up

Switch Threshold vs Supply Voltage

- Input Voltage
- High Limit = 2.4V
- Low Limit = 0.8V

Supply Voltage

0 5 10 15

Supply Voltage

0 5 10 15

Supply Voltage

0 5 10 15

Supply Voltage

0 5 10 15
Typical Performance Curves — Contd.

**Average Supply Current vs Voltage and Frequency**

- $V_{DD} = +15V$
- $V_{DD} = +10V$
- $V_{DD} = +5V$
- $C_L = 2000 \text{ pF}$

**Rise/Fall Time vs Load**

- $V_{DD} = 10V$

**Typical Applications**

**Pin Driver**

**Adjustable Amplitude Pulse Generator**

- $+15V$
- $0.1 \mu F$
- $1K$
- $0.1 \mu F$
Typical Applications — Contd.

IGBT Driver (with Negative Swing)

PMOS Follower

Resonant Gate Driver
Features
- 3-State output
- 3V and 5V input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Low, matched output impedance—5Ω
- Low quiescent current—2.5 mA
- Wide operating voltage—4.5V–16V

Applications
- Parallel bus line drivers
- EPROM and PROM programming
- Motor controls
- Charge pumps
- Sampling circuits
- Pin drivers
- Bridge circuits

General Description
The EL7232C 3-state drivers are particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 2A peak drive capability, makes the EL7232C an excellent choice when driving high speed capacitive lines, as well. The input circuitry provides level shifting from TTL levels to the supply rails. The EL7232C is available in 8-pin P-DIP and 8-lead SO packages.

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Temp. Range</th>
<th>Pkg.</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL7232CN</td>
<td>-40°C to +85°C</td>
<td>8-Pin P-DIP</td>
<td>MDP0031</td>
</tr>
<tr>
<td>EL7232CS</td>
<td>-40°C to +85°C</td>
<td>8-Pin SO</td>
<td>MDP0027</td>
</tr>
</tbody>
</table>

Truth Table

<table>
<thead>
<tr>
<th>3-State</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Open</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Open</td>
</tr>
</tbody>
</table>

Manufactured under U.S. Patent Nos. 5,334,883, # 5,341,047
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Supply (V+ to Gnd)</th>
<th>16.5V</th>
<th>Operating Junction Temperature</th>
<th>125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pins</td>
<td>-0.3V to +0.3V above V+</td>
<td>Power Dissipation</td>
<td></td>
</tr>
<tr>
<td>Combined Peak Output Current</td>
<td>4A</td>
<td>SOIC</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td>PDIP</td>
<td></td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Important Note:**

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

<table>
<thead>
<tr>
<th>Test Level</th>
<th>Test Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>100% production tested and QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>II</td>
<td>100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$. $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.</td>
</tr>
<tr>
<td>III</td>
<td>QA sample tested per QA test plan QCX0002.</td>
</tr>
<tr>
<td>IV</td>
<td>Parameter is guaranteed (but not tested) by Design and Characterization Data.</td>
</tr>
<tr>
<td>V</td>
<td>Parameter is typical value at $T_A = 25°C$ for information purposes only.</td>
</tr>
</tbody>
</table>

## DC Electrical Characteristics $T_A = 25°C$, $V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Logic &quot;1&quot; Input Current</td>
<td>@V+</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; Input Voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Logic &quot;0&quot; Input Current</td>
<td>@0V</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>I</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{HVS}$</td>
<td>Input Hysteresis</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{OH}$</td>
<td>Pull-Up Resistance</td>
<td>$I_{OUT} = -100$ mA</td>
<td>3</td>
<td>6</td>
<td></td>
<td>I</td>
<td>$\Omega$</td>
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<tr>
<td>$R_{OL}$</td>
<td>Pull-Down Resistance</td>
<td>$I_{OUT} = +100$ mA</td>
<td>4</td>
<td>6</td>
<td></td>
<td>I</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>3-State Output Leakage</td>
<td>$V_{OUT} = V+$</td>
<td>0.2</td>
<td></td>
<td>10</td>
<td>I</td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{OUT} = 0V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>Source/Sink</td>
<td>2.0</td>
<td></td>
<td>2.0</td>
<td>IV</td>
<td>A</td>
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<tr>
<td>$I_{DC}$</td>
<td>Continuous Output Current</td>
<td>Source/Sink</td>
<td>100</td>
<td></td>
<td></td>
<td>I</td>
<td>mA</td>
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<tr>
<td><strong>Power Supply</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{S}$</td>
<td>Power Supply Current</td>
<td>Inputs High</td>
<td>1</td>
<td>2.5</td>
<td></td>
<td>I</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{S}$</td>
<td>Operating Voltage</td>
<td></td>
<td>4.5</td>
<td>16</td>
<td></td>
<td>I</td>
<td>V</td>
</tr>
</tbody>
</table>
AC Electrical Characteristics $T_A = 25^\circ C$, $V = 15V$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Test Level</th>
<th>Units</th>
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<tr>
<td>$t_R$</td>
<td>Rise Time</td>
<td>$C_L = 500 \text{ pF}$ $C_L = 1000 \text{ pF}$</td>
<td>7.5</td>
<td>10</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall Time</td>
<td>$C_L = 500 \text{ pF}$ $C_L = 1000 \text{ pF}$</td>
<td>10</td>
<td>13</td>
<td>20</td>
<td>IV</td>
<td>ns</td>
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<tr>
<td>$t_{D-ON}$</td>
<td>Turn-On Delay Time</td>
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<td>18</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D-OFF}$</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td>20</td>
<td>25</td>
<td></td>
<td>IV</td>
<td>ns</td>
</tr>
</tbody>
</table>

Timing Table

Standard Test Configuration

Simplified Schematic
Typical Performance Curve

Max Power/Derating Curves

- 1.05W @ 8-Lead PDIP
- 670 mW @ 8-Lead SO
- Max T_J = 125°C
- θJA = 95°C/W
- θJA = 175°C/W

Switch Threshold vs Supply Voltage

- High Limit = 2.4V
- Low Limit = 0.8V

Input Current vs Voltage

- V_IN: -5.0 to 20.0 V
- I_IN: -10.0 to 10.0 mA
- Step: 2.500/div

Peak Drive vs Supply Voltage

- V_Supply: 0 to 15 V
- I_Sink: -2.0A to 2.0A
- I_Source: -1.0A to 1.0A

Quiescent Supply Current

CASE:
- A: ALL INPUTS GND
- B: 3 INPUTS GND
- C: 2 INPUTS GND
- D: 1 INPUTS GND
- E: ALL INPUTS V+

"ON" Resistance vs Supply Voltage

- Measured at 100 mA
- Pull Down
- Pull Up
Typical Performance Curve — Contd.

**Average Supply Current vs Voltage and Frequency**

- $V_{DD} = +15V$
- $V_{DD} = +10V$
- $V_{DD} = +5V$
- $C_L = 1000 \text{ pF}$

 FREQUENCY

**Average Supply Current vs Capacitive Load**

- $V_{DD} = 10V$
- No Load
- (Equivalent Internal Capacitance = 470 pF)

 FREQUENCY

**Rise/Fall Time vs Load**

- $V_{DD} = 10V$

 LOAD CAPACITANCE (pF)

**Rise/Fall Time vs Supply Voltage**

- $C_L = 1000 \text{ pF}$

 SUPPLY VOLTAGE
Typical Performance Curve — Contd.

- **Rise/Fall Time vs Temperature**
  - $t_{D1}$
  - $t_{D2}$
  - $C_L = 1000 \, \text{pF}$

- **Propagation Delay vs Supply Voltage**
  - $V_{DD} = 10 \, \text{V}$
  - $C_L = 1000 \, \text{pF}$

- **Propagation Delay vs Temperature**
  - $V_{DD} = 10 \, \text{V}$
  - $C_L = 1000 \, \text{pF}$

---

7232-14  
7232-15  
7232-16
A Low-Noise Variable Gain Control
by Barry Harvey

The EL2082 current-mode variable gain control IC can be connected in a way to minimize circuit noise. In the usual forward configuration, the circuit has an 80 nV/\sqrt{Hz} input noise which is constant with respect to gain adjustment. The circuit to be shown has an effective input noise which reduces as adjusted gain is increased. The circuit is useful in AGC or leveling functions where a relatively constant output amplitude is required for a range of inputs.

Figure 1 shows the schematic of the configuration. The EL2082 provides an output current equal to \( V_{\text{GAIN}}/1\text{V} \) times the input current. The output impedance of the EL2082 is in the megohm range and the input impedance is about 90\,\Omega, and the part behaves as a current conveyor with adjustable gain. In essence, the EL2082 causes \( R_{\text{FV}} \) to behave as a variable feedback resistor, and in parallel with \( R_{\text{FF}} \) controls the gain of the circuit.

With \( V_{\text{GAIN}} = 0 \), the circuit gain is \(-R_{\text{FF}}/R_{\text{IN}}\), and the noise of the EL2082 is gained to zero. In this mode, the circuit gain is maximum and input noise is determined by the op-amp alone. With \( V_{\text{GAIN}} = 1\text{V} \), the circuit gain is \(- (R_{\text{FF}}/R_{\text{FV}})/R_{\text{IN}}\), and EL2082 noise mixes with op-amp noise.

For the maximum value of \( V_{\text{GAIN}} = 2\text{V} \), the EL2082 dominates the feedback signal and gain is minimum while output noise is increased.

The op-amp must be a current-feedback type for the circuit to work. The CMF amplifier's low-input impedance prevents capacitance at the input from causing a feedback pole and drastically limiting potential bandwidth. On the other hand, since the time delay of the EL2082 is inside the \( R_{\text{FV}} \) feedback loop, \( R_{\text{FV}} \) is a rather high value and must be adjusted to prevent excessive peaking or oscillation when \( V_{\text{GAIN}} = 2\text{V}, R_{\text{FF}} \) is set to control the maximum gain when \( V_{\text{GAIN}} = 0 \). For the values shown, the output can swing ±2\,\text{V} for 0.25\% distortion, and the maximum swing is ±4\,\text{V}.

The input noise is successfully reduced by the circuit when small inputs require higher gain, as shown in Figure 2. The constancy of bandwidth and peaking and gain range are the tradeoffs. Here is a table of measured values:

<table>
<thead>
<tr>
<th>( V_{\text{GAIN}} )</th>
<th>( A_v )</th>
<th>( \text{BW, } -3,\text{dB} )</th>
<th>( \text{Peaking} )</th>
<th>( \text{Input Noise} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>9.03</td>
<td>11 MHz</td>
<td>None</td>
<td>8.7 nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>0.5V</td>
<td>5.41</td>
<td>26 MHz</td>
<td>None</td>
<td>19 nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>1.0V</td>
<td>3.91</td>
<td>58 MHz</td>
<td>None</td>
<td>33 nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>1.5V</td>
<td>3.11</td>
<td>75 MHz</td>
<td>2.2 dB</td>
<td>42 nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>2.0V</td>
<td>2.62</td>
<td>80 MHz</td>
<td>5.5 dB</td>
<td>57 nV/\sqrt{Hz}</td>
</tr>
</tbody>
</table>
A Low-Noise Variable Gain Control

Figure 1

El2082

\( V_{\text{IN}} \rightarrow R_{\text{IN}} \)

\( 300\Omega \)

\( V_G \)

\( V_{\text{IN}} \)

\( V_{\text{OUT}} \)

\( R_{\text{FF}} \)

\( 2.7\, \text{k}\Omega \)

\( 2.2\, \text{k}\Omega \)

\( 1\, \text{pF} - 2\, \text{pF} \)

\( V_{\text{OUT}} \rightarrow \)

Figure 2

\( V_{\text{GAIN}} \) (0V to +2V)

\( 0 \) V

\( 0.2 \) V

\( 0.4 \) V

\( 0.6 \) V

\( 0.8 \) V

\( 1.0 \) V

\( 1.2 \) V

\( 1.4 \) V

\( 1.6 \) V

\( 1.8 \) V

\( 2.0 \) V

-3 dB BANDWIDTH (MHz)

GAIN

BANDWIDTH

INPUT NOISE

PEAKING

Figure 2
Thermal Considerations of the SO-8
by Barry Siegel

The world owes Phillips and Signetics a great debt in introducing the SO package. It offers a very small footprint, low cost, reliable, surface mounting package demanded by today's high density systems. However, since the thermal impedance of any package is, to the first order, inversely proportional to its area, the SO-8 imposes severe restrictions on the allowable power dissipation of the package. As pointed out in Reference (1), power dissipation raises the die junction temperature, and system reliability may be degraded. This brief sets forth a practical design method to ascertain what, if any, restrictions have to be placed on operating a linear IC in the SO package.

Analysis

Probably the best place to begin is to establish at what junction temperature a given device will be allowed to operate. Most manufacturers rate their junctions at a maximum of 150°C in plastic packages, but for reasons of reliability, a lower number may be mandated. The datasheet usually stipulates $\theta_{JA}$, the thermal impedance from junction to ambient, and the difference between the maximum junction temperature we will allow and the maximum ambient temperature stipulates the thermal budget that we have or the junction temperature rise:

$$\text{Pt} = \frac{T_{j}^{\text{max}} - T_{A}^{\text{max}}}{\theta_{JA}} \quad (1)$$

where:

- $\text{Pt}$ = Total Power Dissipated by the Device
- $T_{j}^{\text{max}}$ = Maximum Junction Temperature
- $T_{A}^{\text{max}}$ = Maximum Ambient Temperature

Power dissipation is comprised of two parts—$P_{q}$, the power dissipated by the device due simply to its supply current, and $P_{l}$, the power dissipated by the chip as a consequence of driving a load. In general, $P_{q}$ is independent of $P_{l}$ and vice versa, so an analysis can be made of each case and the results simply added together to obtain Pt.

The analysis should start with $P_{q}$ since it is straightforward, and if $T_{j}^{\text{max}}$ is exceeded under quiescent conditions, an alternate strategy is dictated. A word of caution, however, is in order. There are devices such as the EL2001 Unity Gain Buffer that draw a supply current of 1 mA but are capable of driving 100 mA loads. Clearly, in this case, power dissipation will be dominated by $P_{l}$. As a case in point, we might examine the EL2120 100 MHz CFA. Its quiescent supply current is specified as 20 mA. A typical video application is to use ±10V power supplies with 150Ω load driven to 8V peak-to-peak with an ambient temperature of 50°C. Under these conditions, $P_{q}$ is equal to 400 mW, and using the datasheet value of 175°C/W for $\theta_{JA}$, we obtain an average value for $T_{j}$ of 120°C. What this tells us is that in order to keep the junction below 150°C, the junction rise due to driving a load must be under 30°C.
If we assume a steady state (sinusoidal) output voltage of 4V, the power dissipated in the EL2021's output transistor, Pl, would be:

\[ P_l = (V^+ - V_{OUT})(I_{OUT}) \]  \hspace{1cm} (2)

Where:

\[ I_{OUT} = \frac{V_{OUT}}{R_L'} \]

\[ R_L' = R_L \parallel R_F \]

The recommended feedback resistor for the EL2120 is typically 300Ω, and for an inverter, R_F is indeed in parallel with R_L. For our particular case, Pl is equal to 240 mW, and the additional increase in junction temperature is 42°C exceeding our earlier requirement of limiting the load incurred junction rise to less than 30° and putting the junction at an average of 162°C.

In the final analysis, either the supply voltages have to be reduced or the load decreased to maintain the junction temperature below 150°. Our best advice is to approach the problem carefully, do the Pq "spot check" first, and verify the conditions with the vendor's applications department.

References

1. "Reliability and the Electronic Engineer" by Barry Siegel, paper given at the EE Times Analog conference, October, 1991

DC Restored 100 MHz Current Feedback Video Amplifier
by John Lidgey and Chris Toumazou

Summary
The EL2090 is an extremely versatile video amplifier with an integral on-board DC loop amplifier and sample-hold control circuitry. It is the first complete DC-restored monolithic video amplifier subsystem. It uses a current-feedback video amplifier with a nulling sample and hold amplifier specifically designed to stabilize video performance. This application note includes a video signal restorer with some fundamentals about DC restoration. As an application circuit of the EL2090, a x2 gain video amplifier is described together with a full evaluation circuit and double sided pc-board artwork. The EL2090 is a high-speed part, and some useful tips on layout have been included.

Although DC restoration is not a new concept, the high slew-rate, fast settling-time and low phase distortion at high frequencies provided by Elantec's family of monolithic current-feedback amplifiers, make CFAs the most attractive video amplifier choice for this application.

Video Signal Refresher
Figure 1 is a typical composite video signal which has a standard distribution level of 1V peak-to-peak into 75Ω, and comprises several sections. The video signal is the part containing the visible picture information, with a maximum amplitude between black and white of 0.7V. At the end of the picture information is the front-porch followed by a −0.3V of sync pulse, which is regenerated to provide system synchronization. The back porch is the part of the signal that represents the black or blanking level. In color NTSC systems the chroma or color burst signal is added to the back porch, normally occupying 9 cycles of 3.58 MHz subcarrier (4.43 MHz for PAL systems).

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal needs to be restored to an externally set DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the picture displayed. This DC reference voltage VR, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC baseline from the video amplifier to equal the externally set reference voltage VR.

Figure 2 shows the schematic of a classical DC control servo system.

Figure 1. Video Signal

Figure 2. Classical DC Control Servo
Video Signal Refresher — Contd.

The sync pulse is used to drive the control switch so that the DC servo loop is closed during the back porch of the video signal. The low pass filter removes the chroma burst. Operation of the DC loop is best understood by considering the voltage, $V_C$, across the hold capacitor, $C_{HOLD}$. During the back porch sample period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that,

$$V_C = V_{BP} - V_{BP}/[A_1*A_2] - V_R/A_1$$

where $V_{BP}$ is the average back porch voltage for the sample period.

The net result is that $V_{OUT} = V_R - V_{BP}/A_2$, which shows that the output is clamped to $V_R$ with an offset term of $-V_{BP}/A_2$. This offset is clearly small with a high gain DC loop amplifier, $A_2$. The EL2090 has a DC loop amplifier gain of 15 kV/V, reducing this offset to the order of a few millivolts. During the hold period the switch is open and the stored DC value of $V_C$ is now subtracted from the incoming video signal, making

$$V_1 = V_{IN} - V_{BP} + V_R/A_1$$

and so

$$V_{OUT} = A_1[V_{IN} - V_{BP}] + V_R$$

which effectively sets the back porch to $V_R$ and the video signal is amplified by the forward amplifier with gain, $A_1$.

Subcircuits

The EL2090 DC restored amplifier is a 14-pin monolithic version of the circuit shown in Figure 2. The video amplifier, $A_1$, is a 100 MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input is high impedance and the inverting low impedance. However, the special feature of the CFA is that when in closed loop, the feedback current is determined by resistor, $R_F$, which controls the bandwidth of the amplifier independently of the gain setting resistor $R_G$.

The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal $Z$-node and buffering this $Z$-node voltage through a low impedance output, as shown schematically in Figure 3 below.
Subcircuits — Contd.
The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current-limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through \( R_F \) supplies the current demanded by \( R_G \) and the input error current into the inverting input terminal. It is this feedback current component of \( R_F \) which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the \(-3\) dB bandwidth is approximately,

\[
f - 3 \text{ dB} = 1/[2\pi R_F C_Z]
\]

where \( C_Z \) is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, \( A_1 \), is simply

\[A_1 = [1 + R_F/R_G],\]

and the \(-3\) dB frequency can be controlled with \( R_F \) while the closed loop gain can be set independently with \( R_G \).

Features of the EL2090
Elantec pioneered the development of monolithic CFAs. A first to the market with the CFA the established reputation is confirmed with the EL2090 which is the first monolithic DC restored video amplifier. The device is built with Elantec’s fast proprietary complementary bipolar technology which yields NPN and PNP transistors with equivalent AC and DC performance.

The on-chip current-feedback amplifier is optimized for video performance, and since it is a current-feedback amplifier it ensures that the \(-3\) dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 100 MHz when driving 75\( \Omega \). The sample and hold circuit is optimized for fast sync pulse response; the switch operates in only 40 ns. A particular feature of this sample and hold output buffer is its low output impedance which is fairly constant over frequency and load current. This provides good isolation and thus prevents the DC restore circuit from interfering with video amplifier performance through \( R_{AZ} \).

Note that the burst output of Elantec’s EL4581 and EL4583 sync separator chips can drive the Hold input of the 2090 directly.

Typical Application Circuit
Figure 4 shows a component level schematic diagram of the gain x2 DC restored video amplifier. The operation of the circuit is based upon the simple analysis given with the amplifier connected in the non-inverting mode of operation. The application circuit will restore the video DC level in ten scan lines, even if the hold pulse is as short as 2 \( \mu s \) long. The current-feedback resistor \( R_F \) of 300\( \Omega \) will give a stable bandwidth of 115 MHz and all component values are chosen to maintain optimum speed and performance.

DC feedback resistor \( R_{AZ} \) is 2 k\( \Omega \) and is sufficiently larger than \( R_F \) to provide reasonable isolation between the sample and hold circuit and video amplifier and thus avoid any video signal coupling back to the sample-hold. \( R_{AZ} \) may be (optionally) split into two 1 k\( \Omega \) resistors and a 820 pF bypass capacitor to reduce unwanted transient feedthrough from the sample and hold to the video signal to less than about 1 mV seen at the amplifier’s output. The circuit is designed to operate using \( \pm 15V \) supplies, but it can operate down to \( \pm 5V \) supplies by changing \( R_{AZ} \) and \( C_{AZ} \) values. Alternatively an inverting configuration video amplifier could be used with appropriate exchange of the input signals to the DC loop amplifier.
Design Procedures

1. Determining RAZ
Ideally RAZ should be large to provide good isolation between the sample and hold buffer and the video amplifier. This is because any video-induced current through RAZ will cause changes in the buffer output impedance. A large series RAZ will reduce the effect of buffer output impedance variations and thus preserve the differential gain error of the video amplifier. However, too large a value of RAZ along with the output voltage compliance of the buffer will limit the maximum I_{AZ}, the DC correction current. A lower I_{AZ} will result in a lower restored reference level. Consequently, trade-offs have to be made between RAZ, the maximum restored reference level, and the supply voltage which controls the output voltage compliance of the buffer. The following equations address some of the issues related to the trade-offs.

During the back-porch of the video signal, the sample and hold switch is closed. The servo loop charges C_{HOLD} to a voltage level necessary to bring the video amplifier output to the reference input level. The maximum voltage of C_{HOLD} is limited by the supply voltages.

\[ V_{REF} = (V_{BP} \times A_1) - V_{AZ} \left( \frac{R_F}{RAZ} \right) \]  
(1)

where

- \( V_{REF} \) is the new stabilized back-porch level at the output of the video amplifier.
- \( V_{BP} \) is the input back-porch offset voltage at the video amplifier input.
- \( A_1 \) is the close loop gain of the video amplifier.

\[ A_1 = \frac{R_F}{1/RAZ + 1/R_G} + 1 \]  
(2)

\( R_F \) is the feedback resistor of the current-feedback video amplifier. It is nominally 300\( \Omega \) for \( A_1 = +2 \). In gain of +5 application, \( R_F \) should be decreased to 270\( \Omega \) to maintain gain flatness.

\( V_{AZ} \) is the buffered C_{HOLD} voltage developed by the loop to maintain the output at the reference level.

\[ -V_{SUPPLY} + 2.5V < V_{AZ} < +V_{SUPPLY} - 2.5V \]  
(3)

Analysis of equation (1) shows that since \( V_{BP}, A_1, \) and \( R_F \) values are established by system requirements, the maximum RAZ is determined by \( V_{AZ} \) and \( V_{REF} \). A high RAZ value requires a proportionally high \( V_{AZ} \) voltage and low \( V_{ref} \). Outside the back-porch period, the switch is opened. The DC offset is maintained.
2. Design Example

Below examples are intended to show how $R_{AZ}$ changes under different supply voltages and reference level.

**Example A.**

$V_{SUPPLY} = \pm 15V$

$V_{REF} = 0V$

$A_1 = 2$

$V_{BP} = \pm 1V$

$R_F = 300\Omega$

Applying equation (3), the output voltage compliance $V_{AZ}$ of the sample and hold buffer can be calculated,

$$-12.5V \leq V_{AZ} \leq 12.5V$$

Using equation (1), $R_{AZ} = 1.8\ k\Omega$ for $V_{BP} = \pm 1V$.

Once $R_{AZ}$ is determined, equation (2) gives $R_G = 360\Omega$.

**Example B.**

$V_{SUPPLY} = \pm 5V$

$V_{REF} = 0V$

$A_1 = 2$

$V_{BP} = \pm 1V$

Applying equation (1), $R_{AZ} = 375\Omega$ for $V_{BP} = \pm 1V$.

Equation (2) gives $R_G = 1.5\ k\Omega$.

**Example C.**

$V_{SUPPLY} = \pm 15V$

$V_{REF} = 1$

$A_1 = 2$

$V_{BP} = \pm 1V$

Applying equation (3),

$$-12.5V \leq V_{AZ} \leq 12.5V$$

$R_F = 300\Omega$

Equation (1) gives

$R_{AZ} = 1.2\ k\Omega$ for $V_{BP} = -1V$

$R_{AZ} = 3.75\ k\Omega$ for $V_{BP} = -1V$

Therefore, $R_{AZ} = 1.2\ k\Omega$

Using equation (2), $R_G = 400\Omega$.

The above examples demonstrate the trade-off between the supply voltage, $R_{AZ}$, and the reference level. Examples A and B reveal that a lower supply voltage requires a lower $R_{AZ}$. Examples A and C show that when the supply rails are kept constant, a higher reference level requires a lower $R_{AZ}$.

3. Determine $C_{HOLD}$

Fast acquisition time is achieved with small values of $C_{HOLD}$, but this degrades droop performance. For video the droop needs to be better than $\frac{1}{2}$ IRE in one horizontal line, or less than 3.5 mV in 45 $\mu s$ for NTSC. The droop is primarily caused by $C_{HOLD}$ voltage decaying. Since the droop of $C_{HOLD}$ is amplified to the output by the ratio $R_F/R_{AZ}$ then $C_{HOLD}$ must be chosen to satisfy

$$\frac{dV_C}{dt} < 3.5\ mV/45\mu s$$

multiply $R_{AZ}/R_F = 510\ V/\mu s$.

$R_F = 510V/\mu s$.

Since $dV_C/dt = I_{DROOP}/C_{HOLD}$, and the discharge current $I_{DROOP}$ is a maximum of 50 nA, then

$C_{HOLD} = 98\ pF$, or 100 pF, the nearest preferred value.

If $R_{AZ}$ is decreased for lower supply operation, $C_{AZ}$ is correspondingly increased to preserve droop and acquisition characteristics.

4. Acquisition Time

Based on the values shown in Figure 4 the acquisition time is approximately 20$\mu s$. Note that it will take 10 chroma-burst of 2$\mu s$ each to finish settling from a $\Delta 1.0V$ input signal shift.

**Evaluation Printed Circuit Board**

A component layout of the application circuit is shown in Figure 5(b) with some additional features.

- $V_{REF}$ is applied externally to the grounded resistor $R_{14}$, which is decoupled with capacitor $C_{11}$.
- Optional 75$\Omega$ termination resistor has been included at the input and output.
- Built in guard ring on PCB board layout (Figure 5(b)) ensures that leakage from the hold capacitor is minimal to improve droop performance. The guard ring is connected to the S/H Out. The hold capacitor should be low leakage and so mica or mylar capacitors are recommended here.
Evaluation Printed Circuit Board
— Contd.

- Diode clamp circuit to overcome lock-up has been included on board.
- Optional AC input coupling capacitors of about 10 µF has been included.
- Optional snubber circuit has been included.
- Optional R-C low pass filter on hold input logic drive has been included should the logic signal require slowing down.

Printed Circuit Board and Layout Hints

Figure 5(a)–(d) on following pages, shows a component layout together with double sided pc-board. Ground plane is essential throughout to reduce parasitic inductance and stray pickup. Special precautions have been taken to avoid any discontinuity in ground plane since this will make the function of ground plane much less effective. Supply decoupling capacitors are kept close to the power supply pins to ensure good power supply integrity. The feedback path of the video amplifier should be kept as small as possible to avoid deterioration in high frequency gain accuracy. BNC connectors are included at the input and output.

\[
\begin{align*}
R1 &= 360\Omega \\
R2 &= 300\Omega \\
R3 &= 1\, k\Omega \\
R5 &= 75\Omega \\
R6 &= 220\Omega \\
R7 &= 4.7\, k\Omega \\
R8 &= 10\, k\Omega \\
R9 &= 10\, k\Omega \\
R10 &= 2\, k\Omega \\
R11 &= 100\Omega \\
R12 &= 10\, k\Omega \\
R13 &= 75\Omega \\
R14 &= 10\, k\Omega \\
C1 &= 0.1\, \mu F \\
C2 &= 0.1\, \mu F \\
C3 &= 4.7\, \mu F \text{ (Tant.)} \\
C5 &= 820\, pF \\
C6 &= 39\, pF \\
C7 &= 50\, pF \\
C8 &= 100\, pF \\
C9 &= 0.1\, \mu F \text{ (Ceramic)} \\
C10 &= 4.7\, \mu F \text{ (Tant., 25V)} \\
C11 &= 4.7\, \mu F \text{ (Tant., 25V)} \\
C12 &= 30\, pF \\
C13 &= 0.1\, \mu F \text{ (Ceramic)} \\
POT1 &= 10\, k\Omega \\
D1 &= \text{IN914} \\
D2 &= \text{ZN458B} \\
D3 &= \text{ZN458B (2.45 VREF)}
\end{align*}
\]

Figure 5(a). Component Values
DC Restored 100 MHz Current Feedback Video Amplifier

Figure 5(a)
**Do’s and Don’ts**

**General Circuit Layout**
As with all high frequency devices care must be taken with printed circuit board layout. Good ground plane construction is essential and DC power supply integrity must be ensured, so the power supply pins should be bypassed to ground with ceramic capacitors as close to the supply pins of the device as possible. The video current feedback amplifier is, like all CFAs, particularly sensitive to stray capacitance at the inverting input. This capacitance combined with the inverting node input resistance generates an additional high frequency pole in the feedback loop of the CFA leading to gain peaking in the response. Consequently pc-boards should be designed to keep lead lengths as short as possible around the inverting input node, with the ground plane positioned sufficiently far away to prevent this gain peaking effect.

**Load Capacitance**
In general load capacitance with negative feedback amplifiers causes gain peaking. This is because the load capacitance with the non-zero output resistance of the amplifier creates an additional pole in the feedback loop. The video CFA within the EL2090 is no exception to this and it may be necessary to add a series R-C snubber network to ground to minimize peaking, as shown in the data sheet, where the appropriate components are selected for a particular value of load capacitance.

**Sample and Hold Section**
Clock-feedthrough to \( C_{\text{HOLD}} \) leads to an undesirable hold-step, effecting the DC bias level.

![Fig 6](image)

Increasing \( C_{\text{HOLD}} \) is the most direct way of reducing this effect. Under normal operation the loop amplifier only deals with a small correction to \( V_C \) and although increasing \( C_{\text{HOLD}} \) will compromise the slew-rate of the sample-hold section, this is not a practical limitation. However with \( C_{\text{HOLD}} > 1 \text{nF} \) and the sampling interval \( t_S < 2 \text{ms} \) then on power up the device may lock-up if \( V_C \) approaches \( V_{CC} \) causing the output transistors of the sample-hold amplifier to be taken out of their active region. The net result is that the lock-up does not self recover. Limiting \( V_C \) to \( V_{CC} - 3 \text{V} \) using the external clamp circuit shown in Figure 4 prevents this lock-up condition from occurring.

![Fig 7](image)
A Low Distortion Tuneable Sine Wave Oscillator

Summary of Performance Characteristics

One can make a low distortion tuneable oscillator by incorporating an active filter inside an AGC loop. With a control voltage $V_G$ of 0.1 to 2V, one can obtain over a decade of tuning range, with oscillation frequencies from 200 kHz to 3 MHz in this particular design. Total Harmonic Distortion (THD) is $-64.5$ dB at $V_G = 1V$, and is kept below $-57$ dB over most of the tuning range. Modulation sidebands due to loop jitter are at least 50 dB down over the entire tuning range, with suppression approaching 56 dB for higher $V_G$. Linearity error for $f_{OSC}$ vs. $V_G$ is below 4%.

Theory of Operation

The active filter employed in this design is a state variable configuration with the EL2082 in the integrator path providing the frequency control; a circuit diagram of this filter is shown in Figure 1. The EL2082 is a current mode multiplier with low input impedance ($95\Omega$ nom) and current source output. It takes the current through the integrator resistor $R_{IN}$, scales it by a gain determined by $V_G$, then outputs the scaled signal current to the integrator capacitor $C_F$. In effect, we can modify the integrator time constants by adjusting $V_G$; the filter cutoff frequency is then given by

$$f_0 = \frac{V_G}{1V} \cdot \frac{1}{2\pi \left( R_{IN} + 95\Omega \right)C_F}$$

This filter serves as the feedback network for the oscillator, a block diagram of which is shown in Figure 2. At frequency $f_0$, the filter phase is 0°, and if the feedback gain is $\geq 1$, sustained oscillation will occur. To ensure startup, many oscillator designs have feedback gain >1, but then oscillation amplitude grows until nonlinearity sets in and reduces the loop gain down to 1, thus making it difficult to generate a pure sine wave. In this design, Automatic Gain Control (AGC) is used to maintain unity gain and stable oscillation amplitude. The AGC circuit consists of a 4-quadrant multiplier, which multiplies the output sine wave with itself to generate a DC and double frequency term. The high frequency term is filtered and the remaining DC voltage, which provides a measure of the output amplitude, is used to control the variable gain amplifier. This gain is continually adjusted to provide unity gain around the feedback loop.

Figure 3 shows a circuit diagram of this oscillator. The top part of the diagram is the tuneable active filter implemented using two EL2082s and a EL2444 quad op amp package. The output of this filter is fed back to its input via a unity gain buffer, obtained by connecting pins 11 and 14 of the EL4451 together. To compensate for filter losses, this output is also fed through the resistive divider $R_1/R_2$ into the variable gain amplifier of the EL4451. By setting the gain to just the right amount, we have unity gain in the feedback path and the necessary conditions for stable oscillation.

This adjustment is provided by an AGC, which consists of the EL4450 four quadrant multiplier and a filter to act as a RMS to DC converter. If the oscillation amplitude increases, the DC control voltage also increases to lower the gain of the EL4451 amplifier. The inverse can be said for oscillation amplitude that is too small. The loop will servo itself until the mean-square of the oscillation amplitude equals the reference voltage on pin 10 of the EL4450. This reference voltage can be changed by adjusting the potentiometer VR1.

Design Notes

Several issues were raised in this design, the first of which is the speed and stability of the AGC loop. A loop that is too slow, as was found early on, is not able to track the oscillation amplitudes; what results is a backlash phenomenon where the loop is constantly over-correcting and never finds a stable operating point. On the other hand, a loop with too much bandwidth would allow excessive feedthrough, again destabilizing itself and distorting the output. A loop bandwidth of $\sim 16$ kHz has been found to be adequate for this design.
Referring to Figure 3, we see that the EL4450 provides a "pseudo" integrator in its output path; it is termed pseudo since it provides rolloff only until \( \approx 16 \) kHz, after which it becomes a unity gain element. To continue the rolloff after 16 kHz, we need an additional lowpass filter with a pole at the above frequency. Although this seems sound, we encountered loop instabilities with this implementation. By moving the pole of the lowpass filter above the "integrator zero", the loop is stabilized.

The residual loop jitter causes another problem: modulation noise. Small variations in the loop voltage that reach the GAIN – pin of the EL4451 modulates the gain and creates Amplitude Modulation (AM) in the output waveform. Although this modulation is small, it is observable on the spectrum analyzer as sidebands around the fundamental. To reduce these sidebands we lowered the feedback into the multiplier, set by \( R_1 \) and \( R_2 \). Since the loop voltage directly modulates this feedback, by lowering the feedback we also lower the modulated components.

Another problem is the limited Q provided by the active filter network. As opposed to a crystal or LC tuned circuits, we are limited to painfully low Q's in this filter. Since \( Q \neq 1 \) unbalances the gain between filter stages, there is a practical limit to Q before the 2nd integrator is overdriven. Ideally we would like a high Q to reduce phase noise and to reduce the loop jitter. Unfortunately in this implementation, while \( Q > 1 \) does reduce modulation effects, it also increases the THD due to the gain unbalance mentioned earlier. In addition, a \( Q > 1 \) also introduces clipping problems in that during startup, the oscillator can swing to large amplitudes and clip, and the AGC has no hope of recovering from such an unhappy beginning. Hence, a \( Q = 1 \) was chosen for this design to provide reliable startup and lower THD.

As the frequency of operation increases, we see peaking in the active filter due to increased phase shifts through the op amp stages. Once the peaking causes the filter gain to exceed 0 dB at 0° filter phase, the AGC is no longer able to keep the feedback gain to 1, and clipping occurs in the oscillator output. For this reason it is recommended that the oscillation frequency be kept under 3.5 MHz. The range of operation in this design thus lies quite close to the upper limit. For those desiring lower frequencies of operation some recommended component values are given below:

<table>
<thead>
<tr>
<th>Tuning Range</th>
<th>( R_{in} )</th>
<th>( C_F )</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>( C_1 )</th>
<th>( C_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 kHz–300 kHz</td>
<td>3k</td>
<td>330 pF</td>
<td>330</td>
<td>240</td>
<td>10 nF</td>
<td>10 nF</td>
</tr>
<tr>
<td>200 kHz–3 MHz</td>
<td>3k</td>
<td>33 pF</td>
<td>330</td>
<td>120</td>
<td>1 nF</td>
<td>1 nF</td>
</tr>
</tbody>
</table>

The current design runs on a supply of \( \pm 5 \)V. It is possible to push the upper frequency limit to about 4 MHz by operating on \( \pm 12 \)V supplies, provided that the current limiting resistor \( R_Z \) for the LM337 is raised to 2 kΩ.
A Low Distortion Tuneable Sine Wave Oscillator

**Figure 2**

![Circuit Diagram](image)

**Figure 3**

![Circuit Diagram](image)

8-20
Typical Performance Curves

- Oscillation Frequency vs. Control Voltage
- Nonlinearity vs. Control Voltage
- THD and Modulation Noise vs. Control Voltage
High-Purity Sinewave Oscillators With Amplitude Stabilization
by Barry Harvey

While a wide variety of circuits and components are used to generate sinewaves, it has always been a challenge to produce spectrally pure and regulated sines in circuits that require no tuning nor adjustments. This article shows a practical method of achieving these goals. The classic system architecture is shown below.

The crystal (or other frequency-selective network) provides the oscillation path around the multiplier or variable-gain amplifier. The multiplier's output is sampled by some amplitude detector, shown here as a rectifier diode. The DC output of the rectifier is filtered by a low-pass filter, and the output of that is compared to a DC reference voltage by the servo amplifier. The gained-up error is then used as the multiplier's gain-control input. The amplitude-control loop serves to set the oscillation path gain to just unity, so that the multiplier's output doesn't grow nor decay, and the loop also maintains oscillation amplitude within the linear range of all components. This gain-controlled oscillator is more complicated than simple overdriven circuits, but it produces very pure sinewaves and has no start-up problems.

Basic Stabilized Oscillator Loop
Here is a realization using common components:

**Basic Oscillator with Amplitude Stabilization Loop**

The EL4451 is a two-quadrant multiplier, whose gain-control input voltage of $0 \rightarrow +2V$ produces a voltage gain of 0 to 2. The signal input receives a portion of the output signal passed through a series crystal. At resonance, the crystals impedance phase passes through $0^\circ$ and positive feedback occurs around the multiplier. The crystal has a series resistance of about $100\Omega$, so with the crystals $510\Omega$ load the multiplier will need to have a gain of 1.2 to sustain oscillation.

The output is rectified by a simple diode detector and compared to a reference voltage by an integrating op-amp. The integrator's output is attenuated by the 2 kΩ and 2.7 kΩ resistors so it cannot overdrive the EL4451 gain-control input and cause nonlinear oscillations. The diode detector has a 220Ω resistor in series so as to not cause output distortions due to charging pulses. A pull-down current flows through the 510k resistor to allow proper rectification.

Any crystal, up to about 50 MHz fundamental mode resonance, can be used. Overtone crystals will require an added series-tuned circuit to force harmonic oscillation modes. The crystal and 510Ω resistor can be exchanged to put the crystal at ground, using the parallel resonance mode of the crystal.

This circuit generates $-53$ dBc harmonic distortion at 2 MHz with ±5V supplies and 1 Vrms output into 500Ω. This is mostly due to the output stage nonlinearities of the EL4451, and it drops to $-60$ dBc at ±12V supplies. Reducing the output amplitude further improves distortion levels, although the simple diode detector requires a minimum 0.5 Vrms level. Sideband noise is excellent, spanning only 14 Hz at $-90$ dBc, the resolution of the spectrum analyzer used.

A series-tuned LC filter can be substituted for the crystal. As long as the loaded Q is greater than about 5, the output distortion will be as good as with the crystal. Sideband noise is worse than with the crystal, however.
This circuit generates very low distortion levels:

The EL4451 is connected in a slightly different way; the majority of crystal feedback is delivered to the REF input of the feedback amplifier, and a smaller amount of signal routed through the variable-gain input port. In this way, most of the signal runs through a simple voltage-follower path with minimal distortion. The total gain of the EL4451 in this connection is $1 + \left( \frac{\text{Vgain}}{2\text{V}} \right) \left( \frac{160\text{W}}{160\text{W} + 330\text{W}} \right)$, which needs to be servoed to about 1.2 for stable oscillation.

The output of the EL4451 is passed through a simple filter to additionally reduce harmonics, then used as the output. For my measurements, I loaded the output with an additional 500Ω, bringing the total load to 250Ω. The EL4451 can drive lower impedances, but the output distortion will rise. Note that no active amplifier nor buffer can be used to drive the output with distortion levels anywhere near that of the passive filter.

Rather than load the filter with a highly nonlinear diode detector, this circuit uses the high-impedance inputs of the EL4450 to sense output amplitude. This is a four-quadrant multiplier, and is used as a mean-square amplitude detector. The advantages include much more precise initial calibration, easier ripple filtering since its at twice the oscillator frequency, and a built-in amplifier which can be used as the servo error amplifier. The X- and Y- inputs of the EL4450 are wired together to produce an internal output quantity at the Σ point. Added to this is a static level from the LM336 reference that has a polarity that subtracts from the mean-square quantity. The FB terminal, normally used for DC feedback, is connected as something like an integrator using the 0.1 μF capacitor. Thus, the output amplifier of the EL4450 is both the low-pass filter and error amplifier for the servo loop, and attempts to maintain the output mean-squared voltage equal to that of the reference.
Harmonic distortion is $-74$ dB with the circuit running on $\pm 5$V supplies, and $-80$ dB with $\pm 12$V. As before, reducing the output amplitude improves distortion further.

The error amplifier is not actually required for amplitude stabilization. Since even a miniscule amount of oscillation loop gain more than unity results in a continuously growing amplitude, or a tad less than unity gain creates an ever-shrinking level, we could say that the gain-control input of the oscillating EL4451 already has infinite gain. This circuit makes use of this fact:

This circuit is very simple and still has the low distortion levels of the previous oscillators, but the output level is not well calibrated, despite the diode forward voltage compensation network connected to the Gain + terminal. Variations in crystal series resistance will vary output amplitude.

In summary, we see that recent multiplier ICs can be employed in simple circuits to generate highly pure sinewaves over wide frequency ranges. The particular devices shown are low-cost, yet well calibrated and flexible.

![Simple Linear Oscillator Diagram](image)
1. Introduction
The EL4089 is a complete monolithic video amplifier sub-system in a single 8-pin package. It comprises a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance. The part is a derivative of Elantec's high performance video DC restoration amplifier, the EL2090, but has been optimized for lower system cost by reducing the pin count and the number of external components. For RGB and YUV applications the EL4390 provides three channel in a single 16-pin package.

This application note provides background information on DC restoration. Typical applications circuits and design hints are given to assist in the development of cost effective systems based on the EL4089 and EL4390.

Figure 1. EL4089 and EL4093 Package Outlines
2. Video Signal Refresher

2.1 Composite Video Signal

The figure shown below represents a typical composite video signal, which has a standard distribution level of 1 V\text{p-p} into a 75Ω load, and comprises several sections. The video signal is the part containing the visible picture information, with a maximum amplitude between black and white of 0.7V. At the end of the picture information is the front-porch, followed by a sync pulse, which is regenerated to provide system synchronization. The back-porch is the part of the signal that represents the black or blanking level. In NTSC color systems, the chroma or color burst signal is added to the back-porch and normally occupies 9 cycles of the 3.58 MHz subcarrier.

2.2 DC Restoration—The Classical Approach

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal therefore needs to be restored to an externally defined DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the displayed picture. This DC reference voltage, VR, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC output from the video amplifier to be equal to an externally defined reference voltage VR. Figure 3 shows a classical approach to DC restoration in video systems.

![Figure 2. Typical Composite Video Signal](image1)

![Figure 3. Classical DC Restoration Control Servo Loop](image2)
2. Video Signal Refresher — Contd.
The Sync pulse is used to drive the control switch to the sample-and-hold, so that the DC servo loop is closed during the back-porch of the video signal. The lowpass filter is used to remove the chroma burst. The operation of the DC loop is perhaps best understood by considering the voltage appearing across the hold capacitor, $C_{\text{HOLD}}$. During the back-porch sampling period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that

$$V_C = V_{\text{IN}} - \frac{V_R}{A_1} \quad (1)$$

where $V_{\text{IN}} = V_{\text{BP}}$ (the average back-porch voltage of the incoming video signal). Equation (1) can be reconfigured,

$$V_C = V_{\text{BP}} - \frac{V_R}{A_1}$$

The net result is that

$$V_{\text{OUT}} \approx V_R + \frac{V_{\text{BP}}}{A_2} \quad (2)$$

which shows that the output is clamped to $V_R$ with an offset term of $V_{\text{BP}}/A_2$. This offset is clearly small for a high gain DC loop amplifier, $A_2$. During the hold period, the switch is open and the stored DC value of $V_C$ is now subtracted from the incoming video signal, which effectively sets the back-porch to $V_R$ and the video signal is amplified by the forward amplifier with gain, $A_1$, giving

$$V_{\text{OUT}} = (V_{\text{IN}} - V_C)A_1 = A_1 \left( V_{\text{IN}} - V_{\text{BP}} + \frac{V_R}{A_1} \right) = A_1(V_{\text{IN}} - V_{\text{BP}}) + V_R \quad (3)$$

2.3 DC Restoration—The EL4089 Approach
A simplified scheme of the EL4089 as a feedback system is shown in Figure 4. Unlike Figure 3, the input difference symbol is not shown because the error/correction voltage is stored across the coupling capacitor $C_{\text{HOLD}}$ which is outside the control loop.

The operation of the EL4089 is simple, but very subtle. In sample mode, the amplifier’s dynamics are such that the output is set to a predetermined reference voltage $V_R$, which may be at ground potential. The correction voltage required at the input of amplifier $A_1$ to maintain $V_{\text{OUT}}$ at $V_R$ is simply stored across capacitor $C_{\text{HOLD}}$.

![Figure 4. Simplified Block Diagram of EL4089](image-url)
2. Video Signal Refresher — Contd.
Consider the following analysis. With the switch closed, the input voltage of amplifier A1 is 
\((VR - V_{OUT})A2\) giving 
\(V_{OUT} = (VR - V_{OUT})A1A2\) and thus

\[ V_{OUT} = VR \left( \frac{A1A2}{1 + A1A2} \right) \approx VR \]  

(4)

Assuming that the loop gain A1A2 is very high.

The correction voltage stored across capacitor \(C_{HOLD}\) is simply

\[ VC = V_{IN} - (VR - V_{OUT})A2 \]  

(5)

Assuming in this instance that \(V_{IN} = VBP\), which is the average back-porch reference of the incoming signal, and substituting for \(V_{OUT}\) from Equations (4) and (5) gives

\[ VC = VBP - \frac{VR}{A1} \]  

(6)

Notice that the correction voltage \(VC\) is stored across that coupling capacitor \(C_{HOLD}\), which is external to the loop amplifier. Unlike the classical system of Figure 3, it is this unique feature of the EL4089 which obviates the need for a classical sample-and-hold buffer amplifier in the feedback path; thus allowing a very economical 8-pin solution to be realized. Furthermore, the coupling capacitor has two functions, namely to avoid DC bias interaction between different systems and to hold the correction voltage as described above.

During the hold period, the video input signal \((V_{IN})\) is amplified in the classical way by the *2 video amplifier A1, but in this case the correction voltage held by \(C_{HOLD}\) is subtracted from the input to give

\[ V_{OUT} = VR + (V_{IN} - VBP)A1 \]  

(7)

Summary of Operation
1. When the HOLD logic input is set to TTL/CMOS logic 0, the sample-and-hold amplifier can be used to null the DC offset of the video amplifier.

2. When the HOLD input goes to a TTL/CMOS logic 1, the correcting voltage is stored on the video amplifiers input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.

3. The video amplifier is optimized for video performance and low power. Its current-feedback design allows the user to maintain essentially the same bandwidth over a given gain range of nearly 10:1. The amplifier drives back-terminated 75\(\Omega\) lines.

Subcircuits
The EL4089 DC restored amplifier is an 8-pin monolithic version of the circuit shown in Figure 4. The video amplifier, A1, is a 60 MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input impedance is high and the inverting a low impedance. However, the special feature of the CFA is that when in a closed loop configuration, the feedback current is determined by the resistor, \(R_F\), which controls that bandwidth of the amplifier independently of the gain setting resistor \(R_G\).
2. Video Signal Refresher — Contd.
The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal Z-node and buffering this Z-node voltage through to a low impedance output, as shown schematically in Figure 5 below.

The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through RF supplies the current demanded by RG and the input error current into the inverting input terminal. It is this feedback current component of RF which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the $-3\,\text{dB}$ bandwidth is approximately,

\[ f_{-3\,\text{dB}} = \frac{1}{2\pi RF C_Z} \]  

(8)

where $C_Z$ is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, $A_1$, is simply

\[ A_1 = 1 + \frac{RF}{RG} \]  

(9)

and the $-3\,\text{dB}$ frequency can be controlled with RF while the closed loop gain can be set independently with RG.

![Figure 5. The Current-Feedback Op-Amp](image-url)
2. Video Signal Refresher — Contd.

The EL4390 Approach

The EL4390 is three high performance current feed-back amplifiers with DC restore function. A simplified schematic diagram of one of the channels in a DC restore configuration is shown in Figure 6. Its basic approach is very similar to the EL4089 in that the error/correction voltage is stored across the coupling capacitor $C_{HOLD}$ from the video input to the positive input of the amplifier. Different from the EL4089, when the sample and hold switch is close, an internal buffer amplifier is enabled to force the non-inverting input of the video amplifier to be equal to the reference input level. When the switch is open, an error voltage is stored on the input coupling capacitor $C_{HOLD}$ to maintain the offset at the output. The following details the mathematical relationships between the inputs and output.

When the sample and hold switch is close,

$$V_{OUT} = A_1 \cdot VR$$  \hspace{1cm} (11)

where $A_1$ is the close-loop gain of the amplifier.

The voltage across the hold capacitor is

$$VC = V_{IN} - VR$$  \hspace{1cm} (12)

In many NTSC video applications, the back-porch of the video signal is clamped. Thus, $V_{IN}$ is the input back-porch level, $VBP$.

$$VC = VBP - VR$$  \hspace{1cm} (13)

When the sample and hold switch is open, the voltage across the hold capacitor maintains the proper offset.

$$V_{OUT} = A_1(V_{IN} - VC)$$
$$= A_1(V_{IN} - VBP + VR)$$  \hspace{1cm} (14)

![Figure 6. Simplified Connection Diagram of EL4390](image_url)
3. Features of the EL4089C

Elantec pioneered the development of monolithic CFAs. As first to the market with the CFA our established reputation is confirmed with the EL4089 which is the first 8-pin monolithic DC restored video amplifier. A connection diagram for the EL4089 configured as a DC restoring amplifier with a gain of 2 restoring to ground (pin 3—zero voltage reference) is shown in Figure 7.

The EL4089C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089C is specified for operation over the 0°C to +75°C temperature range.

The on-chip current-feedback amplifier of EL4089 and EL4390 is optimized for video performance. Since it is a current-feedback amplifier, the -3 dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 60 MHz for the EL4089 and 80 MHz for the EL4390 when driving 75Ω. The sample and hold circuit is optimized for fast sync pulse response.

4. Typical Application Circuits

The EL4089 and EL4390 are designed to DC-restore a video waveform (Figure 2). A typical application circuit of the EL4089 is illustrated in Figure 8. The following analysis also applies to the EL4390. This circuit forces the cable driving video amplifier's output to pin 3 reference voltage level when the HOLD pin is at a logic low. In the case of EL4390, when HOLD pin is logic low, the output of the video amplifier is driven to the reference voltage multiply by the close loop gain of the video amplifier. In Figure 8, pin 3 is grounded and HOLD pin is low during back-porch of the video signal, consequently, the back-porch is clamped to the ground voltage level.

Figure 7. EL4089 Connection Diagram (Configured as a DC Restoring Amplifier with a Gain of 2, Restoring to Ground)
4. Typical Application Circuits — Contd.

CX1 Determination

The correction voltage is stored across the capacitor CX1, an external ceramic capacitor connecting from the video signal input to the non-inverting input of the video amplifier. The following demonstrates how the CX1 capacitor should be chosen to satisfy the system droop voltage and sampling requirements.

Ideally the input impedance of the video amplifier should be infinite during the hold period to avoid any discharging effects on the CX1 capacitor. However, due to the inherent nature of the bipolar transistors, a bias current is always present. This bias current discharges CX1 during the hold time and as a result causes the correction voltage across CX1 to drift. Equation (15) gives the basic relationship between correction droop voltage and the CX1 value.

\[
V(\text{droop}) = \frac{(I_B^+) (T_{\text{LINE}} - T_{\text{SAMPLE}})}{CX1} \tag{15}
\]

Where:

- \(V(\text{droop})\) is the voltage change across CX1 during hold period.
- \(I_B^+\) is the amplifier’s non-inverting input bias current.
- \(T_{\text{LINE}}\) is the single video line duration.
- \(T_{\text{SAMPLE}}\) is the sampling time during which the S/H switch is closed.

The output voltage change due to voltage drooping is simply,

\[
V_{\text{OUT(\text{droop})}} = V(\text{droop}) \times A1
\]

Where:

- \(A1\) is the close loop gain of the video amplifier.

In the Figure 8 design example, a typical input bias current of the video amplifier is 1 µA, so for a 62 µs hold time and 0.01 µF capacitor, the correction voltage droops 6.2 mV; consequently, the output voltage drifts by 12.4 mV in one video line.
4. Typical Application Circuits — Cont'd.

The CX1 value and sampling time also determine the amount of time required by the EL4089 to reach within its DC-restored voltage range.

\[ V(\text{charge}) = I_{OUT} \frac{T_{\text{SAMPLE}}}{CX1} \]  

(16)

Where:

- \( I_{OUT} \) is the sample and hold amplifier output current.

The sample and hold amplifier can typically provide a current of \(300 \mu A\) to charge CX1, so with \(1.2 \mu s\) sampling time, the output can be corrected by \(36\) mV in each line.

Equations (15) and (16) demonstrate the trade-offs between CX1, sampling time, DC off-set droop voltage, and speed of the DC-restore function. Using a smaller value of CX1 increases both the voltages that can be corrected each line and the drift while being held, likewise, using a larger value of CX1 reduces those voltages.

In Figure 9, a resistor is connected from the non-inverting input of the amplifier to the negative supply to compensate for the non-inverting input bias current. To obtain the optimum performance, the compensation resistor R1 should be adjusted to give 0 mV droop voltage at 50% field.

The restore current generated by the sample and hold amplifier decreases as the output voltage approaches the reference voltage. This effect combines with the 7 mV of offset voltage error in the sample and hold amplifier can result in a 22 mV of total error from the output to the reference voltage input during clamping. A method of correcting this problem is depicted in Figure 10. A voltage divider is used to compensate for the sample and hold amplifier offsets.

A complete DC-restore circuit with the EL4581 sync separator is shown in Figure 11. An optional RC low pass filter on HOLD input pin is included should the logic signal require slowing down. This RC network can also serve to prevent foot-through from the falling and rising edges of the back-porch sync timing signal to the video amplifier output. The video DC restore output and EL4581 back-porch timing waveforms are illustrated in Figure 12. During the back-porch interval, the EL4581 pulls the hold pin of the EL4089 low and the EL4089 servo loop forces the output to the reference voltage level. In the photo, the input back-porch voltage level is \(0.5V\) and the output back porch voltage level is restored to \(0V\), the reference voltage level.
4. Typical Application Circuits — Contd.

Figure 9. $I_{B+}$ Bias Current Correction

Figure 10. Sample and Hold Off-Set Error Compensation
4. Typical Application Circuits — Contd.

Figure 11. EL4581 and EL4089 Restore Amplifier and Sync Separator

Figure 12. Video Output and EL4581 Back-Porch Sync Signal
4. Typical Application Circuits — Contd.

**EL4089 in Inverting Gain Configuration**

Placing the hold capacitor in the signal path leads to sync signal feed-through and phase distortion of the burst signal. Rearranging the EL4089 in the inverting configuration as shown in Figure 13 provides significant improvements.

Figure 14 indicates a 15 mV of voltage spike in amplifier output during the sampling interval and coincides with the falling and rising edge of the HOLD signal. The output voltage spike is caused by the charging current injecting out of the output of S/H amplifier during the back-porch interval. One way to minimize the sync feed-through is to feed the video input signal directly into the inverting input of the video amplifier and short the DC restore capacitor to ground. As a result, the video input signal is not affected by output current of the S/H amplifier. The voltage spike is also reduced by an addition of a simple RC network from the output of the EL4581 to the HOLD input of the EL4089. Figure 15 test result shows no voltage spikes and only a 4 mV of voltage dip during the sampling period. In the inverting configuration, the video signal goes directly into a purely resistive component, thus, no phase shift occurs.
4. Typical Application Circuits  
— Contd.

**EL4581 Interface**
The hold input of the EL4089 is designed to interface directly to Elantec's existing suite of sync separators, namely the EL4581 and the EL4583. The connection diagram of the EL4581 is shown in Figure 16.

The EL4581 extracts timing information including composite sync, vertical sync, burst/backporch timing and odd/even field information from standard negative going sync NTSC, PAL, and SECAM video signals. The EL4581 detects video signals from 0.5 to 2 Vp-p. The 50% slicing feature provides precise sync edge detection even in the presence of noise and variable signal amplitudes. A built-in linear phase, third order, color burst filter minimizes spurious timing information and reduces the number of external components. The integrated circuit is also capable of providing sync separation for non-standard, faster, horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default output is produced after an internally generated time delay, in the event of missing serration pulses, for example, in the case of a non-standard video signal. All outputs are active low.

5. Printed Circuit Board Layout Hints

The feedback path of the video amplifier should be kept as small as possible to avoid deterioration of high frequency gain accuracy.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the VIN- pin (pin 1) to minimize the stray capacitance between pin 1 and ground.

Power supply bypassing is important and a 0.1 μF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7 μF tantalum bead capacitor, is recommended.

When both digital and analog grounds are on the same board, the EL4089 should be on the analog ground. The digital ground can be connected to the analog ground through a 100Ω–300Ω resistor near the EL4089. This allows the digital signal a return path while preventing the digital noise from corrupting the analog ground.

![Figure 16. EL4581 Connection Diagram](image-url)
Real Time Power Measurement of a Transistor

Introduction
It is quite typical to monitor the current through a component or a voltage on a node to regulate an input. Some applications may find it more useful, however, to monitor the power through a transistor. One such occasion would be in charging a battery. When the voltage is low, the designer may want more current charging, but as the voltage increases, the current could decrease, ultimately saving charging time and power.

Circuit Description
The circuit in Figure 1 utilizes an EL4452, a wideband variable gain amplifier compensated for a gain of 10. Circuit operation is very straightforward. Add a small resistor (Re) in shunt with the emitter and apply the differential voltage across it to the differential input of the EL4452. The voltage at this input will be:

\[ V_{IN1} = I_e \times Re \]

Secondly, attach a simple voltage divider between the collector and emitter and apply this voltage to the gain input of the EL4452. The voltage at the gain input will be:

\[ V_{IN2} = V_c \times R_{c2}/(R_{c1} + R_{c2}) \]

The voltage divider, R1 and R2, is necessary to ensure linearity if the collector will swing beyond ±2V.

Simply choosing \( R_{fb} \) and \( R_{gain} \) to give a gain of ten (\( R_{fb} = 9 \times R_{gain} \)), the output will be a real-time, scaled measurement of power:

\[ V_{OUT} = k \times I_e \times V_c \]

where \( k = [Re \times R_{c2} \times 10/(R_{c1} + R_{c2})] \)

The EL4452 is internally compensated for a feedback gain of 10. It is not guaranteed stable for smaller values of gain. Also, since it is a high frequency part, the feedback resistors should be on the order of hundreds of ohms so that the pole created by the feedback resistors and the parasitic capacitances does not limit the performance. If there are instability problems with parasitics, small capacitors can be placed across \( R_{fb} \) and \( R_{gain} \) to dominate these parasitics, increase the compensation, and allow for higher divider resistances.

Conclusion
A circuit capable of providing real time power measurements has been presented. This circuit has a functional bandwidth of 50 MHz (with \( R_{fb} \) and \( R_{gain} \) chosen for a gain of 10.) The gain bandwidth product holds, so if more gain is needed, it is a proportional tradeoff with bandwidth.

**Figure 1**
Measuring the Thermal Resistance of Power Surface-Mount Packages

by B. Harvey

Modern miniature IC packages have allowed great space savings in products, but frustrate the designer by concentrating the heat generated by circuits into smaller volumes. Increasing IC speeds and complexities over the years have also demanded greater power dissipation. Higher internal operating temperatures will shorten the life of an IC; elevated but safe temperatures often reduce the quality of performance in circuits, for instance degrading frequency response or distortion.

To cope with the problem, a variety of heat management packages have been introduced which conduct heat from the IC die through the package leads to the circuit board. The board becomes the major heatsink, and the onus of thermal design passes from the IC manufacturer to the board designer. This article is intended to assist the board designer in measuring thermal resistance of mounted IC devices efficiently.

Traditional parameters \(\theta_{JA}\) (thermal resistance of a device not connected to anything) and \(\theta_{JC}\) (infinite heatsink connected to the part) are not useful with mounted devices. Circuit boards are neither insignificant nor infinite heat sinks. We will use the parameter \(\theta_{JM}\) as the mounted thermal resistance of an IC, and it will vary with die size, package type, and circuit board features. The \(\theta_{JM}\) can be estimated by thermal simulation of the part and its mounting environment, but seldom is there concrete data on the thermal structure of the IC, and correctly modeling the board environment is difficult. A good way to estimate \(\theta_{JM}\) is to solder the IC to an area of circuit board that has been suitably sculpted with a Dremel tool to emulate a final board pattern in the region of the test device (or a finished board itself) and use the following circuit to measure \(\theta_{JM}\):

\[
\text{Some terminal} \text{ is any pin that is connected to an internal parasitic diode whose other connection is either power supply pin. The IC manufacturer's technical support people can help select the right pin and drive polarity. We will use the forward voltage as a measure of internal die temperature. When the relay grounds the supply pins, R provides a current from a supply to bias the diode. Depending on the internal diode connection, V+ or V− will be connected to R. R should supply a current low enough to create minimal resistive drop in series with the diode. 50 \mu{A} is a good guess for the current, or any current that sets up about 600 mV of forward diode voltage at room temperature. The general equation for diode tempco (it generally need not be measured directly) is:}
\]

\[
\frac{\Delta V}{\Delta T} = -(1.12V_{be}(25^\circ C))/300^\circ K. \text{ Thus a 600 mV junction at room temperature has a } -1.7 \text{ mV/}^\circ C \text{ temperature coefficient.}
\]
Using a storage or digitizing oscilloscope measuring the forward diode voltage, we will observe the thermal relaxation of the die after a steady power dissipation is terminated. The dissipation is the part’s own supply current, applied through the relay. The relay’s drive is also the oscilloscope trigger. Because the temperature change may only cause tens of millivolts of diode voltage variation against the background of 600 mV, a stable differential-amplifier with adjustable offset will be used for the oscilloscope input. Alternately, the ground of the above circuit may be shifted with a third supply before being connected to the oscilloscope.

This is the test sequence:

1. Connect everything with the device powered down. Set the oscilloscope sweep to the slowest setting, continuously sweeping.
2. Adjust the offset against the diode voltage to center the oscilloscope trace. The 10 mV/div. sensitivity is a good start.
3. Apply power to the device via the relay. The oscilloscope trace will be off-screen. Allow the part at least ten minutes to warm up its mounting.
4. Clear any stored trace. Turn off power to the device. The following trace should be seen on the oscilloscope:

We see an initial rapid cooling followed by very slow settling back toward room temperature. The cooling rate is not a simple exponential decay, but has a wide range of time dynamics. Here is the decay behavior of an EL1501 mounted on a large heat spreader:

![Oscilloscope Display of Diode Voltage Relaxation During Cooling](image)

For the first ten milliseconds little die temperature change occurs. Then the heat makes its way through the die and flows out through the leadframe, which occurs in around ten seconds. The last event is the settling of the heat-sinking board, which resolves in ten minutes. Clearly, thermal measurements require patience and time.

The thermal resistance $\theta_{JM}$ is then the temperature variation (long-term) divided by the power dissipated, so:

$$\theta_{JM} = \frac{\Delta T_{diode}}{P_{diss, quiescent}}$$

$$= \frac{\Delta V_{diode} \cdot 300^K}{P_{diss, quiescent} \cdot (1.12V - V_{BE} (25^\circ C))}$$

**Thermal Relaxation vs. Time of a Mounted Power SO-20 Package**

![Graph: Thermal Relaxation vs. Time](image)
Using this technique, the thermal resistance of the SOL-20 fused-lead package was measured. This package houses the EL1501 and has four center leads on each side fused to the IC's mounting header. Thus, heat flows directly through these pins from the IC and spreads through the ground plane on top of the circuit board. A nearly continuous ground plane is hand-drawn. Several variations of the board were tested. The first was the most straightforward: just the top foil is a heatsink. By cutting away board material, a variable area was implemented and thermal resistance measured. Then the measurements are repeated on an identical board with no solder mask to add to thermal resistance. Another variation was to create another heatsink area on the back of the board, thermally connected to the top foil by a multitude of feedthroughs. Finally, a copper sheet-metal heatsink was soldered to the top foil near the IC's heat-spreading pins.

The results are shown in this graph:

The SO-20 standard package has a $\theta_{JA}$ of 80°C/W. With 4 in² of circuit board heatsink copper with solder mask cutout, the thermal resistance drops to 32°C/W. Given a quiescent dissipation of 1.25W, the die temperature rise of the mounted EL1501 is 40°C. With a maximum ambient temperature of 85°C, we have a worst-case die temperature of 125°C, safely within the 150°C package limit.

Some observations:
1. 4 in² of copper area is sufficient in that more doesn't help much.
2. The bottom foil did not greatly help.
3. Removing the solder mask over the heat spreading area, if appropriate, reduces $\theta_{JM}$ nicely.

Finally, a large metal heatsink mounted close to the heat-spreading pins produced a $\theta_{JC}$ of 30°C/W.
Driving Reactive Loads with High Frequency Op-Amps
by Barry Harvey and Chris Siu

As the bandwidth of op-amps today pushes past 100 MHz towards the GHz region, increasing attention must be paid to the components, loads, and circuit traces which surround the op-amp. Not only is this necessary to optimize performance, but neglecting to do so may throw the amplifier into oscillation. This application note discusses the effect of loads, especially capacitive ones, on the behaviour of a high speed op-amp.

1.0 Real World Loads
To start, one needs to question whether there are any pure capacitive loads at high frequencies. To connect any load we need some wires or metal interconnect, and associated with these wires are resistance and self-inductance. In the following sections we will examine some possible loads and their behaviour over frequency.

Coaxial Cables
Coaxial cables must be terminated in the proper impedance to look like a resistive load to the driving source. A common myth is that an unterminated cable looks capacitive. While this may be true for short cables at low frequencies, it certainly does not hold at higher frequencies. An unterminated cable presents a varying impedance to the source over frequency, and it can look capacitive or inductive depending on the length of the cable and the frequency. This behaviour can be explained by viewing the coaxial cable as a lossless transmission line. The input impedance $Z_i$ of a transmission line with characteristic impedance $Z_0$ and length $L$, terminated in a load $Z_L$, is given by:

$$Z_i = Z_0 \frac{Z_L + jZ_0 \cdot \tan \beta L}{Z_0 + jZ_L \cdot \tan \beta L}$$

where $\beta = 2\pi/\lambda$, and $\lambda$ is the size of one wavelength on the line. As an example, consider the standard RG58C/U 50Ω coaxial cable. If we terminate the cable with a 50Ω load, then by the above equation $Z_i = Z_0$ and the cable should look perfectly resistive over frequency. Figure 1.1 shows an actual measurement done on a 5' long cable terminated in a 50Ω load. Except for minor impedance variations due to mismatch and line loss, the cable does look like 50Ω over a wide range of frequency. If the cable was terminated improperly, with a 75Ω load for example, the impedance then varies with frequency as shown in Figure 1.2. Note that even though we have terminated the cable with a resistive load, the cable impedance phase varies between $\pm 23^\circ$. In the extreme, if the cable is unterminated, then $Z_L = \infty$ and the equation reduces to $Z_i = -jZ_0/(\tan \beta L)$. Figure 1.3 shows the input impedance of an unterminated 50Ω cable, and we see the phase skipping between $-90^\circ$ (capacitive) to $+90^\circ$ (inductive) at regular intervals. In fact, for frequencies at which the line length is an odd multiple of a quarter wavelength, $Z_i$ becomes zero. Conversely, for frequencies at which the line is a multiple of a half wavelength, $Z_i$ becomes infinite.

![Figure 1.1. Impedance of a 50Ω Cable Terminated in 50Ω](image1.png)

![Figure 1.2. Impedance of a 50Ω Cable Terminated in 75Ω](image2.png)
Driving Reactive Loads with High Frequency Op-Amps

Figure 1.3. Impedance of an Unterminated in 50Ω Cable

The moral of the story is that you must terminate your cable with the correct load at high frequencies. Otherwise, the driving source will see a wildly changing load with frequency, and this may cause the amplifier to oscillate.

Discrete Capacitors

At high frequencies, another parasitic which becomes dominant is the inductance of a leaded capacitor. We can treat the capacitor as a series RLC circuit, with L modelling the lead inductance and R modelling the losses due to the electrodes, leads, and dielectric. The capacitor will thus self-resonate at a frequency given by:

\[ f_0 = \frac{1}{2\pi \sqrt{LC}} \]

As an example, the impedance of a 10 nF leaded ceramic capacitor was measured, yielding the equivalent series RLC values of 0.66Ω, 36 nH, and 8.6 nF respectively. Figure 1.4 shows the impedance of this capacitor over frequency, and we see that it self-resonates at 9.1 MHz, behaving as an inductor for frequencies above that. For this measurement the leads of the capacitor were kept as short as possible. If we were a bit sloppy and left 1" leads on the capacitor, the inductance would increase to about 60 nH, lowering the resonance down to 7 MHz. Generally, an inch of slender wire has about 20 nH of inductance per inch, which is why it is so important in high frequency work to minimize lead length.

Figure 1.4. Impedance of a Leader 10 nF Capacitor

Inputs of Active Devices

Besides driving cables or passive loads, an amplifier could also be driving the input of another active device. At first, one might think that the input of an op-amp can be modeled by some high-value resistance in parallel with a capacitance. While this model is correct to some extent, some measurements quickly reveal that the input capacitance is not all that "pure". Figure 1.5 shows the input impedance of the EL2044 connected as an unity gain buffer. While the impedance does decrease with frequency, it does not do so at -6 dB/octave; rather, the impedance is decreasing at a greater rate. The phase of the input impedance also reveals the "impurity" of this input capacitance.
Other Capacitive Loads
As the examples above may suggest, strictly capacitive loads are difficult to find at high frequencies. The only load we know of that is capacitive at high frequencies is a Liquid Crystal Display (LCD). In this instance, the intersection of the row and column lines causes many capacitances to be distributed along the line, and because of numerous parallel lines the inductance tends to be low, giving loads upwards of 1000 pF without large amounts of inductance.

Although pure capacitive loads are rare at high frequencies, this does not mean that we can ignore them. Capacitive reactance can exist over narrow frequency ranges, and we must ensure that our amplifier does not oscillate in these ranges.

2.0 Capacitive Loads are Hard
Generally, an op-amp has no problem driving resistive or inductive loads. Of course, this statement needs to be qualified as to the size of the load, but the point is that both kinds of loads do not degrade the phase margin of the amplifier. Capacitive loads, on the other hand, do reduce an amplifier's phase margin, and in severe cases can cause the op-amp to oscillate.

Op-Amp Output Resistance
To see how various loads affect the phase margin, we can model the open-loop output impedance of an op-amp as the resistance $R_o$. Shown in Figure 2.1, $R_o$ forms a divider with the load $Z_L$, and the output $V_o$ goes to the feedback network $R_F$ and $R_G$. If the phase lag of $V_o$ increased due to the $R_oZ_L$ divider, the phase margin around the loop diminishes and peaking, even oscillation, will occur.

First, if $Z_L$ is resistive, then there is no phase lag and the phase margin is preserved. If $Z_L$ is inductive, then $V_o$ gets a phase lead and the phase margin is increased! Finally, if $Z_L$ is capacitive then we do get a phase lag and the amplifier will peak due to this load. The severity of this problem increases with high speed op-amps, as the example below illustrates.

Suppose that we have a 100 MHz amplifier with 45° of phase margin. Let $R_o = 50 \Omega$ and $Z_L = 15 \text{ pF}$, then this network has a cutoff frequency $f_c$ of 212 MHz. At 100 MHz, this network provides 25° of phase lag and thus reduces the phase margin to 20°. Severe peaking will result in the frequency response. The loss of phase margin due to a capacitive load is given by:

$$\Delta PM = \tan^{-1} \frac{f_o}{f_c}$$
where \( f_u \) is the op-amp's unity gain frequency, and \( f_c \) is the cutoff frequency of the \( R_oC_L \) network. Thus we see that for high frequency op-amps, even a small capacitive load can cause a large reduction in the phase margin.

**Op-Amp Output Inductance**

Another way to understand an op-amp's sensitivity to capacitive loads is to look at its closed-loop output impedance more closely. As an example, consider the output impedance vs frequency curve of the EL2044, reproduced in Figure 2.2. We see that beyond about 200 kHz, the output impedance actually looks inductive, and this would resonate with a capacitive load! To see why an op-amp's output impedance looks inductive, consider the circuit in Figure 2.3, where we have an op-amp with open loop gain \( A(s) \) and some general feedback network with gain \( \beta \). The transfer function of this circuit is given by:

\[
H(s) = \frac{A(s)}{1 + A(s)\beta}
\]

If the loop transmission \( A(s)\beta \) is large, then \( H(s) \approx \frac{1}{\beta} \), and we arrive at one of the important results of negative feedback: the system's gain depends largely on the feedback network and not on the op-amp itself. Similarly, the system's output impedance is given by:

\[
Z_{OUT} = \frac{R_o}{1 + A(s)\beta}
\]

where \( R_o \) is the op-amp's open loop output resistance. Thus for large values of loop transmission, negative feedback drives the output impedance to some low value. As frequency increases, however, the magnitude of \( A(s) \) rolls off, reducing the loop transmission and raising \( Z_{OUT} \). Eventually, at frequencies where \( A(s)\beta \ll 1 \), \( Z_{OUT} \) asymptotes to the output impedance of the op-amp output stage.

**Output Stage Superinductance**

Beyond the system level explanations given above, we can gain understanding into the problem by looking at the op-amp at the transistor level. In any op-amp we have an output stage that buffers the gain stage from the external load. The emitter follower is often used for this purpose, so we will consider the follower's output impedance under different conditions. Figure 2.4 shows the general circuit. At low frequencies we can find the output impedance using the reflection rule:

\[
R_{OUT} = \frac{R}{\beta + 1}
\]
At higher frequencies, however, we cannot neglect the frequency dependence of $\beta$. If we model $\beta$ as a single-pole system with DC gain $\beta_0$ and unity gain crossing $w_u$, then the output impedance becomes the following:

$$Z_{OUT} \approx \frac{R}{\beta_0 \left( 1 + \frac{f_\beta_0}{f_T} \right)} = \frac{R}{\beta_0} \left( 1 + \frac{f_\beta_0}{f_T} \right) = \frac{R}{\beta_0} + j \frac{R}{f_T}$$

Finally, when the source is inductive, the output impedance has a negative real component. This negative impedance has no reactive phase, but its magnitude increases as the frequency squared; we will name this component a "super-inductor". If the sum of series resistance in a network is negative and all the reactances cancel, then the network will oscillate. Thus the seemingly benign emitter follower really misbehaves if we drive it with an inductive source!

So where do we get an inductive source from within an op-amp? The Darlington connection is one possibility. In this configuration, an emitter follower drives another emitter follower. The first follower transforms its base resistance into an output inductance, and the second follower transforms this inductance into an output super-inductance. The effect is the same for a NPN follower driving a PNP, or vice versa. Since base resistance tends to be larger for IC transistors than for discrete transistors, super-inductance is very much an issue for monolithic amplifiers. An output stage with this topology is shown in Figure 2.5, first used in the LH0002 buffer amplifier. Most integrated amplifiers built with a complementary bipolar process also use this output stage, and so a real amplifier’s output impedance is the sum of resistive, inductive, and super-inductive components. If a capacitive load resonates with the inductance at a frequency where the super-inductance is greater than the real resistance, oscillations will occur in the output stage independent of loop characteristics.

The next transformation is for a capacitive source, which results in a resistive and capacitive output impedance.

Figure 2.3. Block Diagram of General Feedback System
Figure 2.4. Impedance Transformations for an Emitter Follower with Various Source Impedances
3.0 Possible Solutions

Like death and taxes, it is inevitable that we will have to drive some form of capacitance. Unlike death and taxes, techniques exist to deal with capacitive loads to some degree. We will present some of these techniques in the following sections.

Internal Compensation

As we saw earlier, heavy capacitive loads can reduce the phase margin of an amplifier, and thus cause the amplifier response to peak. However, if we can lower the dominant pole of the amplifier such that the phase margin is restored, then the overall amplifier response should not peak, although the bandwidth will also be reduced. Is there such a way of sensing the amount of capacitive load and adjusting the dominant pole appropriately? The answer is yes, and the solution can be seen in Figure 3.1, where a capacitor $C_c$ has been connected between the gain stage and output of an op-amp.

First, consider a light load on the output (high $R_L$, low $C_L$). Driving this load, the two voltages $V_{OUT}$ and $V_{HIZ}$ should track each other closely, and no current will flow thru the $R_cC_c$ combination. The compensation network does no work in this case, and we get the normal amplifier response as given by Curve A in Figure 3.2. Now suppose we raise $C_L$ to some high value. The voltage $V_{OUT}$ will not follow $V_{HIZ}$ as closely, and current begins to flow in the $R_cC_c$ network.

![Figure 2.5. LH0002 Output Stage Topology](image)

![Figure 3.1. Compensation Scheme To Make Op-Amps More Tolerant of Capacitive Loads](image)
This in effect puts part of \( C_c \) on the gain node, thus lowering the bandwidth of the amplifier. Curve B in Figure 3.2 shows what the response may look like in this case. On the other hand, Curve C shows what will happen if we did not use the compensation network to drive a large \( C_L \); although we retain the bandwidth, severe peaking occurs.

This technique does have its drawback: the bandwidth reduces for heavy loads in general. Thus, the bandwidth lowers for heavy resistive loading as well, which is an undesirable trait. In addition, this technique degrades the RF linearity of the amplifier, ruining such performance parameters as differential gain and phase.

**External Compensation—Series Resistor**

To avoid sacrificing performance, most of Elantec’s op-amps are not heavily compensated for capacitive loads. The use of external compensation networks may be required to optimize certain applications. Figure 3.3 shows one such network, where we have inserted a series resistor with the op-amp’s output. The stabilizing effect of this resistor can be thought of in two ways. One is that \( R_{\text{SERIES}} \) serves to isolate the op-amp output and feedback network from the capacitive load. The other way to think about it is to recall the superinductor concept introduced earlier. Since the output stage presents a negative resistance over certain frequencies, adding enough series resistance would cancel this negative resistance and prevent oscillation.

The required amount of series resistance depends on the part used, but values of 5Ω to 15Ω is usually sufficient to prevent local resonances. The disadvantage of this technique is a reduction in gain accuracy, and extra distortion when driving nonlinear loads.

**External Compensation—The Snubber**

Another way to stabilize an op-amp driving a capacitive load is the use of a snubber, as shown in Figure 3.4. To see how a snubber can reduce peaking, consider the 300 MHz \( f_T \) transistor presented in Section 2. For that example, the output inductance of the emitter follower was shown to be 100 nH. With a light resistive load \( R_L = 1 \) kΩ and moderate capacitive load \( C_L = 50 \) pF, the circuit resonates at 70 MHz with a \( Q \) given by:

\[
Q = \frac{R_L}{\sqrt{C_L L}}
\]
In this case, Q works out to be about 22, giving us severe peaking in the frequency response. However, with a load of 150Ω, the Q reduces to 3. Thus the extra stability gained with a heavy load resistor is desirable, but we may be wasting DC load current with this approach. A way around this is to insert a capacitor in series with the resistor, resulting in a snubber.

There are various ways to determine appropriate values for $R_{SNUB}$ and $C_{SNUB}$, one of which is presented in [2]. We will describe an alternative method here. First, operate the amplifier as in the intended application and look at its frequency response on a network analyzer. Find the frequency at which the peak occurs, and denote that as $f_p$. Next, try loading the amplifier with different load resistances until the peaking reduces to a satisfactory level; this value will be $R_{SNUB}$. Finally, we need a capacitor that will make the snubber look resistive at the frequency of the peak. A rough guideline is to make the snubber zero frequency 3 times lower than $f_p$, resulting in the following design equation:

$$C_{SNUB} = \frac{3}{2\pi \cdot f_p \cdot R_{SNUB}}$$

Note that as opposed to the series resistor method, the use of a snubber does not degrade the gain accuracy or cause extra distortion when driving a nonlinear load.

**Unterminated Coaxial Lines**

As we may have hinted earlier, unterminated coaxial lines mean trouble. The simple remedy for this is to terminate the line in its characteristic impedance, and the cable will look like a stable resistive load to the driving amplifier.

In certain cases the cable termination may be unknown, or it may not be under our control at all times. A good example of this is in ATE systems, where an amplifier drives a signal through a coaxial cable to a test pin. However, when a device under test is not plugged in, the test pin is left unterminated, and so the amplifier is driving into an open cable. Figure 3.5 shows how we can use back-matching to solve this problem. In back-matching, we insert a resistor $R_{BM}$ equal to the cable’s characteristic impedance between the amplifier and the cable. $R_{BM}$ serves to isolate the amplifier from the cable, the impedance of which could wildly vary with frequency. Also, since $R_{BM}$ terminates the cable at the source end, reflected signals are absorbed in $R_{BM}$, preventing multiple reflections from occurring.

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**Figure 3.4. The Snubber**

**Figure 3.5. Backmatching**
4.0 Summary

High frequency op-amps are sensitive to capacitive loads due to the loss of phase margin in driving these loads. In addition, the op-amp output stage can introduce its own resonance, further complicating the stability issue. These problems can introduce severe peaking in the frequency response or excessive ringing in the transient response. Some recent op-amp designs have incorporated an internal compensation network for capacitive loads. Such op-amps, however, sacrifice bandwidth and RF linearity in return for foolproof usage. For the best performance, amplifiers without the internal compensation network should be used in conjunction with a snubber when necessary. Proper bypassing and board layout have not been stressed in this application note, but they are equally important to the well-being of a high speed op-amp.

References

Current Boosted and DC Stabilized Half Bridge Driver

by Les Mills

Following are two applications notes for the EL7661 half bridge driver.

1. The current boosted half bridge driver offers the control functions of the EL7661 with enhanced drive capability. For example an application with $V_S = 16V$, a 25 ns turn on time and a 3000 pF load would require $I_{PK} = (V_S + V_{GS}) \cdot C/T_{ON} = (16 + 10) \cdot 3000 \text{ pF}/25 \text{ ns} = 3.12\text{A}$ peak current from the driver. Since the EL7761 specifies $I_{PK} = 1\text{A}$ typical, the output requires current boosting to achieve the desired turn on time. This circuit is also useful in applications where the switching time is less stringent or the load is lighter but the output is required to swing over a greater range due to higher supplies voltages.

![Figure 1. EL7661 Half Bridge Driver with Output Current Boost](image-url)
2. DC stabilization of the half bridge driver is achieved by charge pumping the high side supply storage capacitor while the output is in the high state. This keeps the top half of the circuit (VDD to Lx) biased at 12V when a 12V Zener is used as shown. The Zener should be 15V or less. The EL7232 was selected for the oscillator since its output must swing between GND and the 16V supply and provide a minimum of 10 mA, the supply current of the EL7761. The EL7232 is capable of 1.5A peak. Any driver providing 30 mA, swinging between GND and the 16V supply would also be suitable.

Figure 2. EL7661 Half Bridge Driver DC Stabilized with Output Current Boost
25 kHz Electronic Ballast Using The EL7981 Delay Driver
by Bruce Rosenthal

Introduction
Electronic ballasts are rapidly gaining market acceptance, as ballast prices drop, electrical rates increase, and performance improves. Their primary advantages are: (1) the elimination of flicker, and noise (hum), (2) increased efficiency resulting in a cost advantage, and (3) reduces size and weight. The EL7981 is particularly well suited for this application by using the programmable delay and high current drive features.

System Operation
The ballast, in many respects, resembles an OFF-LINE Switch-Mode Power Supply. The 120 VAC line is rectified and doubled, developing ≈ 300 VDC rail-to-rail. When the intensity switch is set to "Low", the doubler is eliminated, and 150 VDC is produced. A "half bridge" configuration, using (2) Power MOSFET's drives an LC resonant circuit, with sufficient "Q" to develop the necessary starting voltage. The resulting current and voltage to the lamp are sinusoidal. Isolated drive to the FET's is provided with a transformer coupled from EL7981 Dual Delay Driver. The delay function allows for the "Recovery Time" of the parasitic diodes in the Power Mosfet's. A 555 timer generates the desired clock frequency. The clock can be tuned to the resonant frequency of the series L-C network. For tutorial reasons, auxiliary power for the clock and driver were supplied externally, however, in practice a simple charge-pump can be used to develop the 10V supply.

Lamp
The "F40" 40 watt, 48" flourescent lamp was selected for its popularity, and low cost. Above 20 kHz, these flourescent lamps behave like a 300Ω resistor because the plasma is maintained. The "striking" voltage for a cold tube is around 400V, however, this can be reduced by supplying current to the starter filament. Additional lamps can be added, but require separate L-C networks. 25 kHz operation was chosen, because it's above the audible range, yet not so high, that switching losses would be of concern. Increased lamp life has been reported by operating at these frequencies compared to 50 Hz–60 Hz.

EL7981
The EL7981 Dual Delay Driver generates a programmable delay to the rising edge of the output waveforms. Each output has a nominal "ON" resistance of 5Ω, and can source and sink 1A. With \( R_{SET} = 300 \text{ kΩ} \), the delay is about 1.5 \( \mu s \), which provides sufficient time for the parasitic diodes in the FET's to recover. The strong output devices are suitable for driving the "Gate" transformer directly. The resulting gate drive waveform has (3) distinct levels: \(-10V, 0V, +10V\).

Magnetics
The two magnetic components of the Ballast are (1) the gate transformer, and (2) the output resonating inductor. The output inductor is rated at 1.8 mH (Magnetic Circuit Elements Inc. #OC25BL25). The gate transformer is wound 1:1:1 and is tightly coupled to provide fast switching. (Magnetic Circuit Elements Inc. #0-1853T1). For further information on these components, contact John Conklin at Magnetic Circuit Elements (408) 757-8752.

8-55
25 kHz Electronic Ballast Using The EL7981 Delay Driver

Electronic Ballast (Power Mesh)

- VARISTOR
- 120 VAC
- 0.047 μF, 400V
- HIGH
- 100 μF, 250V
- LOW
- 1A/400V
- FLOURESCENT LAMP
- 1.8 mH
- 0.047 μF, 400V
- 0.01 μF, 600V
- 1A/400V
- Q1 AND Q2 - N CHANNEL POWER MOSFETS 500V/3Ω
- PULSE TRANSFORMER

Electronic Ballast (Gate Drive Circuit)

- 555 TIMER
- 1000 pF
- 10k
- 2500 pF
- 0.1 μF
- EL7981
- 4.7 Ω
- A
- TO PULSE TRANSFORMER
- 4.7 Ω
- B
Temperature Compensation for the EL4581C and EL4583C
by Chris Siu

The EL4581C and EL4583C are sync separators with on-board filters. It has been found that over temperature, the propagation delay of composite sync varies due to this filter. For example, in the 25°C to 85°C range, the delay varies by about 20 ns. The reason for this is that as temperature increases, the $g_m$ of transistors in the filter stage drops, causing the filter bandwidth and delay to change. A solution for this is to introduce a PTAT (Proportional To Absolute Temperature) bias current for this stage, thus maintaining a constant $g_m$ as temperature increases.

For the EL4581C, the filter bias current is set by the resistor $R_{SET}$ on pin 6. We replace this with a resistor and two diodes in series as shown in Figure 1 below. Since the diode voltage has a negative temperature coefficient, this would increase the bias current thru $R_{SET}$ as temperature rises. Shown in Table 1 below are the propagation delays over temperature with and without compensation. With compensation, we achieved a threefold improvement over the uncompensated case.

Table 1. Propagation Delays for the EL4581C

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Delay w/o Comp (ns)</th>
<th>Delay with Comp (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>233</td>
<td>232</td>
</tr>
<tr>
<td>50</td>
<td>240</td>
<td>228</td>
</tr>
<tr>
<td>85</td>
<td>253</td>
<td>226</td>
</tr>
</tbody>
</table>

Note: Propagation delay is defined as the time from the rising edge of the input horizontal sync to the rising edge of the CSYNC output.

If we look more closely at the above results, however, we see that the circuit is over-compensating, causing the delay to decrease with temperature. The two diodes actually provided too much of a PTAT current, whereas a single diode does not create enough PTAT current. Thus, the ideal compensation would provide about one and a half diodes of temperature coefficient.

Shown in Figure 2 below is a circuit which does the job; it is a $V_{BE}$ multiplier with a multiplication factor of about 1.6. Measured on the scope, there is no perceivable delay variations in the 25°C to 85°C temperature range. Since the measurement accuracy is limited by the waveform jitter, the delay may have actually changed by 1 ns to 2 ns, but this should not present a problem for most applications.

![Figure 1. EL4581C Compensation Network](image1)

![Figure 2. Improved Compensation Network](image2)
Temperature Compensation for the EL4581C and EL4583C

For the EL4583C, however, the filter bias current is not controlled by \( R_{\text{SET}} \), but by the Filter Cutoff resistor \( RF \) on pin 1. Moreover, since there is only about 0.5V on this pin at room temperature, putting a diode in series with \( RF \) would not work in this case. A compensation network which circumvents this problem is shown in Figure 3 below. At room temperature, the voltage at node A would be about 0.7V due to the diode, and since node A is higher than node B, \( R_2 \) would inject a current into \( RF \), thus requiring a smaller current from pin 1 than would otherwise. As temperature rises, the voltage at node A would decrease, such that \( R_2 \) would take current away from \( RF \) and requiring pin 1 to supply more current. We have thus achieved the desired PTAT effect on pin 1 with this arrangement, and the results using this network is shown in Table 2.

Table 2. Propagation Delays for EL4583C

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Delay w/o Comp (ns)</th>
<th>Delay with Comp (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>243</td>
<td>247</td>
</tr>
<tr>
<td>50</td>
<td>250</td>
<td>244</td>
</tr>
<tr>
<td>85</td>
<td>261</td>
<td>246</td>
</tr>
</tbody>
</table>

![Figure 3. EL4583C Compensation Network](image)

We can see that with these compensation schemes, we obtained a drastic reduction in propagation delay drifts over temperature. For comparison the delay drift of the LM1881 is also shown.
Thermal Design Considerations—EL75XX
by Vijay Soman

1.0 Introduction
Elantec's EL7560C/EL7561C/EL7556C series of voltage regulators are highly integrated, simple to use and the most effective switching mode designs to power microprocessors such as Intel Corporation's *Pentium® Pro, and *Pentium. The EL7560C/EL7561C is designed for classes of processors such as the Pentium Pro. EL7556C is designed primarily for Pentium class desktop models.

These devices are packaged in a 28-pin power SO package (28 PSOP 2) developed by Amkor Corporation. The 28 PSOP 2 is a 28-lead surface mount package with 50 mil lead centers. It includes a specially designed copper slug on which the die is attached. The copper slug provides the excellent power dissipation capability required for these devices. Two versions, "Slug up" and "Slug down", are available for various board mounting and heatsink options. This application note describes the various package and heatsink combinations, which can be used with the EL75XX series.

2.0 Typical Applications Power Requirement
The typical power applications requirement for microprocessors is either a VRM (Voltage Regulator Module) or a direct mother board solution, both options operate under certain power dissipation, environmental, physical, and, of course, cost constraints. Table 1, below, summarizes the majority of typical applications requirements.

Several other variations in ambient temperature and airflow conditions may exist in practice, depending upon the user's board layout and system configurations.

3.0 Structure and Characteristics of the 28 PSOP 2
Figure 1 illustrates the structure of the Amkor PSOP 2 package. The copper slug is 535 x 170 mils in dimension and its thickness is optimized in order to arrive at a good compromise between biggest size possible for maximum thermal performance and the smallest foot print for the package. The die can either be soft soldered to the slug or attached using a thermally conductive epoxy.

<table>
<thead>
<tr>
<th>Application</th>
<th>Thermal Requirement</th>
<th>Typical Environment</th>
<th>Thermal Resistance Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>VRM-Pentium Pro</td>
<td>Pdiss = 3.4W, Tj = 105°C</td>
<td>T_A = 60°C, 100 LFM</td>
<td>$\theta_{JX} = 13°C/W$</td>
</tr>
<tr>
<td>VRM-Pentium P54/55</td>
<td>Pdiss = 2.4W, Tj = 105°C</td>
<td>T_A = 50°C, 100 LFM</td>
<td>$\theta_{JX} = 23°C/W$</td>
</tr>
<tr>
<td>Laptop-Pentium P54</td>
<td>Pdiss = 1.6W, Tj = 105°C</td>
<td>T_A = 50°C, No Airflow</td>
<td>$\theta_{JX} = 34.3 C/W$</td>
</tr>
</tbody>
</table>

*Pentium® Pro and Pentium are registered trademarks of Intel Corporation.
The slug provides low thermal resistance from the die to the external heatsink and also through the leads. At the same time, it provides a large thermal capacitance to absorb power peaks during switching. Thermal resistance ($\theta_{JC}$—junction to case) for a typical 100 x 100 mil die is 4–5°C/W. The electrical lead resistance is in the range (5) mmhos; inductance is typically (2 nH) per lead and capacitance is about 1 pF. The package comes in two different lead stand-offs: normal stand-off is 9 mils and low stand-off is 2 mils. The two board mounting options are shown in Figure 2.

### 4.0 Components of Thermal Resistance and Heat Dissipation

Long term reliability of the semiconductor device is enhanced by keeping the junction temperature ($T_J$) as low as possible consistent with the given application. (See Elantec “Reliability and the Electronic Engineer” Tutorial #1.)

$T_J$—Junction temperature is a function of the amount of heat dissipated, the thermal resistance between the junction and the ambient air, and the ambient air temperature.

---

**Figure 1.28 PSOP 2 Structure**

<table>
<thead>
<tr>
<th>PSOP 2—Exposed Slug with Coupled Leads</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polyimide Tape</td>
</tr>
<tr>
<td>Gold Wire</td>
</tr>
<tr>
<td>Die</td>
</tr>
<tr>
<td>Exposed Slug</td>
</tr>
<tr>
<td>Leadframe</td>
</tr>
</tbody>
</table>

**Figure 2.28 PSOP 2 Board Mounting Options**

- **PowerSOP2:**
  - Direct slug solder to PCB
  - Low stand-off (4 mils)

- **PowerSOP2:**
  - Die down
  - Slug exposed to ambient
Integrated thermal resistance ($\theta_{IT}$) is the sum of the following individual thermal resistances.

$\theta_{JC}$—Thermal resistance from junction to case (die size, d/a, package dependent).

$\theta_{CH}$—Thermal resistance from case to heatsink (interface—package to heatsink dependent).

$\theta_{HA}$—Thermal resistance from heatsink to ambient (heatsink dependent).

Thus,

$$\theta_{IT} = \theta_{JC} + \theta_{CH} + \theta_{HA} \text{ (C/W)}$$

As stated above in section 2, the thermal resistance required is the total integrated thermal resistance $\theta_{IT}$ under the "In Situ" applications condition.

$\theta_{JC}$—Thermal resistance from junction to case depends on the die size, Cu slug size, the die attach material and the lead frame. In the case of PSOP 2 package, almost all the heat from the die is conducted through the Cu slug and very little through the leads.

Figure 4 shows the relationship between $\theta_{JC}$ and die size for a given package and die attach material.

$\theta_{CH}$—Thermal resistance from case to heatsink is dependent upon the thermal properties of the interface used to attach the heatsink to the copper slug of the package. Various types of heat conducting pads, thermal greases and thermal epoxy bonding materials are available from several manufacturers. Table 2 shows estimated values of $\theta_{CH}$ for several types of epoxy bonding materials.

$\theta_{HA}$—Thermal resistance from heatsink to ambient is a function of the conduction through heatsink material to the dissipating surface area; convection (natural or forced); and radiation from the heatsink surface area. Different designs of the sizes of heatsinks are available to achieve maximum conduction and convection. Forced air can be used to improve convection and black anodizing can improve heat dissipation through radiation.

5.0 Thermal Resistance—28 PSOP 2

The 28PSOP 2 is available in two versions—the "Slug down" in a low stand-off version (2 mils) and a "Slug up" version with a standard stand-off of 9 mils. The slug down version is suitable for direct mounting onto the PCB by using surface mount solder technique. The heat dissipating copper area on the circuit board can be configured in various shapes and sizes depending upon the particular application. Figure 3 shows a typical configuration for heat dissipating copper clad. Thermal resistance measurements for the slug down version are listed in Table 3. Medium power dissipations of up to 2W are easily obtainable in practice with this configuration. The slug up version offers more heat sinking options. One of the most beneficial options is to epoxy bond a suitable heatsink to the package slug as shown in Figure 5 and Figure 6.

Another heat sinking option is to use a mounting clip to secure the heatsink to the PCB, as shown in Figure 7 adding mechanical strength against shock and vibration. Heatsink arrangements shown in Figure 5 and Figure 6 offer very effective heat dissipation under forced air condition of 100 LFM–200 LFM in a typical PC system application. (See Figure 8 for effect of forced air convection on thermal resistance.) The methods shown in Figure 5 and Figure 6 allow power dissipations in the 2W–9W range, as shown in Table 3. Figure 9 graphically summarizes the power dissipation capability of the 28 PSOP 2.

Figure 3. Typical Footprint for a Heat Dissipating Copper Clad
Figure 4. Thermal Resistance—$\theta_{JC}$ 28PSOP 2

Table 2. Thermally Conductive Bonding Materials

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Type</th>
<th>Thermal Conductivity</th>
<th>Strength Mechanical (Bond Shear)</th>
<th>Thickness Applied</th>
<th>$\theta_{CH}$ $\degree$C/W Thermal Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ablestik</td>
<td>84-1LMIT</td>
<td>4.3 w/mk</td>
<td>6000 psi</td>
<td>2 mils</td>
<td>0.2</td>
</tr>
<tr>
<td>Wakefield</td>
<td>120</td>
<td>0.74 w/mk</td>
<td></td>
<td>2 mils</td>
<td>1.1</td>
</tr>
<tr>
<td>Thermagon (Elastomer)</td>
<td>T-pill 210</td>
<td>6 w/mk</td>
<td></td>
<td>10 mils</td>
<td>0.14</td>
</tr>
<tr>
<td>Wakefield Deltabond</td>
<td>152-B4</td>
<td>0.9 w/mk</td>
<td>2300 psi</td>
<td>2 mils</td>
<td>0.95</td>
</tr>
</tbody>
</table>
Figure 5. PSOP 2 with Wakefield # 8052-60 Heatsink

Figure 6. PSOP 2 with Wakefield Penguin # 658-60A Heatsink

Figure 7. PSOP 2 with Heatsink and a Mounting Clip
Figure 8. Thermal Resistance vs Air Flow—LFM
Figure 9. Power Dissipation vs Thermal Resistance
EL75XX Thermal Design Considerations

Table 3. Power Dissipation Capability of 28 PSOP 2

<table>
<thead>
<tr>
<th>Mounting Condition</th>
<th>Ambient Condition</th>
<th>Thermal Resistance °C/W</th>
<th>Power Dissipation-Watts</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>ΔT 45°C</td>
<td>ΔT 55°C</td>
</tr>
<tr>
<td>I. Slug Up</td>
<td></td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>Package Only</td>
<td>Still Air</td>
<td>52</td>
<td>0.87</td>
</tr>
<tr>
<td>Package + Wakefield H.S. #8052-60</td>
<td>Still Air</td>
<td>25</td>
<td>1.8</td>
</tr>
<tr>
<td>Package + Wakefield H.S. #8052-60</td>
<td>Air Flow 100 LFM</td>
<td>12.9</td>
<td>3.5</td>
</tr>
<tr>
<td>Package + Wakefield H.S. #8052-60</td>
<td>Air Flow 200 LFM</td>
<td>11</td>
<td>4</td>
</tr>
<tr>
<td>Package + Wakefield H.S. Penguin #658-60AB</td>
<td>Air Flow 600 LFM</td>
<td>7.7</td>
<td>5.8</td>
</tr>
</tbody>
</table>

II. Slug Down

| Package Soldered to 3" sq Cu PCB | Still Air | 33.4 | 1.3 | 1.65 | 1.8 | 2.2 |
| Package Soldered to 3" sq Cu PCB | Air Flow 100 LFM | 30   | 1.5 | 1.8  | 2   | 2.5 |

Notes: A—TJ = 105°C, TA = 60°C  
B—TJ = 105°C, TA = 50°C  
C—TJ = 110°C, TA = 50°C  
D—TJ = 125°C, TA = 50°C  

All thermal resistance measurements were done with a thermal die size of 100 x 100 mils. The actual die size of the EL7560/61 is larger than the thermal die therefore, the thermal resistance of the EL7560/61 will be 1-3°C/W lower than the numbers in the table.

Conclusions
Powering of the *Pentium® Pro and *Pentium microprocessors presents a challenge in thermal management. It has been demonstrated that by utilizing special power dissipating capability of the 28 PSOP2 package and an appropriate heatsink, the EL7560C/EL7561C and the EL7556C DC regulators will successfully power Pentium and Pentium® Pro microprocessors. Power dissipations from 2W to 6W can easily be achieved, while keeping the junction temperature as low as 105°C.

Acknowledgments
The Author wishes to thank Ratnaji Arumilli for his work on thermal modeling, Mas Kobashi and Dave Mabrey for their efforts in thermal resistance measurements and also Amkor Ltd for their support in supplying thermal die packaged in PSOP2 packages.

References
1. Reliability and the Electronic Engineer, Tutorial #1—Barry Siegel  
2. Simple Method of Characterizing Hybrid Package Thermal Impedance—Steve Ott and Barry Siegel, Hybrid Circuits Technology, June 1990  
3. Measuring the Thermal Resistance of Power Surface Mount Packages—Barry Harvey  
An Improved Peak Detector
by Tamara I. Ahrens

Diodes have long served as adequate rectifiers despite necessarily large input voltages and poor accuracy. The most common configuration for a simple diode peak detector (Figure 1) provides a mediocre 10% error for very large input voltages (Figure 2). If the diode is linearized, the necessary input voltage is only reduced to 1V peak for the same 10% error (Figure 2). However, development of high frequency op amps allows feedback circuitry to provide better accuracy and more sensitivity at the input. With feedback (Figure 3), peak detection is feasible at input voltages as small as 50 mVRms.

Function of Feedback Diode Circuitry
The input stage consists of a high frequency op amp whose output is fed into both a diode (D1), which functions similar to the diode of a simple peak detector, and a clamping network, which limits the negative output swing of the forward op amp. The output of the diode (D1) is connected to the storage capacitor and is also fed back to the input through a buffer. A storage capacitor of 0.1 µF is recommended for peak detection at audio frequencies. A small resistance is shown in series with the storage capacitor to isolate it from the feedback loop. The smallest functional value is recommended for minimal peaking and maximum bandwidth; 10Ω is suggested. A bleed current is necessary to allow the output to relax for a smaller input or in the absence of an input. 20 µA, small enough to avoid deteriorating the output value substantially, but large enough to dominate the bias current of the feedback buffer, was chosen. The output of the buffer is fed back to the negative input of the forward op amp through a resistor. This resistor buffers the emitter of the pnp transistor of the clamping network from the low impedance at the output of the buffer. Please note: a compensation capacitor on the forward op amp may be a necessary addition to ensure stability and the output of the entire peak detection circuit must be buffered to prevent a disturbance in performance.

Clamping Network
The diode (D2) of the clamping network is always held on by the current source. For voltage signals greater than the peak held at the output, the forward, rectifying diode (D1) is conducting, the output voltage is raised to match the input voltage, the buffer feeds that voltage back around to the negative input of the forward op amp, and the emitter of the pnp transistor is held at the same voltage as its base, keeping it off and eliminating the second feedback loop.

For voltage signals less than the peak held at the output, the rectifying diode (D1) is off. The emitter of the pnp transistor is set as high as the output voltage by the buffer through the 1 kΩ resistor while the base is pulled down by the output of the forward op amp through the feedback diode (D2). The 270Ω resistor adds a 0.3V bias to the base of the transistor producing a charge-discharge current ratio of 10,000:1. When the transistor turns on, a crude unity gain feedback loop is completed through the clamping network (from the output voltage, down a diode drop and up the base-emitter diode of the transistor, to the input voltage) and a voltage drop builds across the 1 kΩ resistor. This clamping action minimizes the recovery time of the circuit. Since the clamping network works like a unity gain buffer for inputs less than the peak voltage, the output needs to slew less than one diode drop to turn on the rectifying diode (D1) for inputs greater than the peak voltage. In this manner, the clamping network prevents the forward op amp from exhibiting open loop behavior and railing negative for inputs less than the peak voltage. This greatly reduces the slew rate necessary to achieve a desired bandwidth.

Amplitude Considerations
This circuit has the ability to function with amplitudes 30 times smaller than a simple diode peak detector. The EL2244C has an open loop gain of 60 dB, raising smaller input signals
enough to be detectable by the diode. The smallest amplitudes recoverable will be determined by the noise amplified within the circuit. For the given circuit, this limit is approximately 30 mVrms input voltage. The largest amplitudes allowable will be determined by the input constraints of the op amp. For the EL2244C at ±5V supplies, the maximum input range is approximately ±3.5V.

**Frequency Considerations**

If 5% errors can be tolerated, this circuit has a bandwidth of 100 kHz (Figure 4), making it ideal for audio applications. A great deal of small signal bandwidth and large slew rates are necessary to swing quickly through the dead zone at the output of the first op amp and these quantities limit circuit performance.

Thus, for a handful of inexpensive parts, a drastic improvement can be made in the performance of a peak detector over that of a simple diode. With the utilization of modern, high-speed op amps, the feedback diode peak detector offers almost two decades of input voltage range improvement while maintaining functionality into the megahertz range.

Fine Harmonic Distortion Measurements in the Megahertz Range
by Barry Harvey

Harmonic distortion measurements of amplifiers is easily accomplished using a commercial test set which includes a low-distortion oscillator. These units work only up to 100 kHz or less; at higher frequencies, a low-distortion oscillator and spectrum analyzer are employed. Unfortunately, commercial sinewave oscillators have no better than −56 dBc harmonic content (0.16%), and spectrum analyzers offer no better than −72 dBc (0.025%) internal distortion levels. This author had to test amplifier IC’s to −80 dBc (0.01%) levels at 2 MHz, and couldn’t buy general-purpose lab equipment to do the job at any price. This article shows the circuits made to do the job.

Referring to Figure 1, we will make a clean sinewave source to drive the Device Under Test (DUT). Its output will pass through a fundamental reject filter so that the harmonics may be amplified without overload from the high-amplitude fundamental. Having stripped most of the fundamental away, the reject filter's output may be viewed on a spectrum analyzer or passed on to individual harmonic measurement sections for fast automated testing.

The sinewave applied to the DUT must have less than −80 dBc distortion. This is pretty hard to accomplish, since we will generate it with active semiconductors whose distortion levels are too high. About the best unfiltered output distortion level we can obtain from transistor amplifiers is −60 dBc (ref. 1). We cannot use an active filter to clean up the harmonics further, because again no amplifiers can be used that will not add more distortion. A simple passive filter is used to bring distortion below −80 dBc.

Figure 2 shows the oscillator schematic. It produces 1 VMRS into a 500Ω load. Note that the simple passive network is not a fancy N-th-order filter of some precise characteristic; it is simply a series tuned circuit and a parallel trap at the output, both resonant at the oscillator frequency. The Q's of the circuits are intentionally low, around 10 with the 500Ω load, to make them non-critical with respect to tuning. Two ranks of tuned circuit give a harmonic rejection of roughly Q², more than enough to achieve the desired output distortion level. The loss of the filter does not affect the output level; it is actively stabilized, even if a 50Ω load is used.

The EL4451C in Figure 2 is a variable-gain amplifier. It has two inputs: REF, which has a low distortion gain of 1 to the output; and V_IN, which is a variable-gain input controlled by the Gain inputs. A crystal is connected from the output back to the REF input, loaded by 330.0 + 160.0. The crystal has about 150Ω series impedance at resonance, so the voltage division through the crystal prevents sustained oscillation. The extra gain required for oscillation comes from the V_IN path, and if the Gain input level is sufficient the EL4451C will oscillate.

This oscillation will grow uncontrollably until clipping occurs, so an EL4450C is used as an amplitude stabilizer. The EL4450C is a four-quadrant multiplier, and its X- and Y-inputs are wired to the filtered oscillator output. In the EL4450C's multiplier is developed a level proportional to \( V_{OUT}^2 \), and this is compared to a reference level at the REF input. The FB terminal is connected to DC ground, but it also is connected to C3 to form a pseudo-integrator with the output amplifier. Thus, the output is approximately the integral of the RMS of the oscillator output level minus the DC reference. If the oscillator output is greater than the reference, the EL4450C output ramps positive and reduces the EL4451C gain via its Gain-terminal. If the oscillator output is less than the reference, the integrator output ramps negative and raises the EL4451C gain. Thus the EL4450C acts as a level detector and servo loop integrator. Amplitude modulation noise is extremely low with this servo.

The pseudo-integrator in the EL4450C output circuit includes a zero between C3 and its 10K resistor. This is cancelled with an additional pole from C4 and the parallel of its 20K resistors.
The crystal can be replaced by a series LC circuit. It is very difficult to make this circuit provide widely variable output frequency, but it can easily be switched with rotary switches and multiple crystals and output filters. Both input and output terminals of the filter must be switched. Other load impedances can be driven, but the output filter must be redesigned. Generally, at resonance \( X_{L1} = X_{C1} = R_L * Q \) and \( X_{L2} = X_{C2} = R_L / Q \).

Figure 3 shows the fundamental reject circuitry. Because in the author's test setup the DUT produces a 9 VRMS fundamental amplitude, the L3-C3-L4-C4 filter attenuates it immediately so that the first amplifier is not overloaded. The EL2074C is a very low distortion wideband amplifier, but we still have to control the levels. The amplifiers provide a total gain of 100 for the harmonics to the spectrum analyzer or harmonic select sections, and each stage includes a fundamental-reject filter.

The output of the first amplifier still has an attenuated fundamental level of around 900 mVRMS, so the second filter knocks the fundamental down further to around 9 mVRMS. The final output has a fundamental down by about 80 dB, and harmonics up by 40 dB, easily viewed on a spectrum analyzer. Calibration is simple: just provide an input at some frequency greater than the fundamental and find the gain with an oscilloscope, or better yet use a network analyzer to measure gain over frequency. Set amplitudes so that no more than 1 VRMS is outputted.

SW1 is used to select high or low gain for the harmonic select and measure sections, due to their restricted dynamic ranges. A switch can be used, but the author used a relay. To preserve distortion and noise quality, semiconductor analog switches or multiplexed-amplifiers should not be used.

The EL2120C amplifier buffers the final filter and provides a gain of +2 to compensate for the loss of the back-matched 50Ω load termination.

Figure 4 shows a harmonic select channel. The output from SW1 routes through the L9-C9-L10-C10 network which passes the desired harmonic frequency. The EL2074C amplifies this harmonic and drives another filter also tuned to the desired harmonic. This highly selected harmonic is passed a fast comparator and then to the EL4450C four-quadrant multiplier. The multiplier's input signals are the harmonic and a clipped version of the harmonic. This clipped signal is the same as the sign of the harmonic, so the multiplier output is the harmonic times its own sign, or the absolute value of the harmonic. A simple RC filter passes the DC component, which is a linear measure of the selected harmonic. The 180Ω–10 pF components provide a simple time delay equal to that of the comparator to balance the phase of the multiplier inputs, improving accuracy at higher frequencies.

The design of L's and C's in the harmonic select section is similar to that of the other sections, where at the harmonic frequency \( X_{L9} = X_{C9} = X_{L11} = X_{C11} = 250Ω * Q \) and \( X_{L10} = X_{C10} = X_{L12} = X_{C12} = 250Ω / Q \).

Unless 5% L's and C's are used and parasitic capacitances are kept to less than 2 pF, the networks will have to be tuned. The author used a network analyzer, measuring the output of an amplifier following a tuned circuit so as not to load and de-tune it. Either the inductor or the capacitor can be adjusted; if the capacitance value is less than 100 pF a variable trimmer can be used in parallel with a fixed capacitor, otherwise a slug-tuned variable inductor can be used. It seems archaic to have to adjust LC circuits in this era of IC's, but they do allow the lowest distortion measurements.

It is completely practical to use multiple-pole rotary switches to allow different operating frequencies, seven poles being adequate for the oscillator and fundamental reject section. A pole can be saved by wiring all crystals together at the EL4451C output. The filters should be kept as physically separate as possible.

This project provided a lab test device better than commercial units. It does require assembly and adjustment, but it produces solid results.

References.
Fundamental Reject Filters and Amplifiers

Harmonic Select and Measure Circuit at $2f_0$

Harmonic Select and Measure Circuit at $3f_0$

Figure 1. Block Diagram of Distortion Measurement System
Figure 2. Low-Distortion Oscillator
Input from DUT

L3 4 μH
C3 1600 pF
C4 16 pF

L4 400 μH

0.05 μF

510Ω

360Ω

39Ω

+ EL2074C

- EL2074C

L5 4 μH
C5 1600 pF
C6 16 pF

L6 400 μH

0.05 μF

510Ω

360Ω

39Ω

L7 4 μH

0.05 μF

510Ω

300Ω

47Ω

Output to Spectrum Analyzer 50Ω

SW1

Low-Gain

High-Gain

C7 1600 pF
C8 16 pF

L8 400 μH

510Ω

300Ω

300Ω

±Vs ≥ ±5V to each amplifiers with separate 0.1 μF bypasses

Figure 3. Fundamental Reject Filters and Amplifiers
Fine Harmonic Distortion Measurements
in the Megahertz Range

Figure 4. Harmonic Select and Measure Section
A Simple Circuit Removes Sync
by Mike Wong

As the digital world encroaches into analog territory, signal conditioning circuits are required to prepare analog signals for digital processing. The standard composite video signal is an analog signal and generally AC coupled in video systems to prevent circulating DC currents. The following circuit demonstrates a method of conditioning a composite video signal for an analog to digital converter. The design example as depicted in Figure 1 consists of two main sections, a DC restore amplifier and a clamping amplifier. The DC restore amplifier clamps the back-porch of the video signal to a fixed reference and the clamping amplifier removes the sync portion of the video signal.

The video signal first goes into a sync separator, the EL4581C, and at the same time into a DC restore amplifier, the EL4089C. The EL4581C outputs a CMOS logic low signal into hold control input of the EL4089C during the back-porch section of the video signal. When the hold control input is low, the servo loop in the DC-restore amplifier forces its output to the reference level. A necessary offset voltage is placed across the sample and hold capacitor to create the proper input to output voltage shift. In the design example, C1, the AC coupling capacitor doubles as a sample and hold capacitor. Photo 1 shows the analog video input and the sync separator back-porch output waveforms. The back-porch output is used as the control signal for the sample and hold clamp signal. The combination of the EL4581C and EL4089C clamps the back-porch of the video signal to the ground level. Note that the sync tip of the video signal remains untouched.

All CMOS ADCs have a parasitic latch-up problem when subjected to negative input voltage levels. Since sync tip contains no useful video information and it is a negative going pulse, we can chop it off. The EL2157C stage limits the negative excursion to the ground level. The input and output range of the EL2157C is 0V to 3.5V. Its fast 7 ns of negative over-drive recovery makes it ideal for clamping applications. Photo 2 shows the incoming video signal whose back-porch is clamped to the ground level and the amplifier output signal with negative going portion of the sync tip chopped off.
A Simple Circuit Removes Sync

Figure 1. DC-Restore Sync Remover

Photo 1. DC Restore

Photo 2. "Sync-Less" Video Signal
Simple CMOS Driver Circuits Generate Bipolar Outputs

by Mike Wong

There are many applications such as IGBT, CCD, and transducer drivers where high peak current and bipolar output voltage swings are often required. This applications brief discusses two implementations of generating bipolar output using the EL7182 and EL7501 CMOS drivers.

Figure 1 shows the traditional scheme. The EL7182 is powered with a +5V and -7V supplies. The input comparator threshold is referenced to the ground pin which is connected to the negative supply so proper input voltage level shifting is necessary to operate the input comparator. The Zener diode in series from the TTL output to the input of the EL7182 provides the voltage level shift. Figure 2 depicts the inputs and the output waveforms. When TTL input is 0V, the voltage at the EL7182 input is shifted to -7V. When TTL input is 3V, the voltage at the EL7182 input is shifted to -4V which is 3V above the -7V on the ground pin. However, this implementation has a couple of drawbacks, in addition to the extra components required for input level shifting, the series Zener diode and resistor can also load down the TTL signal. When TTL input signal is high, bias current must flow across the Zener diode through the resistor to ground. This pulls the EL7182 input pin high with reference to the -7V supply.

Figure 2 uses the EL7501 to escape the input loading problem. The inputs of the EL7501 are differential where a 1V differential voltage across its input pins guarantees the output voltage to switch state. The input can be modeled as a series 180 kΩ resistor tied to a DC voltage 1V below the VDD supply. The series 50 kΩ resistor puts a 1.1 voltage at pin 4, as a result, when the TTL input at pin 1 is switching between 0V to 3V, the current comparator internal to the EL7501 senses current changes through the input resistors and changes the state of its output FETs. The ground and input pins are isolated and their breakdown voltage is over 100V. There are a couple of drawbacks with this circuit solution, 1) the maximum frequency is limited to 2.5 MHz, 2) input to output delay is higher than the EL7182. Figure 4 shows the input and output waveforms.
Simple CMOS Driver Circuits Generate Bipolar Outputs

Figure 3

Figure 4
Designing a High Efficiency DC-DC Converter with the EL75XX
by Mike Wong

Preface
Since the beginning of the digital revolution, the speed of a microprocessor has been governed by Moore's law postulated in 1968 by Intel's co-founder Gorden Moore. Moore suggested that the speed of a microprocessor would double in every 18 months. However, the principle of conservation of energy, more scientific in nature, will eventually dominate and limit the rate at which the speed of a microprocessor is increasing. The equation $P = CV^2F$, a derivative of the principle of conservation of energy, dictates that the power dissipated in a device is linearly proportional to its clock frequency and distributed capacitance. Microprocessor manufacturers have made great advances in reducing the amount of power dissipation in the device. The popular Pentium microprocessor, for example, employs a combination of heat-sink/fan to extract heat from the package. To further combat the power dissipation problem, a new generation of low voltage CMOS fabrication processes have been developed. The low voltage processes have a smaller transistor geometry that results in lower parasitic capacitance, reducing $C$ in the above equation. Smaller transistor size also allows for a increase in the number of transistors in a given die area, and as a result, the lifetime of Moore's law is extended. However, technical problems are being passed onto the shoulders of power supply designers. Lower microprocessor supply voltages and higher supply currents mean that the linear DC-DC regulator is no longer a viable solution. Power supply designers are forced into using switching regulator techniques. Lower output voltage, higher output current, and smaller output voltage ripple requirements have greatly increased the difficulty of the power supply design. To further burden the problem, power saving "stop-clock" modes have demanded faster and more stable transient response from the DC-DC converter.

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Introduction

The purpose of this Application Note is to demonstrate the operation of the EL7560 in an 12.4A output current mode DC-DC converter module for powering Intel's latest microprocessor, the Pentium-Pro. The EL7560 is the world's simplest, most integrated, and most cost effective switcher. It incorporates the PWM functions, current sense resistor, high current synchronous FETs, precision DAC for output voltage programming, and over-voltage and over current protection features. In addition, the advanced control loop design controls the load regulation of the DC-DC converter to meet the Pentium-Pro DC-DC converter output load transient specification with low cost and readily available Aluminum Electrolytic capacitors.

Lower output current versions of the device are also available. The EL7560 requires an external reference. This gives the application more flexibility and accuracy. A precision ±½% reference is incorporated in the EL7561 to reduce component count. The EL7556 is the 6A output current version. The power supply design considerations presented in this Application Note are applicable to all devices in the EL75XX family.

In the component selection sections, all calculations are based on the worst case specification limits in the Intel P6 DC-DC Converter Design Specifications.

EL7560 Theory of Operations

The EL7560 is a current mode switcher which means that the power switch duty cycle is determined by comparing the output inductor current and the error amplifier output voltage. Current mode control offers a number of advantages over the traditional voltage mode control. First, because the inductor current ramp is proportional to the input voltage level the converter can respond quickly to line variations. Second, it greatly simplifies the over-all loop design. The pole introduced by the output inductor is taken out of the loop and replaced by a high output impedance current source which is regulated by an inner current control loop. Lastly, it allows automatic pulse by pulse current limiting which protects the power switches when the output is overloaded or shorted.

The negative input of the error amplifier is brought out to sense the output voltage. The output of the error amplifier is compared with the current ramp from the current sense amplifier. (The current ramp is modified by slope compensation circuitry in order to prevent noise and oscillation problems.) The output of the comparator then resets a flip-flop which terminates the "on" time of an internal power NMOS FET. The error amplifier reference voltage is programmed by a 4-bit DAC with 100 mV resolution.

The EL7560 also includes a number of housekeeping functions. In the case of overheating, the power switches can be shut off by properly configuring Obar, pin 13/OT. When the output voltage is within regulation, the power good signal pin will go high. The device can be disabled by pulling output enable (pin 14) low, putting the device in a lower power state. During start-up, the switching duty cycle is limited by the internal soft-start circuit to generate a smooth power converter output response.

The oscillator frequency can be easily set by an external capacitor. The oscillator is designed to operate up to 1 MHz switching frequency. External adjustable slope compensation is provided to obtain the best system performance.
Figure 1. EL7560 Functional Block Diagram
### Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, C⁻</td>
<td>Negative terminal for the charge pump bootstrap capacitor. This pin oscillates from V_DD to V_SS at one half the clock frequency.</td>
</tr>
<tr>
<td>2, C⁺</td>
<td>Positive input for the charge pump bootstrap capacitor. This pin oscillates from V_DD to twice V_DD at one half the clock frequency.</td>
</tr>
<tr>
<td>3, C₂V</td>
<td>Voltage doubler input. A 100Ω resistor is used to limit current into this pin. A 1 μF capacitor is also needed to sustain the voltage doubler output. The 1 μF capacitor should be returned to the power ground node. The voltage on this pin will be 8V–10V depending on the load.</td>
</tr>
<tr>
<td>4, V_SS</td>
<td>This pin is the ground input for the control circuitry. It must be separated from the high current power ground. This pin should be connected directly to the ground point of the output capacitors.</td>
</tr>
<tr>
<td>5, V_HI</td>
<td>This pin is the positive supply for the high side driver. It is bootstrapped from the LX pin with a 0.1 μF capacitor.</td>
</tr>
<tr>
<td>6, 7, 8, 9, and 10, LX</td>
<td>This is the halfway point between the two large internal FETs. It drives the inductor of the buck regulator circuit. High switching current is seen at this pin.</td>
</tr>
<tr>
<td>11, TEST</td>
<td>This pin is used to test the internal power FETs during the final test at the factory. It must be connected to any convenient ground in the application.</td>
</tr>
<tr>
<td>12, PWRGD</td>
<td>This pin outputs a high signal (Logical &quot;1&quot;) to signify power good when the FB pin is within 7% of its programmed value.</td>
</tr>
<tr>
<td>13, OTbar</td>
<td>This pin pulls low (Logic &quot;0&quot;) when the die temperature exceeds 135°C. It is normally a high impedance output. It has 15°C of hysteresis. To turn off the FETs in the event of an over-temperature condition, simply connect this pin to the OUTEN pin and a 10 kΩ resistor to V_DD.</td>
</tr>
<tr>
<td>14, OUTEN</td>
<td>A high input signal applied to this pin enables the switching regulator. The reference, oscillator, and voltage doubler operate whenever the power supply is above its UVLO threshold regardless of the state of this pin.</td>
</tr>
<tr>
<td>15, 16, 17, and 18 V_ID3, 2, 1, and 0</td>
<td>These are the DAC input pins used to program the output voltage.</td>
</tr>
<tr>
<td>19, 20, and 22, V_SSP</td>
<td>These pins are the ground returns to the buck regulator. They are internally connected to the source of the low side synchronous NMOS FET.</td>
</tr>
<tr>
<td>21 and 23, V_IN</td>
<td>These pins are the positive power supply input to the buck regulator. They are internally connected to the drain of the high side synchronous NMOS FET.</td>
</tr>
<tr>
<td>24, V_DD</td>
<td>This pin supplies power to the internal control circuitry. It typically draws 30 mA when operating.</td>
</tr>
<tr>
<td>25, COSC</td>
<td>A capacitor connected from this pin to ground sets the frequency of the PWM oscillator. The oscillator frequency is approximately ( F_{OSC} = 0.001/C_{OSC} ). The maximum duty cycle is fixed at 96%.</td>
</tr>
<tr>
<td>26, CSLOPE</td>
<td>A capacitor connected from this pin to ground sets the amount of slope compensation. A 30 μA current flows out of this pin. The voltage at this pin is reset to the reference voltage whenever the high side NMOS FET is off.</td>
</tr>
<tr>
<td>27, C_REF</td>
<td>This is the external reference input pin. A minimum of 1.0 μF to ground is recommended.</td>
</tr>
<tr>
<td>28, FB</td>
<td>This is the voltage feedback input pin for the buck regulator. It is internally connected to a resistor divider.</td>
</tr>
</tbody>
</table>
Figure 2. P6 DC-DC Converter Circuit
Basic Buck Regulator Topology

Figure 3 shows the basic buck regulator topology. When Q1 turns on, the voltage across L1 is \( V_{IN} - V_{OUT} \) and current flows from \( V_{IN} \) to \( V_{OUT} \). When Q1 turns off, the inductor current continues to flow, and as a result the cathode of D1 gets pulled below ground by the back EMF of the output inductor, L1, and starts to conduct. The voltage across L1 is \(-V_{OUT}\) and output current flows through D1 and L1 to \( V_{OUT} \). Under steady-state conditions, the voltage across L1 must average to zero. If \( T_1 \) is the time Q1 is closed, and \( T_2 \) is the time Q1 is open, then the relationship between \( V_{IN} \) and \( V_{OUT} \) is:

\[
(V_{IN}-V_{OUT})T_1 - (0 - V_{OUT})T_2 = 0
\]

Equation (1) can be simplified to

\[
V_{OUT} = V_{IN} \cdot D
\]

Where D is the duty cycle, \( D = T_1/(T_1 + T_2) \).

Equation (2) tells us a great deal about switching mode converters. First, it suggests that the output voltage is solely a function of \( V_{IN} \) and the duty cycle of the switch. Secondly, it is not a function of the output inductor, capacitor or switching frequency. Lastly, it is not a function of the magnitude of the output load current.

Continuous Mode Operation

The preceding discussion describes the situation where the inductor current never reaches zero. This form of operation is called "continuous" mode. Figure 5 depicts Q1 and Q2 gate drive waveforms, Q1 drain and Q2 source current waveforms, and the output inductor currents.

During \( T_1 \), Q1 is turned "on" and Q2 is turned "off", inductor current \( I_{L1} \) and \( I_{SOURCE1} \) increase from the initial value which is not zero. The slope of the current ramp is dictated by

\[
\frac{\Delta I_D (Q1)}{\Delta T} = \frac{V_{IN} - V_{OUT}}{L_1}
\]

In this cycle, energy is stored in the inductor for use during the off cycle and current flows from input to the output.

During \( T_2 \), Q1 is turned "off" and Q2 is turned "on", inductor current \( I_{L1} \) continues to flow to the output via Q2. Inductor current declines to the initial value and gives up energy to the output.
Discontinuous Mode Operation

Normally, a converter designed for the continuous mode operation stays in continuous current mode under all load conditions. However, the converter can go into discontinuous current mode momentarily when the output load is changed from its maximum to minimum level. The mode of operation where the inductor current falls to zero is called discontinuous operation. The waveforms in Figure 6 are synchronized gate drive waveforms, power FET source current and output inductor current waveforms. During T1, Q1 turns "on" and Q2 turns "off", the inductor current starts from zero and rises to the peak value Ip. Energy, $P = LI^2/2$, is stored in the inductor. During T2, Q1 turns "off" and Q2 turns "on", inductor voltage reverses and its stored energy is delivered to the output. The inductor current decreases linearly to zero. When the inductor current reaches zero, Q2 must turn "off" to prevent inductor current flow from the storage capacitor to ground. Thus, during T3, both Q1 and Q2 are turned "off".
Current Mode Control
The advantages of current mode control were discussed in an earlier section. It basic block diagram is shown in Figure 7. The duty cycles of the power FETs are generated by comparing the error amplifier output voltage with a sawtooth ramp. This sawtooth ramp is provided directly from the power switching circuit inductor current waveform through a current sense resistor, RSENSE. The fact that the slope of the current ramp is a function of VIN, VOUT, and the output choke inductance, VIN - VOUT = L ΔI/ΔT, suggests an inherent voltage feed forward characteristic with instantaneous open loop response to any input voltage changes. The output inductor pole is included in the current loop, and as a result, it is eliminated from the outside voltage loop. This reduces the output filter from a two pole network to a simple single pole. The outer loop is a voltage loop where the output voltage, VOUT, is compared with a reference voltage, VREF, and produces an error voltage output for the PWM comparator. An interesting aspect of the current mode control scheme is that the error amplifier output voltage programs the inductor current which causes the output voltage to rise or fall and the error amplifier output voltage is derived from comparing VOUT with VREF. The result is that the PWM duty cycle maintains the inductor current such that VOUT is equal to VREF.

Slope Compensation
While current mode control has a number of desirable characteristics, it also carries a flaw which, if not treated properly, can cause severe output oscillation. As described in the previous sections, current mode control regulates the peak inductor current via the inner current loop. However, in a buck converter, the output current is the average inductor current. Figure 8 graphically represents the output inductor current using two different input voltages. When in regulation, the error amplifier output voltage, VE, should not change. A constant VE (VE sets the peak output inductor current level) implies that the average output current for the higher input voltage level (duty cycle = D1) is slightly higher than the output current associated with the lower
input voltage (duty cycle = D2). This will result in a higher output voltage which the voltage loop will correct by changing \( V_E \), which in turn will result in a different duty cycle, which results in different average current levels. This effect has been dubbed sub-harmonic oscillation and can be evidenced by output voltage oscillation at one half the switching frequency.

One method of maintaining constant output current is to add a voltage ramp on the current sense output as depicted in Figure 9. This has the effect of lowering the error amplifier voltage as a function of \( T_{ON} \).

Slope compensation also improves noise immunity. Figure 10 demonstrates how a small perturbation in the inductor current can result in an unstable condition. For a duty cycle less than 50%, the perturbation is suppressed quickly each cycle (\( dI'1 \approx dI1 \)). For greater than 50% duty cycle, a small perturbation is amplified (\( dI'2 \gg dI2 \)) each cycle and causes an unstable condition.

Figure 11 shows the inductor current perturbation problem being corrected with slope compensation. With slope compensation, inductor current perturbation is attenuated each cycle at all times even when the duty cycle is greater than 50%.

In the EL7560, a slope compensation ramp is created with a 30 \( \mu \)A current source charging an external capacitor, \( C_{SLOPE} \). The voltage on \( C_{SLOPE} \) is reset to the reference voltage whenever the internal high side NMOS FET is off.
Note 1: Figure 12 shows the experimental test results of the effects of the amount of slope compensation on the output voltage accuracy, output load regulation, and line regulation. The fact that slope compensation limits the duty cycle becomes apparent in Figure 12a. A $C_{\text{slope}}$ is decreased, the slope of the current ramp increases as a result the duty cycle is decreased and thus the decrease in output voltage.
PWM Comparator

In the heart of the EL7560 PWM section is a direct summing comparator. The regulator output is first compared with a reference (DEC output) voltage. The resultant error voltage is then compared with current sense signal and slope compensation ramp. PWM duty cycle is then adjusted according to the summing comparator output. The direct-summing scheme enables cycle by cycle control of the output voltage. This scheme also eliminates the traditional feedback compensation integrator. The dominant pole is set by the output capacitor and the equivalent output resistive loading.

Output Inductor, L1

The output inductor serves two purposes, it stores energy and filters output ripple current. Trade-offs often have to be made between the physical size of the inductor and the maximum energy storage. The primary criterion for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode operation under all line and load conditions. To maintain the conditions of continuous mode operation under the minimum load and maximum line condition (duty cycle is at its minimum) at 500 KHz switching frequency, the minimum inductance can be calculated with the following equation:

\[ V = L \cdot \frac{\Delta I}{\Delta T} \]

where

- \( V \) is the voltage across the inductor,
- \( V = 5.25 - 3.07 = 2.13 \text{V} \) (The Worst case P6 DC-DC converter specifications are used in all calculations.)
- \( L \) is the inductance required to maintain continuous mode operation
- \( \Delta I \) is the peak ripple current,
- \( \Delta I = 2 \cdot I_{\text{OUT(min)}} = 0.6 \text{A} \)
- \( \Delta T \) is the duration at which the current is ramping up in the inductor, or the "on" time of the PWM,
- \( \Delta T = (3.07/5.25)/500 \text{ KHz} = 1.17e-6 \)

\[ L = V \cdot \frac{\Delta T}{\Delta I} = 2.13 \cdot 1.17e-6 / 0.6 = 4.15 \mu \text{H} \]

One inductor which meets this criterion is the Pulse Engineering PE-53681. Its inductance is 4.2 \( \mu \text{H} \) at minimum output current. The saturation effect of the magnetic core causes the inductance to decrease. At the maximum output current of 11.4A, the inductance of the PE-53681 decreases to 2.5 \( \mu \text{H} \). As a result the ripple current will increase at high output current,

\[ \Delta I = V \cdot \frac{\Delta T}{L} = 2.13 \cdot 1.17e-6 / 2.5e-6 = 1 \text{A} \]

When selecting the output filter capacitor, the worst case 1A ripple current must be used when calculating the output ripple voltage.

There are two important criteria in selecting an output inductor:
1. The minimum inductance at zero DC current must be greater than the inductance required to maintain continuous mode operation.
2. The core size and wire gauge must be sufficient to handle the maximum output DC current.

Output Capacitor, C10

The output capacitor filters the output inductor ripple current; thus, it must be low ESR type electrolytic capacitor. One must carefully decide between cost, size, and quality (ESR) of different types of capacitors. Names of capacitor manufacturers are listed at the end of this Application Note. The calculations shown below are done with the low cost United Chemi-Con LXF series Aluminum Electrolytic capacitors. The module layout available in the appendices of this document can accommodate both the high quality OS-Con capacitors or the inexpensive United Chem-Con capacitors.

As stated previously, the output capacitors must be low ESR type for two reasons: 1) to ensure lower ripple voltage 2) to meet the load transient specifications.
1. The Intel P6 DC-DC converter specification calls out for a maximum of ±1% output voltage ripple. For a 3V output that corresponds to 60 mV peak to peak. The previous inductor calculation section shows the ripple current to be 1A at the maximum load, thus, the maximum ESR allowed is 60 mΩ. For this example we have chosen 6 pieces of 680 μF United Chemi-Con series LXF aluminum electrolytic capacitors (part # LXF16VB681M10X12FT). The total capacitance is 4 mF and their combined ESR is 10.33 mΩ. The resultant peak to peak ripple voltage under full load condition is 10.33 mV.

2. When the output is stepped from minimum to the maximum level, the full output current load step will initially be supplied from the output capacitor Co (IC), as shown below.

\[
\Delta V_{OUT} = ESR \cdot I_{TRANSIENT} + ESL \frac{\Delta I}{\Delta T} \quad (4)
\]

Cylindrical aluminum electrolytic capacitor typically has 5 nH of ESL. The combined effective series inductance is 5/6 nH. The change in output voltage due to ESR and ESL during the initial output current transient is

\[
\Delta V_{OUT} = 10.33 \text{ mΩ} \cdot (12.4 - 0.3) + \frac{5}{6} \text{ nH} \cdot \frac{30 \text{ A} / \mu s}{153 \text{ mV}} = 153 \text{ mV}
\]

Immediately after load transient, Co will continue to supply current to the output load until the inductor current ramps to the maximum 12.4A output current level. The internal FET will be switching at 96% duty cycle until the output voltage gets back to within regulation. The amount of time for the inductor to ramp up to 12.4A is,

\[
\Delta T = \frac{L \cdot \Delta I}{V_{IN} - V_{OUT}} = \frac{2.5 \mu H \cdot 12.1A}{2.1} = 14.4 \mu s
\]

Taking the 96% duty cycle into account:

\[
\Delta T = 14.4 \mu s / 0.96 = 15 \mu s
\]

In 15 μs the output voltage drops to:

\[
dV = \left[ \frac{1}{C_o} \int_0^{15 \mu s} (12.4A - 0.3A - \frac{dI}{dt}) dt \right] + (12.4A - 0.3A) \cdot ESR
\]

\[
\frac{dI}{dt} = \frac{(V_{IN} - V_{OUT})}{L} = \frac{(5 - 2.9)}{2.5 \mu H} = 0.84 \text{ A} / \mu s
\]

Plugging in the numbers to equation (4) yields:

\[
dV = 146.7 \text{ mV}
\]

The output drop caused by the output capacitor discharging is less than voltage drop due to ESR and ESL of the output capacitor.

![Figure 13. Output Current Path during Transient](image-url)

![Figure 14. Output Voltage Variation with Traditional Control Scheme](image-url)
The total $\Delta V_{\text{OUT}}$ transient allowed by the Intel spec is $\pm 5\%$. If we subtract 1% for the tolerance of the EL7560 reference we end up with only 4% of the 2.9V which is 116 mV which is less than the 153 mV that we calculated. However, the unique loop compensation of the EL7560 degrades the load regulation by $\pm 2\%$ so that at maximum load the output voltage is 2% lower than nominal and at minimum load the output voltage is 2% higher than nominal. The result is 58 mV of additional output voltage head room to move around during load transient.

The timing diagrams in Figure 14 show how the output voltage changes in a converter with the traditional control scheme. The converter output current, waveform 14a, is changed from the nominal level (5A) to the minimum (0.3A) then to the maximum (12.4A) then back to 0.3A again.

Figure 14b depicts the output voltage response for a control IC with infinite open loop gain and the error amplifier reference voltage is exactly at 3.00V. The infinite open loop gain gives us the perfect load regulation, i.e., the output voltage always settles to 3.00V under all conditions. $dV = 153$ mV is a result of ESR and ESL of the output capacitor. Equation (4) is the equation and derivation.

Figure (14c) and (14d) show output transient effects with $\pm 1\%$ tolerance on the error amplifier, 153 mV of voltage change at the output gets out of the $\pm 5\%$ output voltage limit called out in the Intel P6 DC-DC converter design specification.

The EL7560 utilizes a unique error amplifier compensation technique to control the load regulation. The Intel spec allows a 4% total output change with loading. The load regulation is set such that at minimum output load (0.3A) the output voltage is 2% higher than nominal (5A) and at maximum load (12.4A) the output voltage is 2% lower. The result is an additional 2% (60 mV) of head room for transient load response. Figure 15 shows the transient response waveforms.
In summary, if the load regulation is properly controlled, i.e., at minimum load the output voltage is 2% (60 mV) higher than nominal load (5A) and at maximum load the output voltage is 2% (60 mV) lower than nominal load, we can fit the output transient response curves within Intel's ±5% window under any conditions.

**Input Filter/Input Current Transient Analysis**

A 1 μH inductor in series with the input capacitor is required to meet the Intel "Load Transient Effects" specification which states that, "During this step response (the output load is switching from 0.3A to 12.4A) the input current di/dt shall not exceed 0.1A/μs." The input filter inductor is absolutely necessary in the standard buck topology. The simulation results of input transient current during output load changes are shown in Figure 16. As the input inductance increases, the slope of the input transient current decreases.

In the Elantec module reference design, a custom inductor is used. The core of the inductor is Micrometals T30-26 and the wire gauge is AWG #20 with 7 turns. The inductance value is 1.6 μH. For users who want to use an off the shelf inductor we suggest the Pulse engineering PE53188. Its inductance spec is 2.2 μH at 6.4A.

Figure 16 shows the simulated input current response for various combinations of the input inductor and capacitor. The simulation result shows that a 1.5 μH inductor and a 2 mF capacitor combination suffice to meet the Intel input transient specification.

**Over-Voltage Protection**

The over-voltage condition is defined by Intel as the situation when the output voltage goes 10% higher than the programmed level. Upon detection of an over-voltage fault, the internal high side FET is turned off. A clamping diode D4 from the LX pin back to the input is recommended to keep the LX pin a diode voltage drop above the input. The switcher recovers automatically when the over-voltage fault is removed.

**Over-Current Protection**

The EL7560 has a built-in over-current protection feature. When an over-current fault occurs, the high side FET automatically turns off. The switcher recovers automatically when the over-current fault is removed.

**Efficiency Calculations**

Most of the power dissipated in the EL7560 is due to the "on" resistance of the power FETs. Each power FET exhibits a typical 30 mΩ "on" resistance; therefore, the power loss is $P = I^2 R = 12.4 \times 12.4 \times 0.030 = 4.61W$ (at rated maximum load).

Efficiency curves of the typical VRM demo module is depicted in Figure 17. The curves show low efficiency at both ends of the output loading. At the low output current end, switching losses of the switcher is high relative to the output power. At the high output current end, the on-resistance of the power mosfet dominates.

![Figure 16. Input Filter Transient Response](image1)

![Figure 17. VRM Efficiency](image2)
Heat Sinking Requirements
For reliability reasons, the Intel spec requires that the junction temperature of the EL7560 be kept below 115°C with the ambient temperature at 50°C and 100 LFM air flow. The minimum θJA required is:

$$\theta_{JA} = (115 - 50) / 4.61W = 14.1°C/W$$

The θJA for the 28-pin PSOP2 without a heat sink is 52°C/W, and the θJC is 5°C/W. The θJC of the device combined with the thermal resistance of the heat sink must be less than 17°C/W. Thermal analysis has been done with Wakefield 8052-60 mounted on top of the package with Ablebond 84-1 LMIT epoxy adhesive which has 0.2°C/W thermal resistance. With a board size of 1.5" x 3" and an air flow of 100LFM, measurements made by Elantec yield a θJX is 12.9°C/W.

Board Layout Considerations
Grounding Issues

Figure 18 is the simplified circuit of the power system.

When the high side FET is turned on, Figure 19 shows current flow directly from the AC/DC power supply and the input capacitor through the high side FETs to the load. The ground return current splits into two directions: 1) from the load directly to the AC/DC power supply 2) from the load into the DC-DC module and to the ground of the input capacitor.

When the low side FET is turned on, most of the output load current flows through the low side FET. Current from the AC/DC power supply continues to flow into the input capacitor, whose magnitude (around 8A at maximum output load) is the same as the ground return current from the load. The 12.4A of output current is a combination of current from the input capacitor and the ground input of the DC-DC module.
Figure 18. A Simplified Power System Block Diagram

Figure 19. Current Flow Path when High Side Switch is ON

Figure 20. Current Flow Path when Low Side Switch is ON
Figure 21 summarizes the magnitudes and directions of currents at various nodes in the DC to DC converter under the maximum output loading condition. The DC-DC module input and output current, and AC/DC power supply ground return current, and load return current are constant under steady state conditions.

The current path in the above figures show that the power ground pin, VSSP, VIN, and LX pins, which are switching at 500 KHz, are thus extremely noisy. They should be isolated from the logic control and reference of the PWM controller. The ground pin of the output capacitor, C10, is the quietest point in the converter. We recommended splitting the signal ground and power ground at the ground pin of the output capacitor.

The VSS pin and ground connection for C4, C7 and C8 should all be connected to the signal ground.

A 12.4A DC-DC converter reference layout is included in the appendices section of this application note. Proper grounding and layout techniques discussed above are demonstrated in this design.

Charge Pump Design
The EL7560 has an internal voltage doubler and a bootstrap charge pump to generate the high voltage required to switch on the internal high side N-channel FETs. C5, the 1 μF capacitor from pin 1 to 2, is the voltage doubler pump capacitor. It charges C11 through D2. A ceramic capacitor is adequate for C5. D1 and C6 are the bootstrap diode and capacitor. When the low side FET is turned on, capacitor C6 is charged to 10V, when the high side FET switch on the VHI pin is bootstrapped to 15V. Capacitor C11 holds the voltage doubler output voltage and the resistor R1 limits the current into the low side FET drivers inside the chip. A 1N914 type diode suffices for both D1 and D2. The most critical specification for selecting this diode is its reverse breakdown voltage which should be greater than 15V. In addition, a low forward voltage drop is desired to generate a higher voltage level for the high side drive. If a 12V supply is available, then the charge pump diode and voltage doubler capacitor can be eliminated. Figure 22 shows the circuit implementation.

![Figure 21](image1)

![Figure 22](image2)
Remote Sense
Although it is not specified in Intel P6 DC-DC converter design guide, remote sensing is often desired in many applications. In the case of a 200 MHz P6 microprocessor, the supply current can reach over 12.4A. A 10 mΩ of trace resistance results in a 124 mV of voltage drop from the converter output to the microprocessor supply pin. A simple method of implementing remote sensing is depicted in Figure 23.

![Figure 23.](image)

The 1 kΩ resistor is connected directly to the converter output and the 10Ω remote sense resistor should be tied directly to the load or the microprocessor supply input pin.

Bill of Materials

<table>
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<tr>
<th>Component</th>
<th>Quantity</th>
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</thead>
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</tr>
<tr>
<td>680 μF</td>
<td></td>
</tr>
<tr>
<td>C9, United Chemi-Con, LXF16VB681M10X20LL,</td>
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<tr>
<td>Heat Sink—Wakefield Engineering, 8052-60</td>
<td>1 pc</td>
</tr>
</tbody>
</table>

Appendices

Package outline
Core and Inductor Manufacturers
Magnetic Cores
Micromets
1190 N. Hawk Circle
Anaheim, CA 92807
Phone 800-365-5977

Inductors
Pulse Engineering
P.O. Box 12235
San Diego, CA 92112
Phone 619-672-8100

Inductors
Pan Technology Ltd.
Unit 11, 6/F Proficient Industrial Center (Block A)
6 Wang Kwun Road
Kowloon Bay, Hong Kong
Phone 852-2758-5759
Fax 852-2758-5761

Capacitor Manufacturers
Aluminum Electrolytic Capacitors
United Chemi-Con
9801 West Higgins Road
Rosemont, IL 60018
Phone 708-696-2000

Solid Tantalum Chip Capacitors/OS-Con
Solid Aluminum Capacitors
Sprague
678 Main Street
Sanford, ME 04073
Phone 207-324-7223

Heat Sink Manufacturers
Heat Sink and Mounting Clip
Pan Technology Ltd.
Unit 11, 6/F Proficient Industrial Center (Block A)
6 Wang Kwun Road
Kowloon Bay, Hong Kong
Phone 852-2758-5759
Fax 852-2758-5761

Heat Sink
Wakefield Engineering
Introduction

Unity gain buffers have been available in integrated form since the introduction of the LH0002 by National Semiconductor several years ago. The "ideal" buffer would exhibit a gain identically equal to one, an input impedance of infinity, an output impedance of 0Ω, infinite bandwidth and zero phase shift, infinite slew rate, large but limited to a safe level output current, and an output offset voltage and input bias current of zero. These devices are usually implemented with fairly simple circuit topologies which makes them very cost effective in applications requiring large output currents, isolation from reactive loads, input to output isolation, and in some instances thermal isolation in circuits requiring precision gain and offset. The buffers simplicity imply obvious applications in a circuit. After all, what could go wrong with a unity gain buffer? This note is intended to discuss this very subject.

Circuit Topologies

When you get down to it, there are only two types of circuits: open and closed loop. The latter are specially designed operational amplifiers optimized for operation at unity gain which typically exhibit less bandwidth, more phase shift, and usually more expensive than the open loop variety. On the other hand, they exhibit better offset voltage and gain linearity. The former is essentially a glorified compound emitter follower offering cost, increased bandwidth, and in general poorer DC characteristics.

Open Loop Buffers

Shown in Figure 1 is the classic "0002" topology. It is comprised of compound emitter followers Q1 and Q3 which provide current gain for positive going signals and their mirror image of Q2 and Q4 for negative signals. Bias is set up with current sources I1 and I2. In some realizations of the circuit, I1 and I2 are replaced by resistors. If we assume for simplicity that I1 = I2, inspection of the circuit reveals that the Vbe's of Q1 and Q2 are impressed across the base emitter junctions of Q3 and Q4; hence, the emitter currents of Q3 and Q4 are almost equal to I1 or I2 (ignoring the effects of R1 and R2). In real circuits, R1 and R2 are used to prevent thermal runaway of the output stage. Since Q3 and Q4 will sink or source many milliamps, their Vbe's will decrease as they heat up, but the "bias" voltage across them, Vbe(Q1) + Vbe(Q2) remains substantially the same, there is a real possibility of reaching a thermal runaway point. R1 and R2 provide "positive" feedback to the output transistors increasing their effective Vbe as the output current increases.

One of the nice things about the 0002 topology is that it exhibits very low crossover distortion (typically under 0.1% with an output power of 0.5W @ 10 MHz). As the output current in Q3 increases, its Vbe increases while Q4's emitter current and Vbe decrease while the bias of Vbe(Q1) + Vbe(Q2) remains essentially constant. Q4's emitter current never quite goes to zero thus minimizing crossover distortion.

The output current will limit or the output voltage will "clip" when all the current provided by I1 (or I2) is demanded as base current to Q3 (or Q4) which obviously occurs when: I1 = IOUT/β or when I1 saturates. The output offset voltage is simply the difference between VbeQ1 and VbeQ3 or VbeQ2 and VbeQ4 whichever is lower. To the first order then:

\[ V_{OS} = V_{beQ1} - V_{beQ3} \text{ or } V_{beQ2} - V_{beQ4} \]  
\[ I_{bias} = I_1 (\beta_1 - \beta_2) / (\beta_1 \beta_2) \]  
\[ A_V \approx R_L / (R_L + R_{OUT}) \]  
\[ R_{OUT} \approx [R_1 + r_e Q4 + R_s / (\beta 4 \beta 1)] / 2 \]  
\[ R_{IN} \approx (\beta_1 \beta_2) R_L \]  
\[ I_{SUPPLY} \approx 3 I_1 \]
Myth Number 1: Input Impedance

Earlier we said that one of the attributes of an ideal buffer was infinite input impedance. Illustrated in Figure 2 is a plot of the input impedance of the EL2002, 180 MHz Unity Gain Buffer. Clearly, at low frequencies, the input impedance is above 1 MΩ; however, as the frequency increases the β decreases and the input impedance drops accordingly per equation (5). In fact there is a doublet in the vicinity of 50 MHz where the input capacitance of the EL2002 and the source resistance create the additional pole. This behaviour is typical of all 0002 type buffers and whereas it is not fatal, the user should be aware of the issue.

Myth Number 2: Output Impedance

The ideal buffer should exhibit zero output impedance. Illustrated in Figure 3 is the DC output impedance of the EL2002 as a function of output current. As the load current increases, $R_{OUT}$ asymptotically approaches the value of $R_1$ or $R_2$ (depending on which half of the circuit is working). In other words, the $r_e$ term approaches zero as the emitter current increases per equation (4) above. Furthermore, Figure 4 illustrates the small signal output impedance of the EL2002 as a function of frequency. In this instance any impedances which exist at the base of Q3 (or Q4) is divided by the product of $β1*β4$, but as the frequency goes up, the $β$ goes down, and the $R_{OUT}$ increases. The dip in the output impedance above 100 MHz is due to capacitance of the package and on the die.

The foregoing discussion would have consequences in applications where the buffer was used “open loop” for example as a video distribution amplifier. Since $R_{OUT}$ is both a function of output current and frequency, the gain of the circuit would vary destroying the backmatch to the coax cable thereby creating distortion.

Booby Trap Number 1: Closed Loop Operation Oscillation

Clearly, a straight forward way of avoiding the problem in the previous section is to put the buffer in a loop with an op amp or CFA as illustrated in Figure 5. Indeed, this is a classical application for a buffer when the op amp does not have enough output current to drive the desired load. What could go wrong? In some instances, depending on the bandwidth and phase margin of the amplifier and the phase shift through the buffer, the composite loop can and will oscillate. For example, the phase shift of the EL2002 is illustrated in Figure 6. At about 100 MHz, it exhibits a phase lag of about 70°. When placed in a loop with an EL2044 which exhibits a nominal 60 MHz bandwidth with 45° phase margin and connected for unity gain, the circuit peaks 12 dB (or if you prefer oscillates) as shown in Figure 7. The caveat of this story is that one might expect 45° of phase lag at the $-3$ dB bandwidth of the buffer which in the case of the EL2002 is 180 MHz, but you would be wrong. Obviously, in the circuit of Figure 5, the phase margin of the EL2044 is eradicated by the phase shift of the buffer and the circuit oscillates. The moral of the story is to select an amplifier and buffer whose phase characteristics are compatible.

Another distinct possibility that can cause oscillation is the pole created by $R_3$ and the input capacitance to $A2$. $R_3$ isolates $C_{IN}$ from the output of the op amp, but if $R_3 * C_{IN}$ is in the same order of magnitude as the unity gain crossing frequency as the op amp, you get oscillation. In this case, get the value for $C_{IN}$ from the datasheet, and keep the value of $R_3$ as small as possible.

Finally, given that the buffers are no more than compound emitter followers, their ability to buffer reactive loads is no better (or worse) than a conventional op amp. See Elantec Application Notes Numbers 9 and 22 for details.
Booby Trap Number 2: Closed Loop Operation

Virtually all monolithic buffers offer some sort of short circuit protection. Although not shown explicitly in Figure 5, the typical scheme senses current in R1 and R2 and limits the base drive to Q3 and Q4. Yet in some applications in spite of the manufacturer's claims of being short circuit proof, the buffer dies in the circuit. In this instance, envision a 0Ω short from the output of A2 to ground. The loop goes open and the output of A1 saturates toward the positive or negative rail. Clearly, the bases of Q3 and Q4 are "clamped" by the short to one Vbe above (or below) ground. If the base emitter breakdown voltage of Q1 or Q2 is less than the saturation voltage of A1 less a Vbe, these transistors can and will avalanche leading to self destruction.

To preclude this possibility, Elantec places a chain of back-to-back diodes (usually about 4) from input to output. This clamps the input to 4 Vbe's several volts below the rated breakdown voltage of Q1 and Q2. The moral of this story is to check with the vendor on the details of the short circuit method.

Closed Loop Buffers

Most of the pitfalls of the preceding sections can be avoided by choosing a "closed loop" buffer. One of our favorites is the EL2099 whose primary mission was intended as a video distribution amplifier. Nevertheless, it is a 50 MHz Current Feedback Amplifier with output current capability of 800 mA. It has all of the virtues of Figure 5 with none of the booby traps.

Conclusion

Some of the basic issues in using unity gain buffers has been presented, and armed with these details the wary and informed circuit designer can make excellent use of buffers in real and demanding applications.

Figure 1. "0002" Topology
The Care, Feeding, and Application of Unity Gain Buffers

Figure 2. EL2002 Input Impedance

Figure 3. EL2002 DC Output Impedance

Figure 4. Output Impedance vs Frequency

Figure 5. Buffer in a Closed Loop with an Op Amp
Figure 6. Phase Shift vs Frequency for Various Capacitive Loads

Figure 7. 2044 in Loop with 2002
Using Single-Supply High-Frequency Amplifiers
by Barry Harvey and Mike Wong

The trend toward lower power supply voltages has recently inspired the design of integrated single-supply high-frequency amplifiers. The greatest use of these circuits is in passing video signals, although there are many other applications. Unity-gain bandwidths of the new offerings are in the 90 MHz–160 MHz range.

The earliest single-supply IC amplifier is the LM324, developed circa 1974. This is a 1 MHz op-amp that set the definition of a single-supply circuit:

A single-supply device works with no minus supply; using 0V and typically +5V for minus and V+ supply voltages, respectively. Inputs will linearly comply with 0 (ground) to some voltage approaching V+. Outputs will provide from 0V or nearly so to a voltage approaching V+.

Figure 1 shows circuitry at the input of these amplifiers. The input PNP differential pair is followed by an NPN folded cascode that performs level-shifting. The cascode emitter resistors have typically only 200 mV across them, allowing the input PNP bases to comply with ground-level inputs, and even a bit below ground, without severe saturation. For positive swings, the current-source transistors and the VBE’s of the input transistors set the input positive headroom, between 1.1V and 1.7V. The DC input offset will not degrade until input swings are within millivolts of the headroom limits, but AC characteristics can vary hundreds of millivolts from the limits. Usually bandwidth is the non-constant parameter, but in some circuits transient responses are also distorted.

The maximum output swing below V+ usually is about the same as input headroom. A complication is that output stages in bipolar technology cannot inherently sink current all the way to ground, and minimum output low swing depends on the polarity and magnitude of load current. A grounded pull-down resistor is often used to help the output to drop all the way to ground. Figure 2A shows an NPN/PNP output stage. A load resistor keeps the output NPN properly biased all the way to ground, but the output PNP has turned off well above. Figure 2B shows an all-NPN output stage. This design cannot swing as close to ground as 2A with a pull-down resistor, but it can swing somewhat lower than 2A when sinking load current. The all-NPN circuit does exhibit generally greater distortions and load capacitance sensitivity than the NPN-PNP design.
Output linearities are generally quite good within the headroom range for DC signals, but high AC distortions occur when levels approach clipping. Figure 2 shows the differential gain and phase errors, that is, the constancy of small-signal gain and phase as DC level varies, for several commercial amplifiers. Amplifier A is an EL2044, a general-purpose video amplifier; B is an EL2210, a low-cost video amplifier; C is an EL2150, a 125 MHz true single-supply video amplifier; and amplifier D is another vendor's 90 MHz single-supply amplifier. In Figure 3, all amplifiers are wired for a gain of +1, the input is a 50 mVp-p 3.58 MHz AC signal with DC offset sweeps from 0V to 5V, the load is 500Ω to ground, and the supply voltage is +5V. Here is a summary of amplifier swings, with 0.4% or 0.4° gain and phase deviations from the center of the span:

Table 1. Amplifier Output Swings [V] for 0.4% or 0.4° Deviation from Curves in Figure 3

<table>
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<tr>
<th>Amplifier</th>
<th>Low Swing</th>
<th>High Swing</th>
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<th>Total Span</th>
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<td>A</td>
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<td>B</td>
<td>0.65</td>
<td>2.80</td>
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<tr>
<td>C</td>
<td>0.22</td>
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<tr>
<td>D</td>
<td>0.22</td>
<td>4.10</td>
<td>2.16</td>
<td>3.88</td>
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</table>

For small signals, differential gain is similar to linearity error or harmonic distortion, although the scale factor between them is not 1:1. Differential phase is a specification important to preserving color quality in NTSC video. Differential gain and phase errors of 0.5% and 0.5° are sufficient for consumer or overlay NTSC video; 0.1% and 0.1° or better is required for professional NTSC video; and 0.5% gain linearity is sufficient for high-quality component video signals.

Note that each amplifier has a unique set of swings and center of span. Note that the single-supply amplifiers simply cannot operate linearly all the way to ground. If the maximum linear spans are to be obtained, the input signal must be offset by the Span Center. If offset, all of these amplifiers can pass an NTSC video signal with low distortion, even the non-single-supply models.
Figure 4 shows the amplifiers wired for a gain of +2 and driving a 150Ω load to ground, as in driving a back-terminated 75Ω cable service. The input is a 50 mVp-p 3.58 MHz AC signal with DC offset sweeps from 0V to 2.5V. The amplifiers all have more distortion with the heavier load:

The amplifier A cannot linearly swing the 2V span of double-sized NTSC signal and is not applicable to this task. Amplifier B can be used if the input is offset such that the worst distortion occurs in the non-critical sync portion of the signal. Neither of the true single-supply amplifiers will have trouble with video signals, and the output can be allowed to go all the way to ground in the sync tip.

Table 2. Amplifier Output Swings [V] for 0.4% or 0.4° Deviation from Curves in Figure 4

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<tr>
<th>Amplifier</th>
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<th>Span Center</th>
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<tr>
<td>A</td>
<td>1.05</td>
<td>2.50</td>
<td>1.78</td>
<td>1.45</td>
</tr>
<tr>
<td>B</td>
<td>0.50</td>
<td>2.15</td>
<td>1.33</td>
<td>1.65</td>
</tr>
<tr>
<td>C</td>
<td>0.30</td>
<td>3.13</td>
<td>1.72</td>
<td>2.83</td>
</tr>
<tr>
<td>D</td>
<td>0.45</td>
<td>4.00</td>
<td>2.23</td>
<td>3.55</td>
</tr>
</tbody>
</table>
The worst trouble occurs when the load is capacitor-coupled. This is very common for instrument inputs and outputs. In this case, AC load currents can be positive or negative. Figure 5 shows the performance of the amplifiers driving 300Ω to ground and 300Ω to V+, emulating a capacitor-coupled 150Ω load.

Generally, then, in single-supply amplifier circuits, signals will be offset above ground with capacitor coupling and DC-restoration used to regain offset levels.

### Table 3. Amplifier Output Swings for 0.4% or 0.4° Deviation from Curves in Figure 5

<table>
<thead>
<tr>
<th>Amplifier</th>
<th>Low Swing</th>
<th>High Swing</th>
<th>Span Center</th>
<th>Total Span</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.70</td>
<td>2.83</td>
<td>2.27</td>
<td>1.13</td>
</tr>
<tr>
<td>B</td>
<td>2.45</td>
<td>2.80</td>
<td>2.63</td>
<td>0.35</td>
</tr>
<tr>
<td>C</td>
<td>1.15</td>
<td>3.45</td>
<td>2.30</td>
<td>2.30 -0.5%/0.5°</td>
</tr>
<tr>
<td>D</td>
<td>0.73</td>
<td>2.00</td>
<td>1.36</td>
<td>1.27</td>
</tr>
</tbody>
</table>

Again amplifier A does not have enough swing for our video signal. Amplifier B fails altogether without a pull-down resistor. With the pulldown B’s performance will be very close to that of Figure 4. Amplifier C shows crossover distortion but has a good swing, if we allow the error to increase to 0.5% and 0.5°. Amplifier D has terrible crossover distortion and a very restricted output range, so is useless for driving bi-directional load currents.
Figure 5. Differential Gain and Phase Error, $A_V = 2$, $R_L = 300 \text{ to } V_{CC}$ and 300 to Ground, $V_{IN} = 0V - 2.5V$, DG = 0.1%/div, DP = 0.2°/div

The transient response curves shown in Figure 6 present another approach to studying distortion when the output is driven toward ground. All amplifiers are wired in unity gain configuration and powered with a +5V single supply and drive 150Ω load. The input is a 1 MHz 4 $V_{p-p}$ sinewave with its minimum voltage at 0V. Amplifier A output clips are around 250 mV. Amplifiers B and C output linearly go down to 50 mV above ground. Amplifier D, even though it can reach 80 mV from ground, shows a saturation recovery step at 475 mV. Voltage clipping and saturation recovery directly translate to differential gain and phase errors.
Figure 6. Transient Response, $A_V = 1$, $R_L = 150$

Conclusion
High-frequency op-amps' linearities suffer greatly in single-supply service. To optimize video performance it is helpful to level-shift the signal, possibly with a DC-restore system. Specially designed single-supply amplifiers offer the widest swings, but have serious limitations and behaviors that must be measured individually.
Reliability and the Electronic Engineer
by Barry Siegel

Introduction
There is probably no more crucial issue than Reliability at the system level to both the component vendor and the systems house, and surprisingly there is very limited understanding of the mechanisms that yield to failures. This paper sets forth simply what the electronic Design Engineer needs to know with regard to calculating a given component’s Mean Time Between Failure (MTBF), Failure Rate (FR), Failures In Time (FITS), and what all this jargon means.

Reliability Overview
Contrary to popular opinion, all integrated circuits begin “dying” the moment they are born, and in general, raising the average junction temperature will result in increasing the failure rate. The Arrhenius relationship which is common in many physical and chemical processes has been found to fit the failure rates in IC’s as well. Equation (1) expresses the relative failure rate for temperatures, $T_1$ and $T_2$, and the ratio, $R_2/R_1$, is often referred to as the Acceleration Factor.

\[
\frac{R_2}{R_1} = e^{-\left(\frac{E_A}{K} \frac{T_2}{T_1}\right)}
\]

Where:
- $R$ = Failure Rate
- $E_A$ = Activation Energy
- $T$ = Absolute Temperature (°K)
- $K$ = Boltzmann’s Constant ($1.38 \times 10^{-23}$)

One very significant issue is the assumed Activation Energy. Illustrated in Figure 1 is the Failure Rate for 0.5 eV and 1 eV as a function of temperature. Significantly, at junction temperatures above 100°C, the failure rate at 1 eV is 1,000 times that of 0.5 eV.

Reproduced in Figure 2 are the reported Activation Energies for various kinds of components. At Elantec, we use 0.8 eV to 1.0 eV, which is best suited to the kinds of processes that we employ.

In order to calculate MTBF we will also need to obtain reliability data from the IC vendor. Virtually all manufacturers routinely run life tests on devices which span their product line and package repertoire. Life test usually means placing devices in a burn-in oven, under power, at temperatures which are typically set at 125°C for 1,000 hours or more. Shown in Figure 3 is data taken from a slice in time for a variety of devices manufactured by Elantec. As indicated, a total of 692 devices were tested at 125°C, and the total device hours were 867,520. Failure Rate and MTBF are given by:

\[
FR = \frac{\text{No. of Failures}}{\text{Total Device Hours}}
\]

\[
MTBF = \frac{1}{\text{Failure Rate}}
\]

Using Equation (1) and assuming that the Activation Energy is 1 eV, we calculate an Acceleration Factor of:

\[
\frac{R_2}{R_1} = e^{-\left(\frac{E_A}{K} \frac{T_2}{T_1}\right)} = e^{-\left(\frac{1.6E - 19}{1.38E - 23} \left(\frac{1}{398°K} - \frac{1}{298°K}\right)\right)}
\]

Then we multiply the 125°C MTBF of 433.8 hours by 17,698 to obtain 7.7 billion hours and corresponding FR of 0.13 per billion hours.

Another often heard term is FITS which stands for Failures In Time and is defined as the number of failures per billion hours. For the example above, FITS is equal to 0.13.

The Real World
It turns out that the foregoing analysis isn’t quite right, and the reason is that our calculation was based on a relatively small sample of devices. To prove the point without thinking about it too much, suppose that we had observed zero failures in the earlier example. That would lead us to the false conclusion that the MTBF was infinite and the FR was zero. What do we do now?
Fortunately, we can turn to Poisson statistics to bail us out. And we all thought that the statistics course in school would never be of any benefit. Equation (4) predicts the probability (of failure), \( P(X) \), of finding \( X \) failures in a sample whose average failure rate is \( A \).

\[
P(X) = \frac{e^{-A} A^X}{X!}
\]

\( P(X) \) = Probability (of failure)  
\( X \) = Failures observed  
\( A \) = Average number of failures

Suppose we ran a large number of such life tests (say 1,000) which actually had an average failure rate of 3.12. Equation (4) predicts the probability (of failure), \( P(X) \), of finding \( X \) failures in a sample whose average failure rate is \( A \).

We should use 3.12 average failures in all of our calculations instead of our 2 observed failures, and we should always add, “to a 60% confidence level” to all the numbers we quote. So, our experimental data from Figure 3 boils down to an MTBF of 867,520 hours divided by 3.12 or 278,051 hours at 125°C to a 60% confidence level.

On the other hand, 60% confidence level doesn’t sound very confident. If we wanted to be more conservative, we could use a fudge factor from a 90% confidence level. Now our 3.12 average failures become 5.3, and that makes our failure rate and MTBF look a lot worse. Most semiconductor manufacturers have historically used 60% confidence levels.

**The Bottom Line**

To ascertain the system level FR and MTBF, we must perform a thermal analysis for a given device to calculate average junction temperature. We will then use the Arrhenius Relationship and the IC manufacturer’s reliability data and Activation Energy to predict FR and MTBF. For example, an EL2044 packaged in a plastic DIP is operated from 15V rails at an ambient temperature of 70°C. The output voltage is 2V and the load, \( R_L \), is 150Ω; the feedback resistor, \( R_F \), is 300Ω. Th quiescent power, \( P_q \), is simply:

\[
P_q = (V_+ - V_-)I_s \quad (5)
\]

The power dissipated due to load, \( P_l \), is:

\[
P_l = (V_+ - V_{OUT}) \left( \frac{V_{OUT}}{R_L || R_F} \right) \quad (6)
\]

The total power is given by:

\[
P_t = P_q + P_l \quad (7)
\]

From the datasheet, we obtain an \( I_s \) of 7.6 mA, so \( P_q \) is 228 mW. \( P_l \) is 260 mW, and \( P_t \) is equal to 488 mW.

\[
\theta_{JA} \quad \text{obtained from the datasheet is 95°C per watt which results in a junction temperature of 116°C. The datasheet states that the maximum allowable junction temperature is 150°C, so the application is okay from that point of view.}
\]

The life test circuit for the EL2044 indicates that the test is done with 15V supplies and essentially no load at 125°C under “ambient” conditions; hence, the life test data reported by Elantec would be under these conditions. The average power dissipation using equation (5) would be 228 mW, and the corresponding junction temperature per equation (8) would be 147°C.
We can now examine the predicted impact on MTBF and FR resulting from operating the junctions at 116°C. Using the Arrhenius Relationship we derive an Acceleration Factor of:

\[
AF = \frac{R_2}{R_1} = e^{-\left[\frac{1.6E - 19}{1.38E - 23} \left( \frac{1}{389^\circ K} - \frac{1}{420^\circ K} \right) \right]} = 9.0
\]

The corrected (for finite sample size) MTBF with a 60% Confidence Factor that we calculated earlier was 278K hours. To obtain the "worst case" MTBF, simply multiply by 9.0 to obtain 2.5 million hours with a corresponding Failure Rate of 0.4 per million hours.

2.5 million hours seems like a long time, but presumably there could be many devices in the system. If, for example, there were 100 amplifiers, we would expect an MTBF of about 34 months.

The moral of the story is that heat is the implacable enemy of integrated circuits. In order to insure the system reliability, junction temperature must be minimized by every available means. This might mean putting a heat sink on the package or reducing the power supply voltages, or increasing the load resistance, or all of the above.

In summary, in order to calculate MTBF or FR in a system, we need to determine the device's average junction temperature in our system, obtain the Activation Energy and Failure Rate data from the vendor, calculate the Acceleration Factor for our specific application, and correct the failure rate for finite sample size at a Confidence Factor commensurate with the system's needs.
### Activation Energy

<table>
<thead>
<tr>
<th>Component and Mechanism</th>
<th>Reported EA (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Main Population</td>
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<tr>
<td>Silicon Semiconductor Devices</td>
<td>1.0</td>
</tr>
<tr>
<td>Silicon Oxide and Si/Sio2 Interface</td>
<td>1.2</td>
</tr>
<tr>
<td>Surface Charge Accumulation, Bipolar</td>
<td>1.3–1.4</td>
</tr>
<tr>
<td>Surface Charge Accumulation, MOS</td>
<td>0.5–1.2</td>
</tr>
<tr>
<td>Slow Trapping Charge Injection</td>
<td>0.3–0.6</td>
</tr>
<tr>
<td>Metalization</td>
<td>1.0</td>
</tr>
<tr>
<td>Electro-Migration</td>
<td>1.0</td>
</tr>
<tr>
<td>Corrosion (Chemical, Galvanic, Electrolytic)</td>
<td>1.0</td>
</tr>
<tr>
<td>Bonds</td>
<td>1.0</td>
</tr>
<tr>
<td>Intermediate Growth Al/Au</td>
<td>1.0</td>
</tr>
<tr>
<td>N-Channel Si Gate Dynamic RAM</td>
<td>1.0</td>
</tr>
<tr>
<td>Slow Trapping</td>
<td>1.4</td>
</tr>
<tr>
<td>Contamination</td>
<td>0.5–1.0</td>
</tr>
<tr>
<td>Surface Charge</td>
<td>1.0</td>
</tr>
<tr>
<td>Polarization</td>
<td>0.3</td>
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<tr>
<td>Electro-Migration</td>
<td>1.0</td>
</tr>
<tr>
<td>Oxide Defects</td>
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</tr>
<tr>
<td>FAMOS Transistors</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Source: *Burn-In*, F. Jensen, N. Petersen, Wiley and Sons, New York, 1982

**Figure 2**

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Quantity</th>
<th>Failures</th>
<th>Hours</th>
<th>Device-Hours</th>
</tr>
</thead>
<tbody>
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<td>0</td>
<td>1,000</td>
<td>45,000</td>
</tr>
<tr>
<td>EL2020CN</td>
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</tr>
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<td>EL2028J</td>
<td>105</td>
<td>1</td>
<td>1,000</td>
<td>105,000</td>
</tr>
<tr>
<td>EL2020J/883</td>
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<td>0</td>
<td>1,000</td>
<td>105,000</td>
</tr>
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<td>EL2030CN</td>
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<tr>
<td>EL2033CN</td>
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<td>0</td>
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<td>105,000</td>
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<td>EL2037CM</td>
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<td>EL2190L/883</td>
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<tr>
<td>TOTALS</td>
<td>692</td>
<td>2</td>
<td>9,732</td>
<td>867,520</td>
</tr>
</tbody>
</table>

**Figure 3. Partial Summary of Elantec Reliability Data**
### Poisson Distribution Table

<table>
<thead>
<tr>
<th>X</th>
<th>Average = X!</th>
<th>3.12 P(X)</th>
<th>Sum (P(X))</th>
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</thead>
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<td>0.044157</td>
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<td>1</td>
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<td>2</td>
<td>0.214921</td>
<td>0.396849</td>
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<tr>
<td>3</td>
<td>6</td>
<td>0.223518</td>
<td>0.620367</td>
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<td>6</td>
<td>720</td>
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<td>0.960074</td>
</tr>
<tr>
<td>7</td>
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<td>12</td>
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<td>15</td>
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</table>

**Figure 4**

<table>
<thead>
<tr>
<th>Number of Failures</th>
<th>50%</th>
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<th>70%</th>
<th>80%</th>
<th>90%</th>
<th>95%</th>
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<td>2</td>
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<td>4.671</td>
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<td>12.47</td>
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<td>16.95</td>
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</tbody>
</table>

**Figure 5. Average Failures Confidence Level**
High Frequency Amplifier Instability
by Barry L. Siegel

Introduction
High frequency amplifiers pose unique, often puzzling, and frustrating instability problems which can manifest themselves as oscillation, peaking, or overshoot. This paper will address the classic causes of instability starting with the Bode plot and phase margin. Problems unique to high frequency amplifiers will then be addressed covering input capacitance, load capacitance, power supply inductance and decoupling, the use of buffers in the feedback loop, the effects of source and feedback impedance on stability and settling time, and driving loads such as flash Analog-to-Digital converters.

Classical Instability
The classical cause of instability; i.e., the one we learned in school, was due to phase shift through the amplifier which results in a feedback phase of zero degrees “around the loop.” Illustrated in Figure 1 is the Bode plot of an amplifier whose unity gain crossing frequency is about 100 MHz with a Phase Margin of about 45°. Phase margin is simply the difference between the output’s phase lag relative to the input at unity gain and 180°. Since the op amp gives us 180° gratis, the circuit would oscillate under closed loop conditions if we somehow lost the 45°. The key thing to remember is that any loss of Phase Margin will result in peaking, overshoot, or degraded settling time. Figure 2 illustrates Normalized Gain for various Phase Margins for a single pole response system. For the purpose of our discussion, any departure from an ideal response of an amplifier which results in degraded settling time, overshoot, peaking, or oscillation will be called instability.

Buffers in the Feedback Loop
There are occasions when an open loop buffer is inserted within the feedback loop to drive heavy load currents or to isolate perturbations on the output from the input. The parameter to pay attention to is the phase shift of the buffer at a frequency equal to the unity gain crossing frequency of the amplifier. The reason, of course, is that the phase lag through the buffer may be sufficient to erode or eradicate the phase margin of the amplifier, and the net result is instability. The only solution, assuming that the bandwidth of the amplifier is mandatory, is to select a buffer with sufficient bandwidth and minimum phase lag, or to put the buffer outside of the loop.

Power Supply Decoupling
Unfortunately, in the real world of high speed amplifiers, there are many and often more dominant causes for instability. Illustrated in Figure 3 is an amplifier whose power supply leads exhibit significant self inductance. The time varying load current flowing through the supply inductance induces a voltage which is essentially in phase with the input. A vestige of this voltage can be coupled to the input through parasitic capacitance on the printed circuit board (or on the amplifier) which results in instability particularly if the source impedance is high.

The obvious solution is to decouple the power supply leads. The question is with what kind of capacitor. The answer is, in general, with a ceramic disc capacitor. A surprising aspect is that 0.01 µF capacitors actually do a better job than 0.1 µF in that the latter exhibits more self inductance. Chip capacitors reduce the inductance to a minimum and should always be used when the manufacturing process allows. Recently, Tantalum electrolytics have improved but tend to cost more and take up more space. In applications requiring large output currents, Tantalum electrolytics are mandatory, and a good rule of thumb is 4.7 µF per 100 milliampere. Clearly, both rails have to be bypassed, the capacitors placed as close to the package pins as possible, and must be terminated in the ground plane.

More often than not, the compensation capacitor on the chip uses one of the rails as “AC ground”, and many amplifiers (and comparators) oscillate due to poor bypassing of the rails. Furthermore, the PSRR of most amplifiers is degraded at high frequency, and “system” noise will corrupt the signal.
**Input Capacitance**

The source impedance and any parasitic capacitance at the amplifier's input form a low pass filter and its attendant phase shift which can and will degrade the Phase Margin of the system. The change in Phase Margin is given by:

\[
d\phi = \arctan\left(\frac{f_u}{f_c}\right)
\]

where \(f_u\) is the amplifier's unity gain crossing frequency and:

\[
f_c = \frac{1}{2\pi(R_o||R_F)(C_s)}
\]

For the "simple" voltage follower of Figure 4 (\(C_s = 2 \text{ pF}\)), the degradation in Phase Margin is 51°, which means that the 100 MHz amplifier of our earlier example would oscillate.

The feedback resistor, \(R_F\), can be bypassed with a capacitor, but the optimum value is largely a function of parasitics and is always a low and non-standard number. The best solution is to keep the impedance levels as low as possible. Some amplifiers will require a small value for \(R_F\) when operated as a voltage follower. The issue in this instance is isolating the input capacitance from the output.

Current Feedback Amplifiers are simply a special case in that \(R_F\) is selected for bandwidth. The main issue here is minimizing capacitance at the inverting input.

**Load Capacitance**

A simple way looking at instability resulting from loading the amplifier with a capacitor is to assume that the open loop output impedance and the load create a low pass filter and its attendant phase shift akin to the problem created by input capacitance as shown in Figure 5. A formula similar to equation (1) results:

\[
d\phi = \arctan\left(\frac{f_u}{f_c}\right)
\]

where \(f_u\) is the amplifier's unity gain crossing frequency and:

\[
f_c = \frac{1}{2\pi(R_o)(C_L)}
\]

\(R_O\) = The Amplifier's open loop output impedance

A better way is to realize that, to the first order, the output impedance of the amplifier behaves very much like an inductor. Most amplifiers employ class AB compound emitter follower output stages, and since \(h_{fe}\) decreases as a function of frequency, \(R_O\) increases from 10Ω to 20Ω at low frequency to 100Ω or more at high frequency—precisely the behavior of an inductor. An inductor in parallel with a capacitor creates a tank circuit, and a tank circuit can and will oscillate. Whereas, this analysis is not rigorous, it does lend an intuitive insight to a straightforward technique for eliminating or minimizing load induced instability.

The technique employs the use of a "snubber"; i.e., a resistor in series with a capacitor from the amplifier's output to ground as illustrated in Figure 6. The obvious question is what value \(R\) and \(C\) should be used? The quickest answer can be obtained using an oscilloscope and operating the amplifier under conditions that it will see in the end application. The frequency of the "ring" in response to step input (or oscillation frequency) is observed, and \(R\) is calculated by:

\[
R = \frac{1}{2\pi f C_L}
\]

where \(f\) is the "ring" frequency, and \(C_L\) is the load. The value for \(C\) should be made equal to \(C_L\).

The values may have to be iterated somewhat to achieve optimum performance, but as illustrated in Figure 7, excellent results can be achieved in very short order. In this instance, the 100 MHz op amp can be tamed quite nicely using this technique.
Current feedback amplifiers offer a unique solution to this problem in that the bandwidth is determined by the feedback resistor. In this instance, \( R_F \) can be increased to a value sufficient to kill the instability but small enough to achieve the desired slew rate and bandwidth.

The classical technique is shown in Figure 8, which appears on many datasheets in applications in which the amplifier is used to drive the input (capacitance) of a flash A-to-D. The primary limitation of this approach is that 6.9 time constants will be required for the input to settle to 0.1\%, and \( R \) is chosen to keep the amplifier from peaking. The net result is that the time constant and settling time may not be compatible with the required conversion time of the system. The "snubber", on the other hand, does not impact the settling time except to eliminate the peaking.

**Ground Planes and Layout Considerations**

There is, of course, no such thing as "ground" outside of the classroom. The use of ground planes is mandatory in high speed applications. It is frankly difficult to communicate the "art" involved in the design of good ground planes in a paper like this, but there are some general rules that we will discuss. Contrary to popular notion, the ground plane should be terminated in the vicinity of the inputs to minimize input capacitance. The ground plane is also selectively removed to prevent load and supply currents from flowing near the input nodes. At Elantec, we use ground planes on both sides of a test fixture which are selectively connected at various points on the printed circuit board.

We also make extensive use of semi-rigid coaxial cable to route signals to and from a device under test. Stripline techniques can also be employed, but take longer to develop. We "breadboard" critical applications using double-sided copper clad board, hand cutting the ground plane to achieve optimum performance. The final production fixture usually employs a gold plated pattern identical to the "breadboard" which we have found eliminates subtle parasitic changes. For example, one such series of boards which was developed for frequency domain testing is flat to under 0.1 dB at frequencies in excess of 500 MHz. In the final analysis, most manufacturers offer "demo boards" for use with their products, and they are an excellent platform to initiate breadboard testing and a basis for your artwork.

**Component Selection**

Let's eliminate one component right off the bat. Don't use a socket particularly for SO packages. If you are compelled to offer removability, use pin jacks for DIP packages.

As suggested earlier, chip capacitors and resistors are best for high frequency applications. Metal film construction may be mandated in some applications, and it is, therefore, very prudent to ascertain a given resistor's self-inductance on an impedance bridge before using in production. Clearly, an inductive resistor used as a gain setting resistor is an invitation to disaster. Carbon film resistors with their leads cut to \( \frac{1}{16} \) of an inch exhibit excellent high frequency characteristics.

**Oscilloscope Probes**

We have no quarrel with probes, but they do require matching and calibration, exhibit fairly high input capacitance, and grounding is always a problem. For example, the Tektronix P6137 10 MΩ probe recommended for use with 2465 oscilloscope exhibits an input capacitance of about 12 pF which translates to 37Ω at 400 MHz. The first thing to do is to throwaway the alligator clip. Chassis mounting probe tip jacks such as the Tektronix part number 131-0258-00 can be soldered directly to ground plane, or alternatively, the Tektronix 013-0084-01 probe tip adaptor can be used in conjunction with a standard BNC coaxial connector. Lastly, remember there can be bandwidth or rise time contraction which results from "RMS-ing" the probe and instruments bandwidths.

At Elantec, we tend to "roll your own" scope and network analyzer probes as illustrated in Figure 9. The mismatch created by the 450Ω resistor is minimal, tpd skew is much, much less than 1 ns for equal lengths of coax, any gain ratio can be used assuming that the amplifier can drive the impedance, and capacitive loading is minimal.
Diagnostics and Conclusion
The frequency at which an amplifier is oscillating or peaking can, ironically, be a clue as to the cause. For example, if the amplifier is oscillating at several hundred Megahertz, the odds on bet is that the output stage whose transistors exhibit ft's in that range is the problem. If the load is capacitive, a snubber may be in order. Power supply bypassing problems also result in oscillations (or ring frequencies) in that range. If the oscillation is detectable on the power supply, the bypassing is inadequate. On the other hand, if the problem is at or close to the gain-bandwidth product, loop oscillations caused by input capacitance or source impedances is the likely culprit.

High speed analog applications stripped of their mystery are no more difficult to design or troubleshoot than precision circuits, for example. Follow a few simple rules, and when all else fails, call the vendor’s Applications department.

Bibliography
Figure 3. Power Supply Induced Oscillations

Figure 4. Source Impedance Effects

Figure 5. Capacitive Loads

Figure 6. Snubbers
Figure 7. Response with and without a Snubber

Figure 8. "Standard" Technique

Figure 9. Make Your Own Oscilloscope Probe

Equal Length Coax, L ≤ 1M
Practical Current Feedback Amplifier Design Considerations
by Barry Harvey

The current-feedback (CMF) amplifier is a fundamentally different approach to high-frequency gain blocks. Not just an input stage, it is a full amplifier topology. It has outstanding characteristics in several areas: very high slewrates, -3 dB bandwidth which is almost constant with increasing circuit gain, and low high-frequency distortion. Almost all commercial CMF products offer these benefits, but, sadly they also exhibit limitations that are seldom publicized. This article is intended to point out the theoretical basis for the CMF amplifier’s strengths and weaknesses, and some ways of coping with its problems.

Figure 1 shows the modern fundamental CMF circuit, with feedback applied through $R_F$ to implement an operational voltage follower. Q1 through Q4 form a complementary buffer. The terminal called $-\text{Input}$ is thus actually an output, a buffered replica of the voltage at $+\text{Input}$. Q3 and Q4 idle at a quiescent current proportional to the geometric mean of I1 and I2 and a scale factor dependent on the relative sizes of Q1 through Q4. When the feedback loop is at null, no error current will flow to the $-\text{Input}$, and Q3 and Q4 draw equal collector currents (we will ignore base current errors in this discussion). Q3’s collector current is mirrored by Q8 and Q9 and delivered to the gain node. Q4’s collector current is mirrored by Q5 and Q6 and sent to the gain node to balance against the previous mirrored current. Transistors Q11 through Q14 buffer the voltage at the gain node and present it as the output voltage.

Figure 1. A Typical Current-Feedback Amplifier Connected as a Unity-Gain Follower
To understand the behavior of the circuit, imagine that the + Input and the output had been resting at zero volts and a one-volt positive step is delivered to the + Input. The input buffer Q1 through Q4 will very quickly replicate the step at the − Input terminal and the step voltage is thus impressed upon the feedback resistor $R_F$, since the output has not yet had time to move. Let us assume that $R_F$ is 1 kΩ, a typical value. The one-volt step then will cause a transient one milliampere current to flow through $R_F$, increasing Q3's current by 500 μA and decreasing Q4's current by 500 μA. Q9's collector current will then increase by 500 μA and Q6's collector current will decrease by 500 μA, assuming the current mirrors have a gain of one. The milliampere of transient error current through $R_F$ thus is transferred to the gain node of the amplifier and serves to slew the node positive, at a rate determined by $C_{COMP}$. The output, following the gain node, will move positive until equilibrium is reached where no current flows through $R_F$ and currents to the gain node balance.

Slewrate

The output slewrate is the feedback current divided by $C_{COMP}$. If the input step were increased to two volts, twice the previous error current would flow through $R_F$ and twice the slew current delivered to $C_{COMP}$, yielding twice the previous slewrate. Even if the error current through $R_F$ exceeded the quiescent idle currents through Q3 and Q4, one of the two transistors would simply turn off and all error current would be delivered through the other transistor and associated current mirror in class A-B operation. In essence there is no slewrate limit in the conceptual CMF amplifier, and all step inputs produce the ideal single-pole exponential output response.

The high-frequency advantages of the CMF topology are manifold. The absence of slew limitation yields low distortion for large and high-frequency signals, even up to the normal small-signal bandwidth limitation. Since slew current is produced by the feedback error signal, the idle currents can be low without seriously affecting slew rate. And as we will see, the bandwidth is determined mainly by $R_F$ and $C_{COMP}$ and does not diminish rapidly with increasing closed-loop gain.

As in all circuits, there are limitations. We will consider time domain aberrations first. For increasingly large input steps and slewrates, the error current through $R_F$ also increases. A fast 10 V input step could produce a 10 mA peak error current, and this would not be supportable in many amplifiers. Typically, transistors in the current mirrors would saturate during the transient, causing slew and settling aberrations. Monolithic amplifiers support 500 V/μs to 2000 V/μs slew-rates, but many devices display full-out step response that is “out of control”. Saturation also occurs more readily at high temperatures, and takes longer to settle out, so amplifiers that seem to not exhibit saturation distortions at room temperature often do when hot.

The other slew distortion mechanism is input stage slew limitations. Q1 has an essentially unlimited positive slew capability, but its negative-going slewrate is limited by I1 and parasitic capacitance at Q1’s emitter. Q2 similarly is not restricted in its negative-going slewrate, but I2 limits its positive slewrate. The result is that the replicated voltage presented at − Input is limited in each direction of slew by the respective current-source and parasitic capacitance. The maximum input slewrate might be less than the output slewrate (the slew allowed by the supportable error current from $R_F$ mirrored to $C_{COMP}$), or it may be more. If the input slewrate is less than the output slewrate, − Input will “float” toward the new + Input voltage and the output will follow that slew-limited response.

Some CMF amplifier designs are simply not recommended for positive gain connections. These amplifiers are to be connected in inverting gain mode so that the + Input does not see signals at all. Their + Input is not a high impedance and does not offer good input slewrate.

This is the ultimate workaround to input stage limitations: connect the amplifier as an inverter.
This runs counter to most instrument designs, and as we will see, can often be inconvenient in many other ways. Fortunately, there are many CMF amplifier products designed to work well in the non-inverting mode.

Settling Behavior
With their large slewrates, one would expect the CMF amplifier to settle very quickly to high accuracies. This is only partly true; the CMF amplifier can settle very fast to moderate accuracies but displays large thermal settling tails. To see why this is true, consider the offset voltage between −Input and +Input. There is the difference of \( V_{be}(PNP) - V_{be}(NPN) \) at −Input relative to +Input. If we raise +Input by one volt, Q1 will dissipate less power since its \( V_{ce} \) was reduced, and \( V_{be}(NPN) \) will increase slightly as the transistor cools. Conversely, Q4 will gain a volt in \( V_{ce} \) so its \( V_{be}(PNP) \) reduces as it warms. Unfortunately, the drift in \( V_{be} \)'s do not cancel. Note that these are device thermals; the device dissipates power just under its emitter in the collector region. The heat source is so physically small that it spreads and diminishes in a space smaller than the overall size of a transistor, and no device-to-device thermal coupling can be employed in an integrated layout to remove the effect.

To get an idea of the magnitude of the thermal settling errors, let us assume all transistors run at quiescent currents of 1 mA and that each device has a 70°C/W thermal coefficient. Each transistor changes dissipation by 1 mW, causing a 0.07°C temperature change. Since a silicon junction voltage changes by 1.7 mV/°C each device \( V_{be} \) changes 120 μV, for a total thermal error of 240 μV per volt of input. This 0.024% thermal error eliminates any concept of 0.01% settling, at least in positive-gain connections, and most CMF amplifiers are specified for 0.1% settling times instead. Figure 2 shows the settling response for an EL2020 to a 10V step in unity-gain connection. It settles very quickly to 0.1% bounds, 70 ns for a 10V step, but has a thermal input tail that pushes 0.01% settling much longer out.

Further settling aberrations can be generated as feedback current errors into the −Input terminal. The current errors are multiplied by \( R_F \) to contribute an output voltage error. Assuming the current mirrors have a unity gain, any current variation into the gain node has a direct contribution to the feedback error current. The main source of error current, as far as settling is concerned, is thermal error within the current mirrors. There are two popular topologies of CMF design where in one case the current mirrors add little to feedback current errors and in the other case their effect dominates all other settling errors. The simple two-transistor current mirrors Q5/Q6 and Q8/Q9 shown in Figure 3 is an example of the error-prone kind.

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**Figure 2. Short-Term Settling Characteristic of EL2020 (Unity Gain Mode)**

Further settling aberrations can be generated as feedback current errors into the −Input terminal. The current errors are multiplied by \( R_F \) to contribute an output voltage error. Assuming the current mirrors have a unity gain, any current variation into the gain node has a direct contribution to the feedback error current. The main source of error current, as far as settling is concerned, is thermal error within the current mirrors. There are two popular topologies of CMF design where in one case the current mirrors add little to feedback current errors and in the other case their effect dominates all other settling errors. The simple two-transistor current mirrors Q5/Q6 and Q8/Q9 shown in Figure 3 is an example of the error-prone kind.
Settling Behavior — Contd.

Figure 3. Long-Term Settling Tail of EL2020 (Unity Gain Mode)

Let us assume that $R_F = 1 \text{k}\Omega$ and $R_e = 300\Omega$. Assume the gain node and output voltage move by one volt in response to a signal. Further assume that Q6 and Q9 have 1 mA quiescent current and have a $70^\circ C/W$ thermal coefficient. As in the previous thermal calculation, the volt of $V_{ce}$ change across the transistors will cause a 0.07°C temperature change in the device, for a $V_{be}$ change of 120 µV. The diode-connected transistors Q5 and Q8 do not share in this temperature change, so the $V_{be}$ change, divided by $R_e = 300\Omega$, creates a 0.4 µA error into the gain node. This error is doubled and reflected as a current error into $-\text{Input}$. The 0.8 µA error, multiplied by $R_F = 1 \text{k}\Omega$, yields an additional 0.08% thermal settling error.

This simple current mirror offers the widest bandwidth, greatest high-frequency linearity, most docile behavior for its bandwidth, and transient current capability, but much worse thermal errors than the more common Wilson type. Generally, CMF amplifiers whose transimpedance is greater than 150 kΩ have Wilson mirrors.

Figure 4. Short-Term Settling Characteristic of EL2020 (Inverting Gain of −1)
Settling Behavior — Contd.

Figure 4 shows the settling response of the EL2020 connected in inverting mode (Av = -1). Because the input stage does not have to move with the signal, it does not add thermal error and only —Input error current limits settling quality. Although the 0.1% settling time is slowed to about 100 ns, the amplifier can now settle to 0.01% in 130 ns. As the figure shows, the settling tail reduced from the 0.024% size of Figure 2 to 0.007% in this connection.

![Figure 4. Magnified Short-Term Settling Characteristic of EL2020 (Inverting Gain of -1)](image1)

In any event, the CMF amplifier is still prone to load-driving thermal feedback effects. The input and current mirror stages are very hard to place on an IC so as to completely reject temperature changes on the die emanating from the output transistors. In general, if quality settling or best DC accuracy is desired, the CMF amplifier should be loaded as lightly as possible. 50Ω or 75Ω systems are poor choices for moving quality settling signals; direct device-to-device connection is best to avoid load-induced thermals.

Ultimately, the CMF is not the best choice for very high-accuracy settling, although it excels in the 8-10-bit realm. At 12-bit accuracy and above, properly designed traditional voltage feedback amplifiers dominate.

![Figure 5. Magnified Short-Term Settling Characteristic of EL2020 (Inverting Gain of -1)](image2)

![Figure 6. Long-Term Settling Tail of EL2020 (Inverting Gain of -1)](image3)
Gain Accuracy

Figure 7 shows the small-signal macro-model of a CMF, used in positive-gain connection. The input buffer presents a copy of the + Input to the -Input terminal, but has an output impedance of $R_{IN^-}$. The dotted line emanating from the side of the input buffer represents a connection to a current source whose value is a copy of the current flowing into -Input. This current is applied to the gain node, which is loaded at DC by $R_{OL}$ and over frequency by $C_{COMP}$, the compensation capacitor. The external gain-setting resistors are the previous $R_F$ and an added $R_G$. Finally, $C_{IN^-}$ is the external parasitic capacitance at the -Input terminal.

The added term is near unity since $R_{OL}$ is a large number. This term is the gain accuracy expression as a function of amplifier characteristics and feedback resistors. The gain error can be approximated as

$$Gain\; Error = \frac{R_F + A_0 \cdot R_-}{R_{OL}}$$

The ideal gain of the fed-back amplifier is:

$$\frac{V_O}{V_{IN}} = \frac{R_F + R_G}{R_G}$$

which we will term $A_0$.

The precise expression for the fed-back gain is

$$\frac{V_O}{V_{IN}} = A_0 \cdot \frac{1}{1 + \frac{R_F + A_0 \cdot R_-}{R_{OL}}}$$

There is no occurrence in the equations of $A_{VOL}$, the open-loop gain of the CMF amplifier. Actually, $A_{VOL}$ is an "imaginary" parameter which is a holdover from voltage-feedback days and has no meaning with respect to the CMF amplifier. Unfortunately, few data sheets offer $R_-$. $R_-$ can be estimated as

$$R_- = \frac{R_{OL}}{A_{VOL}}$$
Gain Accuracy — Contd.

This is mathematically exact, but the typical R\textsubscript{OL} and A\textsubscript{VOL} numbers offered in data sheets may not give precise estimates of R\textsubscript{–}. For CMF amplifiers drawing supply currents around 16 mA, R\textsubscript{–} ranges from 10Ω to 25Ω; for lower currents around 8 mA, R\textsubscript{–} typically increases to 50Ω. Using R\textsubscript{OL} = 1 MΩ, R\textsubscript{–} = 50Ω, and R\textsubscript{F} = 1 kΩ, the gain error is 0.105% for unity feedback gain and increases rapidly beyond a gain of 20. This is a key consideration in the CMF amplifier: gain accuracy is seldom as good as in most voltage-feedback amplifiers.

Furthermore, gain accuracy reduces with heavy output loading since the output buffer reflects the load as a reduction in R\textsubscript{OL}. The CMF is seldom used for closed-loop gains of more than 50, since amplifier gain and the value of R\textsubscript{G} become too small to retain gain accuracy.

On the other hand, the gain accuracy did not reduce appreciably between the closed-loop gains of 1 and 10. This gain range is the “sweet range” of CMF amplifiers. Note that this relatively limited gain accuracy does not suggest a non-linear situation; the CMF is much more linear open-loop than voltage-feedback amplifiers and does not rely on massive voltage gain to be linear in feedback.

This discussion of gain accuracy was based on open-loop gain; there are three subtle aberrations that make this value optimistic. The first effect is the input common-mode rejection ratio, or CMRR. This effect places an offset on the input proportional to the signal level on the +Input terminal. The offset is indistinguishable from an input signal, and in non-inverting gain configuration creates a gain error. The typical CMRR for the CMF amplifier is 50 dB to 60 dB, so that gain error can be as poor as 0.3%.

The second gain error is due to voltage sensitivity in the +Input terminal’s bias current. As the +Input terminal voltage moves with signal, early errors between Q3 and Q4 modulate their alphas and thus mismatch their quiescent collector currents. The mismatch in currents must be made up for as Input bias current variation. The term for this effect is −ICMR. A −ICMR error, multiplied by R\textsubscript{F}, creates an output error similar to CMRR errors. −ICMR quantities range from 0.2 μA/V to 10 μA/V. In our CMF amplifier example −ICMR would be around 1 μA/V. Using a 1 kΩ feedback resistor would create an output error of 1 mV/V, indistinguishable from a 60 dB CMRR input error in unity gain connection. The −ICMR error is an output error, and reduces in input effect as the overall feedback gain is increased. For instance, a gain of +10 causes −ICMR errors to be ten times less significant.

The third such error source is the thermal settling error previously discussed. At frequencies below 1 kHz, the settling error is indistinguishable from CMRR or open-loop gain limitations. At frequencies above 100 kHz, however, thermal time responses are too slow to make appreciable errors, and gain accuracy can actually improve. The amplifiers will show a small drop in gain below these frequencies and a small increase in gain above. The variation in gain is about the same magnitude as the settling tail. Thus, the better-settling CMF amplifiers will show thermal errors too small to affect overall gain accuracy over (low) frequency, while the poorest-settling amplifiers can display as much as a 0.2% gain bump in mid-band frequencies.

Frequency Response

For the best gain accuracy, therefore, the inverting connection should be used. Ideal frequency response is calculated by inserting C\textsubscript{COMP} in parallel with R\textsubscript{OL}:

\[
\frac{V_O}{V_{IN}} = A_0 \times \frac{R_{OL}}{(R_{OL} + R_F + A_0 \times R_-) + s C_{COMP} R_{OL} (R_F + A_0 \times R_-)}
\]
Frequency Response — Contd.
The $-3\text{dB}$ bandwidth of this expression occurs at a frequency of

$$F_0 = \frac{1}{2\pi C_{\text{COMP}} (R_F + A_0 \cdot R^-)} \cdot \frac{R_O + R_F + A_0 \cdot R^-}{R_O}.$$ 

The term on the right is quite close to unity for any CMF application and will be ignored. Since $A_0 \cdot R^-$ is usually much less than $R_F$, $R_F$ dominates the expression for bandwidth over a wide range of closed-loop gain. This gives a bandwidth relatively independent of gain (or $R_G$), a major advantage for the CMF amplifier. The bandwidth falls to $\frac{1}{2}$ of maximum when the gain is equal to $R_F/R^-$, or 20 in our example.

This first-order analysis ignores the effect of $C_{\text{IN}}^-$ and is an expression of what we will refer to as the "natural bandwidth" of the CMF amplifier. We will use the term natural instead of dominant pole because the pole is not completely dominant in every CMF design. The effect of $C_{\text{IN}}^-$ is to insert a secondary pole in the frequency response of the circuit. This secondary pole usually coincides with the output resonance of both the input and the output buffers, and the overall frequency response is further complicated by phase delays in the current mirrors.

Figure 8 is a simulation of the frequency response of the idealized circuit of Figure 7 at unity gain with a variety of $C_{\text{IN}}^-$ values, for a $C_{\text{COMP}}$ of 3 pF. With a $C_{\text{IN}}^-$ of zero, the frequency response is single-pole in nature and the $-3\text{dB}$ bandwidth coincides with the "natural bandwidth". With increasing $C_{\text{IN}}^-$, a high-frequency zero is introduced which tends to maintain gain over frequency. At a gain of +1, the zero caused by $C_{\text{IN}}^- = C_{\text{COMP}}$ would potentially cancel the pole caused by $C_{\text{COMP}}$ itself. Unfortunately, nature is not so generous and this is an unattainable trick.

Figure 9 shows the effect of $C_{\text{IN}}^-$ on a realistic CMF model. The current mirrors and output stage were modeled as having 200 MHz single-pole bandwidths each, a realistic value in our example where the natural bandwidth is 50 MHz. The limited bandwidths of the mirrors and output stage cause $C_{\text{IN}}^-$ to produce different aberrations. $C_{\text{IN}}^-$ still causes the bandwidth to expand, but at the expense of peaking. Peaking causes undesirable ringing in transient responses, and about 2dB of peaking is generally a gracious maximum. Only about 2.5 pF of $C_{\text{IN}}^-$ can be tolerated for 2dB of peaking in our example, and this is a practical value. However, $R_F$ and $R_G$ must be connected directly to the $-\text{Input}$ pin on the package to maintain so small a parasitic capacitance, and a socket is probably too capacitive to use.
Settling Behavior

The small tolerated values of \( C_{IN}^- \) scale with the effective \( C_{COMP} \) of the CMF amplifier. Higher values of feedback resistor require smaller \( C_{COMP} \) for a given natural bandwidth and thus less \( C_{IN}^- \) can be tolerated. Since 1.5 pF is a minimum practical value for the parasitic \( C_{IN}^- \), almost no CMF designs use \( R_F \) values greater than 1.3 kΩ. Higher frequency amplifiers use \( R_F \) values around 300Ω to mitigate the \( C_{IN}^- \) problem.

As shown in Figure 9, our natural bandwidth of 50 MHz was expanded to a −3dB frequency of over 100 MHz. This design is typical for the moderate supply current devices; there is not enough quiescent current to maximize the current mirror and output stage bandwidths. Higher supply current amplifiers or amplifiers built from very high-frequency IC processes have more bandwidth in the mirrors and output stage and display less peaking for a given bandwidth and give more reproducible frequency responses. Our definition of "moderate" supply current will again be CMF amplifiers that draw about 8 mA–10 mA; optimized amplifiers draw around 16 mA.

The ratio of −3dB frequency to natural bandwidth is an interesting number. In high frequency circuits it is always greater than unity. The closer to unity this "Bandwidth Expansion" ratio is, the better-behaved the amplifier. That is, a ratio close to one makes the CMF more tolerant to \( C_{IN}^- \) and varying values of \( R_F \), and it also makes the −3dB bandwidth at higher gains maximized. If the bandwidth ratio is high, say around 2, then the natural bandwidth of the amplifier is substantially lower than the unity-gain −3dB frequency, and the peaking which caused a −3dB bandwidth increase at unity gain fades and allows the more modest natural bandwidth to dominate the higher gains. Figure 11 shows this effect. The higher gains do not show peaking and the ideal bandwidth loss-vs.-gain relationship holds.

The higher-gain bandwidths can be made closer to the unity-gain −3dB frequency by reducing \( R_F \). The strategy is to make the quantity \( R_F + A_0 \cdot R^- \) constant by reducing \( R_F \) as \( A_0 \) increases. In our example, the natural bandwidth was based on \( R_F + A_0 \cdot R^- = 1050Ω \). At a gain of +10, we could reduce \( R_F \) to 550Ω and obtain maximum −3 dB bandwidth.

The Inverting Connection

When the CMF amplifier is configured as an inverting operational amplifier, as shown in Figure 11, the ideal gain in this configuration is

\[
\frac{V_O}{V_{IN}} = -\frac{R_F}{R_G}
\]

which we will term \(-A_0\).

The precise expression for the fed-back gain is

\[
\frac{V_O}{V_{IN}} = -A_0 \cdot \frac{1}{1 + \frac{R_F + (A_0 + 1) \cdot R^-}{R_{OL}}}
\]

Figure 10. Realistic CMF Response with Various Closed-Loop Gains

Figure 11. The CMF Connected as an Inverting Amplifier
The Inverting Connection — Contd.

The ideal gain error is close to that of the non-inverting case, and the ideal bandwidth also almost the same, with the $A_0$ term replaced by $(A_0 + 1)$. Because the amplifier inputs remain near ground as signals are passed, CMRR and $-1$CMR errors do not occur, and the ideal gain terms are maintained.

The inverting connection’s input impedance is essentially $R_{IN}$. With $R_F = 1\ \text{k}\Omega$, a practical maximum gain for the inverting connection is about $-20$, since the input impedance drops to $50\ \Omega$. Even if the signal source could comfortably drive very low input impedances, simple interconnect inductances reduce bandwidths beyond $100\ \text{MHz}$. The practical maximum gain is even less for CMF amplifiers that use lower value feedback resistors.

Another virtue of the inverting connection is that the sensitivity to $C_{IN^-}$ is substantially reduced. The inverting input is a virtual ground for low frequencies, and is a naturally low impedance $R$ at medium and high frequencies. Thus, the signal magnitudes are low at the inverting input and little current will flow into a $C_{IN^-}$ to upset the ideal frequency response. Figure 12 shows our previous realistic CMF amplifier model’s frequency responses with various values of $C_{IN^-}$. Note the reduced peaking from $C_{IN^-}$. With the flatter frequency response, the $0.1\text{dB}$ bandwidth improves, since the gain does not peak up and out of the $\pm 0.1\text{dB}$ bound, as does the response of the non-inverting connection due to $C_{IN^-}$. The $-3\text{dB}$ bandwidth is usually less than that of the non-inverting connection because of the diminished peaking.

It must be remembered that the input and output impedances of the integrated amplifiers are quite complex over frequency. The terminals themselves can exhibit resonances with connected impedances independent of feedback. These resonances will be exhibited generally between one and five times the natural bandwidth of the CMF amplifier. For instance, few amplifiers tolerate capacitive loading well. Those that can tolerate capacitive loading are designed to simply “wimp out” at high frequencies and lose gain accuracy and load-driving capacity. Many amplifiers do not like to see inductive or high input impedances, and some amplifiers built with very high-frequency processes resonate with $C_{IN^-}$ even in the inverting mode. This term “resonance” can mean oscillation.

Noise

Noise performance of the CMF amplifier is characterized by four quantities, as shown in Figure 13. There is the typical input voltage noise $V_n$, generally placed in series with the $+$ in terminal, the noises generated by $R_F$ and $R_G$, and a noise current $i_n$ which is peculiar to CMF amplifiers. This noise current is represented as being sent to the $-$ in terminal from internal sources.

![Figure 12. Inverting CMF Response with Various Values of $C_{IN^-}$](image1)

![Figure 13. Noise Sources in a Positive-Gain CMF Amplifier](image2)
Noise — Contd.
For positive-gain connections, the noise contributions are so:

\[ v_{\text{in,total}}^2 = v_n^2 + \left( \frac{4 K T R_F}{A_V^2} \right) + \left( \frac{4 K T R_G (A_V - 1)^2}{A_V^2} \right) + \left( \frac{i_n R_F}{A_V} \right)^2 \]

Input-referred noise is in volts-squared per hertz here. \( K \) is the Boltzmann constant, and \( T \) is absolute temperature. The noise terms are, left to right, the - Input noise current, \( R_F \) resistor noise, \( R_G \) resistor noise, and input noise current. Note that all noise contributors except the input voltage noise itself reduce in magnitude as the gain \( A_V \) increases. Since \( R_G \) can be expressed in terms of \( R_F \) and \( A_V \), we can simplify the expression:

\[ v_{\text{in,total}}^2 = v_n^2 + \left( \frac{4 K T R_F}{A_V} \right) + \left( \frac{i_n R_F}{A_V} \right)^2 \]

CMF amplifiers have low values of \( v_n \), ranging from 2 nV/\( \sqrt{\text{Hz}} \) to 8 nV/\( \sqrt{\text{Hz}} \). A 1 k\( \Omega \) resistor has a thermal noise of 4 nV/\( \sqrt{\text{Hz}} \), a value that can be neglected at even modest gains. The current noise has values ranging from 10 pA/\( \sqrt{\text{Hz}} \) to 40 pA/\( \sqrt{\text{Hz}} \). A CMF amplifier designed to use a 1 k\( \Omega \) feedback resistor would convert a typical 20 pA/\( \sqrt{\text{Hz}} \) noise current to a 20 nV/\( \sqrt{\text{Hz}} \) voltage, the largest term in the expression until \( A_V \) is greater than about 3.

Figure 14 shows the input-referred noise versus \( A_V \) for two CMF designs. One amplifier uses a 1 k\( \Omega \) feedback resistor, and has a 6 nV/\( \sqrt{\text{Hz}} \) input noise. The other is designed for a 250\( \Omega \) feedback resistor and has a 4 nV/\( \sqrt{\text{Hz}} \) input noise. Both amplifiers have a 20 pA/\( \sqrt{\text{Hz}} \) noise current. The first amplifier is typical of lower-power designs; the second typical of the fastest designs. Clearly, the higher supply-current amplifiers that use low-value feedback resistors are the quietest.

At low frequencies, in the audio region, \( v_n \) and \( i_n \) have 1/F excess noise. For \( v_n \), the 1/F corner is typically around 200 Hz. For \( i_n \), it is typically at 2000 Hz. These 1/F extra noise quantities do not typically increase the total integrated noise voltage much, due to the large bandwidth beyond the audio frequencies that the CMF amplifier has to accumulate thermal noise over, but they do prevent instrumentation-quality DC performance.

Figure 14. Noise vs Gain for Two CMF Amplifiers

Summary
The CMF amplifier has virtues unavailable in the traditional voltage-feedback design and it also has its own weaknesses. Enough variety exists among CMF products so that attention to individual amplifier characteristics is required to assure optimum circuit performance.
Dielectric Isolation

Introduction
In an integrated circuit, the individual transistors must be isolated from each other for correct circuit operation. In most IC processes, this is done by using reverse biased PN junctions and the technology is referred to as junction isolation (J.I.). The degree of isolation is limited by collector-substrate leakage currents and voltage modulated collector-substrate capacitance. An ideal isolation technology would not have leakage and capacitive coupling between devices.

Elantec uses a Dielectric Isolation (D.I.) bipolar process which differs radically from conventional bipolar J.I. processes in that the individual transistors are electrically isolated from their neighbors by a layer of glass. With the Elantec D.I. process, a layer of glass (SiO₂) surrounds the transistors on all four sides and the bottom. This totally isolates the individual transistors and provides essentially ideal isolation.

Dielectric Isolation (D.I.) is a way of building monolithic integrated circuits which have performance that rivals a multi-chip hybrid.

Elantec D.I. Process
Elantec uses D.I. to make both NPN transistors and PNP transistors in a high frequency vertical structure as shown in the figure. There are two collector, two base, and two emitter diffusions. Therefore, each transistor type can be optimized without compromising its complement. In analog circuit design, both NPN and PNP transistors are in the signal path. Thus the slower of the two transistors determines the overall circuit speed limitations. Most J.I. processes use lateral structure PNP transistors which have speed characteristics (fₐ) that are 50 to 100 times slower than the NPNs. Thus most J.I. processes are 50 to 100 times slower than Elantec’s D.I. process.

D.I. also has the capability of operating at a given high frequency with lower power consumption than conventional bipolar processes of similar geometry due to the reduced collector-substrate capacitance. These stray capacitances require extra supply current to charge them, supply current that is otherwise unnecessary in the circuit.

Collector to substrate capacitances in D.I. are about one-tenth of those in J.I.

D.I. is an isolation technique and as such is a process technology platform which may be used as a starting point in more esoteric process development. Elantec’s advanced D.I. process today uses implanted resistors, MOS capacitors, and Schottky diodes in addition to high performance, totally implanted complementary transistors. Other elements may be added such as BiFETS and thin film resistors. CMOS or even combined CMOS and bipolar (BiCMOS) can be implemented on D.I. In all cases, the D.I. lend its superb isolation, low leakage, and high-speed characteristics to the process.

Elantec’s patented D.I. technology has been improved substantially from the original process. Performance and device density have been increased resulting in costs equaling that of standard J.I. Elantec’s latest process has NPN and PNP ft’s of 4 GHz at 40 V, 2 micron CMOS and very low defect density.

D.I. Benefits

Speed
Speed is improved in D.I. integrated circuits for two reasons. First, since the collector substrate capacitance is smaller than J.I. by a factor of 10, the slew rate of an internal node can be 10 times as fast as the same node in J.I., using the same amount of current. Second, it is very difficult to build fast vertical PNP transistors with J.I., so most J.I. circuits settle for using a lateral PNP transistor somewhere in the signal path. With D.I., fully isolated fast vertical PNP and NPN transistors can be made on the same chip, and therefore performance need not be compromised by a slow transistor.

Temperature Performance
All junctions have leakage currents directly impacted by temperature. Higher temperatures create higher leakages. Many integrated circuits stop working if stray leakages between adjacent transistors are too high. Thus at high temperatures, these I.C.s cease working. With D.I., the
high temperature leakages between adjacent transistors do not exist and the circuit can continue to work at high temperatures. Applications such as oil wells, where the temperatures may reach 200°C, are prime examples where D.I. is necessary for its temperature characteristics.

**Radiation Hardness**

The same leakages affected by temperature are also affected by radiation. The radiation may be from either a nuclear event or from deep space radiation. Because the D.I. glass layer is unaffected by radiation, the performance of D.I. circuits in the presence of radiation makes D.I. the mandatory technology for many military applications.

**Freedom From Latch-up**

Many J.I. devices are prone to latch-up. That is, under some external conditions the circuit will become stuck in a particular internal condition and will not function properly until the power is removed. Sometimes the circuit will self destruct due to latch-up. A key factor in this latch-up is the participation of the isolation junction in the circuitry that creates a parasitic SCR (Silicon Controlled Rectifier). In D.I., since there is no isolation junction, there can be no latch-up.

**Elantec D.I. Advantages Over J.I.**

- **Speed**
  - Fast (vertical) PNP’s and NPN’s
  - Lower Collector to substrate capacitance
  - Collector to substrate capacitance not modulated by collector voltage
- **No Possibility of Circuit Latch-up via Parasitic SCR’s**
- **No parasitic devices with D.I.**
- **Operates in High Temperature and Radiation Environments**
  - Leakage currents are blocked by D.I. walls
- **High Voltage Operation**
  - Device to device breakdown > 2000 V
- **Mixed Technologies on Same Chip**
  - Bipolar transistors, diffused resistors and MOS can be done on the same monolithic chip

**Elantec Complimentary D.I. Process**

![Diagram of NPN and PNP transistors with Poly Si layers and N+ BURIED LAYER](image)
Applying Power MOSFET Drivers by Bruce Rosenthal

Overview
The EL7xxx series of high speed power MOSFET drivers achieve noteworthy improvements in speed, efficiency, input impedance, and functionality thru the application of advanced CMOS technology and novel circuit design. However, their ability to deliver high peak currents with rapid \( \frac{dv}{dt} \)'s makes them susceptible to over stress. Recommended design practices will be discussed to assist the designer in achieving reliable operation.

Common Causes Resulting in MOSFET Driver Problems

Cause 1
CMOS Latch-up: Inherent to CMOS integrated circuitry, is a parasitic SCR which can be triggered by injecting current thru any input or output pad. This occurs whenever the input/output pins exceed the supply rails by more than 0.6V. This condition may exist for any one of the following reasons.
1. During the power up/power down sequence, when voltage is applied to an input without supply voltage.
2. Ground or VDD "bounce" (relative to the input) during switching. This is often attributed to inductance in the current path.
3. Inductive kick-back from the output load.

Cause 2
Over-Voltage Spikes: Power line spikes will occur when a rapid change in current (typical during switching) is present on an inductive supply line. Exceeding the maximum supply voltage can rupture the internal transistor gate oxide, causing catastrophic failure.

Cause 3
Insufficient Overdrive: During switching, some ground bounce is going to occur. If the ground bounce is greater than the overdrive to the input, oscillation may result as the effective drive to the input is modulated. Since the typical input delay is only 20 ns, a slowly rising drive waveform will still be very close to the threshold when the output switches. The ensuing ground bounce may be enough to toggle the input.

Cause 4
Thermal Overload: The high peak drive capability of the Elantec power MOSFET drivers, far exceeds their continuous rating. Limited by the high thermal resistance associated with PDIP and SOIC packages, junction temperatures can exceed the 125°C rated maximum. Users should be aware of those factors which contribute to the total power dissipated, including quiescent current, conduction losses, and switching losses.

Guidelines for Improved Operation
The most important thing to remember in applying CMOS drivers is to minimize inductance to the power pins as illustrated in Figure 1.

![Figure 1. Trouble Prone Configuration](image-url)
Guidelines for Improved Operation — Contd.
To prevent CMOS latch-up restrict the inputs/outputs from exceeding the power rails. This may require the use of clamping diodes, output snubbers, power supply bypassing and decoupling. Effective bypassing requires a minimum path length between capacitor and supply pins. Choose a capacitor with good high frequency characteristics, such as ceramic and/or tantalum construction. Refer to Figure 2.

![Figure 2. Suggested Configuration for Driving Inductive Loads](image)

Overvoltage spikes can be controlled with decoupling. A small resistor (10Ω) from the supply, or a ferrite bead, followed by a 4.7 μF tantalum capacitor with short leads to the power pins is very effective. The suggested configuration is shown in Figure 3.

![Figure 3. Suggested Decoupling/Bypassing](image)

Sensitivity to insufficient drive is most pronounced at supply voltages greater than 12V due to the higher internal peak currents. Where high supply voltage operation is required, 0V to 5V input drive is suggested, with a minimum rise/fall time of 200 ns.

Excessive power dissipation typically results when driving large capacitive loads at high frequencies. These losses are described by:

\[ P = CV^2F \]

where

- \( P \) = Power
- \( C \) = Capacitance (Internal and External)
- \( V \) = Supply Voltage
- \( F \) = Clock Frequency

Internal dissipation can be reduced by adding an external resistor or inductor, as shown in Figure 4. Also, since the power varies as the square of the voltage, a reduction in supply voltage from 15V to 12V results in a 33% power savings.

![Figure 4. Reducing CV^2F Losses](image)
Introduction
A class of Analog to Digital Converters require closely matched differential inputs in terms of amplitude and phase. At the same time, it is also important to provide input signals that exhibit distortion levels that are at least \(-60\) dB down from nominal inputs of nominal 1V at frequencies in excess of 25 MHz. A to D's which run on a single 5V supply can be damaged or misbehave if the input range is exceeded. The circuit of Figure 1 satisfies these diverse requirements.

Circuit Description
A1, one half of an EL2260 (Dual Current Feedback Amplifier—CFA) is operated as a non-inverting gain of 2 amplifier, while A2 is connected for an inverting gain of 2. The bandwidths of these current feedback amplifiers are adjusted with \(R_{f1}\) and \(R_{f2}\) with the (noise) gains set by \(R_{g1}\) and \(R_{g2}\). The outputs are terminated in 75\(\Omega\) allowing the circuit to drive a remotely located A to D through coaxial cable or isolating the outputs from the capacitive loads of the converter. Operating the EL2260 from \(\pm5V\) supplies ensures that the input signals will not exceed the requirements of the A to D converter while using a dual CFA ensures close matching of the AC characteristics of the driver.

Performance Results
The circuit of Figure 1 achieves less than 0.1 dB and 0.1° matching between channels 1 and 2 at 20 MHz and output voltages of 1V peak to peak. Distortion was less than \(-62\) dB at the same frequency.

Conclusion
A cost effective driver suitable for driving A to D's requiring closely matched differential inputs has been presented. The driver also exhibits superb distortion and precludes damage to the A to D in the event if an overdriven situation.

\[
\begin{align*}
V_{CC} &= V_{CC} = 5V \\
R_{f1} &= R_{g1} = 590\Omega, 1\% \\
R_{f2} &= R_{g2} = 610\Omega, 1\%
\end{align*}
\]

**Figure 1.**
Linearized Voltage Control Of Delay On The EL7962/72/82C Dual Rising Edge Delay Drivers
by Stephen G. Brickles

Summary
The EL7962/72/82C Dual Rising Edge Delay Driver IC provides up to 1A of peak current for many driver applications. The rising edge of the output can be delayed from 60ns up to 1.5μs from the corresponding input edge. The block diagram of the EL7962C is shown in Figure 1. A resistor from the DSet A Pin to GND sets the delay time for Channel A and a resistor from the Dset B Pin to GND sets the delay time for Channel B. Connecting the Dset A Pin to VDD disables the delay blocks for both channels giving approximately 30ns of delay on each channel. This programmable delay is useful in applications requiring compensation for long switch turn off times and also applications using resonant mode technology. The inputs of the EL7962/72/82C are T.T.L. compatible and the Peak to Peak output voltages are dependant on the supply voltage.

In all cases, the value of the resistor is approximately proportional to the resulting delay.

This article describes an alternative method of controlling the delay, using a voltage source instead of a resistor. Unfortunately, the relationship between applied voltage and resulting delay is a non linear function. This means that the voltage must be converted before it is used to control the delay. Two methods of converting the voltage are presented here together with their relative advantages and disadvantages.

Controlling The Delay Input
The delay between the Rising Edge of the input and output waveforms is normally controlled by a resistor $R_{\text{Set}}$ connected from the Dset Pin to Ground which varies the flow of current. This sets the value of a current mirror inside the chip which controls the rate of charge of an internal capacitor (See Figure 2).

This results in the following relationship between the charging current $I$, flowing through $R_{\text{Set}}$, and the capacitor $C$ :-

$$ I_{\text{RSet}} = C \frac{dV}{dt} $$

If we relate this to $R_{\text{Set}}$, this gives :-

$$ \frac{V_{\text{RSet}}}{R_{\text{Set}}} = C \frac{dV_C}{dt} $$

Since we want to know the relationship between $R$ and $dt$, the delay time, we can re-arrange the equation to give :-

$$ V_{\text{RSet}} dt = C(dV_C)(R_{\text{Set}}) $$

This can be seen from the graph in Figure 3 which shows delay $(dt)$ versus current $(I)$ flowing through $R_{\text{Set}}$. 
Input To Output Rising Edge Delay vs Current Flowing Out Of The DSet Pin

Figure 3. Rising Edge Delay vs Current Out of the DSet Pin

However, if we want to control $dt$ using a voltage we can see that:

$$\frac{C(dV_C)}{R_{Set}} \text{ hence } \frac{dt}{V_{RSet} - V_{Th}}$$

$$dt \propto \frac{1}{V_{RSet} - V_{Th}}$$

Where $V_{Th}$ is the internal threshold voltage in Figure 2.

Thus any external circuit attached to the Dset Pin which uses voltage as the controlling parameter must perform a $1/V$ operation on the input voltage first.

Since the controlling factor in this circuit is current, then any circuit which is attached to the Dset Pin must **sink** current. This means that we must convert the controlling voltage to a variable current sink of some description.

**Using The EL4451C Multiplier**

If we wish to perform a $1/V$ operation on the input control voltage, we need some kind of mathematical circuit - one way of doing this is to use a multiplier IC. The best IC to use for this operation is the EL4451C, a two quadrant multiplier. The $V_{IN}$ input is two-quadrant whereas the $V_{GAIN}$, $V_{REF}$ and $V_{FB}$ inputs are only single quadrant.

The block diagram of this IC is shown in Figure 4.

![Figure 4. EL4451C](image)

The transfer function of this chip is as follows:

$$V_{OUT} = AV_{IN}(V_{IN}+ - V_{IN}-) + (V_{GAIN}+ - V_{GAIN}-) + (V_{REF} - V_{FB})$$

Since $AV$ is approximately 600, then $V_{OUT}/AV \equiv 0$

This means that

$$(V_{IN}+ - V_{IN}-)(V_{GAIN}+ - V_{GAIN}-) + (V_{REF} - V_{FB}) = 0$$

$$(V_{IN}+ - V_{IN}-)(V_{GAIN}+ - V_{GAIN}-) = -(V_{REF} - V_{FB})$$

If we make $(V_{IN}+ - V_{IN}-) = -V_{OUT}$

$$(V_{GAIN}+ - V_{GAIN}-) = V_{IN} \text{ and } (V_{REF} - V_{FB}) = 1V$$

then

$$V_{IN} = \frac{1V}{V_{OUT}}$$

which is what we need to achieve.
Realization Of 1/V Using The EL4451C

The circuit for a 1/V convertor using the EL4451C is shown in Figure 5.

As has been previously stated, for this application, we need to convert the voltage to a variable current sink.

Two easy ways of doing this are presented here.

Method 1 - Using An OpAmp

This method uses the classic textbook voltage to current convertor consisting of an opamp plus an NPN transistor and a resistor to sink the current. The circuit is shown in Figure 6.

The transfer equation for this circuit is:

\[ I_{OUT} = \frac{V_{IN}}{R} \]

This circuit can be added directly onto the output of the previous 1/V circuit. The Iout line is connected to the Dset Pin on the EL7962/72/82C.

The complete circuit is shown in Figure 7.

Any opamp fast enough to respond to the input will do. Any standard NPN transistor such as a 2N4400 or equivalent will suffice for TR1 here. R may have to be adjusted to maintain stability. 12K works well with an EL2044C amplifier. In addition, it can be seen from the graphs in Figure 8, that VR1 must be set to greater or equal to \(-0.5\)V for best results.

Test Results

Graphs of Output Voltage of the EL4451C versus Control Input Voltage and Input to Output Rising Edge Delay versus Control Input Voltage are shown in Figure 8.
**Figure 7. Voltage To Current Conversion Using An OpAmp**

**Output Voltage of EL4451C vs Control Input Voltage**

- With Offset of 0.5V
- Without Offset of 0.5V

**Input to Output Rising Edge Delay vs Control Input Voltage**

- With Offset of 0.5V
- Without Offset of 0.5V

**Figure 8. Graphs For Method 1**
Method 2 - Stand Alone Variable Voltage To Current Convertor

The second method involves a direct modification to the multiplier circuit and is shown in Figure 9. In this configuration, the current flowing out of the Dset Pin of the EL7962/72/82C is dependent on the voltage across the resistor R. The voltage across R will vary as the control voltage varies. Thus the current through R will vary accordingly.

Note that the VREF and VFB inputs (Pins 10 and 11 respectively) must be reversed from the previous configuration to ensure correct polarity of the current which must flow out of the EL7962/72/82C. The V_GAIN- Pin (Pin 8) needs a variable negative voltage which can be adjusted as needed using VR1. The variable V_GAIN- input control is to compensate for non-linearities in the 1/V circuit below about 0.5V. This means that the V_GAIN- input will be about -0.5V for stable operation.

D1 is included to protect the EL7962/72/82C Dset Pin from any negative voltage and can be any diode with a suitable voltage rating.

VR1 should be a Multiturn type for best adjustment. I recommend that the minimum value of R is not less than 24.1K for stable operation - this corresponds to a minimum delay of 200 ns.

IMPORTANT NOTE

It is recommended that the EL7962/72/82C be powered off a 5V to 6V supply - increasing the supply voltage will cause a corresponding increase in maximum delay, however it introduces greater instability at the lower end of the control range. The suggested values of power supply voltage, the setting of VR1 and the value of R have been chosen to provide the best configuration for greatest control range and stability.

Figure 9. Standalone Variable Current Source
Test Results
Graphs of Output Voltage across R versus Input Control Voltage and Input to Output Rising Edge Delay versus Input Control Voltage are shown in Figure 10.

Setting Up VR1
To set up VR1, measure the voltage at Pin 8 and set it to -1V. Observe the delay between input and output waveforms of the EL7962/72/82C on an oscilloscope. Adjust VR1 until instability is observed then back off VR1 until the display is stable. This should correspond to a setting of -0.5V and a minimum delay of approximately 200 ns. After setting up, in both methods, VR1's value should be measured either side of the wiper terminal and replaced by two 1% tolerance resistors to ensure temperature stability.

Conclusions
Two methods have been presented here - the first method allows the driver IC to be powered from the same supply rail as the multiplier, the second requires a lower supply for the driver which could be a limitation in certain applications. The main disadvantage of the first method is the component count - two IC's, a transistor and a resistor, the second method only needs one IC and a resistor. Both need ±1V supplies for the control inputs and ±12V supplies for the IC's. However over a certain delay span both methods achieve the objective of linearized voltage control of input to output rising edge delay.

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A Cost Effective Method for Transmitting Composite Video

Introduction
Historically, video designers have used coaxial cables to route and transmit composite video signals over distances up to several hundred feet (> 100 meters). In the last few years, however, telephone lines such as twisted pairs have been used successfully in local area networks to transmit data between data terminals and computers. Techniques similar to these may be used by video designers who want to trade the cost of a coaxial cable for the more cost effective twisted pair. For example, RG59 is currently priced at 20 to 25 cents per foot; whereas, a twisted pair cable is under 10 cents a foot. Clearly, in applications in which cable lengths are 500 feet or more, a cost trade-off can be made between a simple single-ended circuit employing a single op amp used to drive coax and a slightly more complicated differential driver using a twisted pair. Presented in this paper is such a device.

Circuit Description
In order to preserve good common mode noise rejection, a differential amplifier comprised of an EL2260, Dual 130 MHz Current Feedback Amplifier (CFA) is employed to convert the single-ended video to a differential signal as shown in Figure 1. CFA's require a known feedback resistor to set the bandwidth and slew rate, and the nominal value for the 2260 is 560Ω. The receiver invoked the EL2045, Gain of 2 stable 100 MHz operational amplifier hooked for a gain of 2 differential amplifier. A gain of 2 was taken in this stage to make up for the attenuation at the output A1 and A2 by resistors R10, R11, R1, and R2. R10 and R11 were used to isolate the outputs of A1 and A2 from the capacitive reactance of the line. R_G may be varied to achieve unity gain at the video output.

Performance Results
The circuit of Figure 1 provided a 3 dB bandwidth in excess of 35 MHz at the Video output, 0.1 dB gain flatness to over 5 MHz. Using a Tektronix 520 NTSC Vector Oscilloscope, the differential gain and phase were under 0.3% and 0.5° respectively. In fact, there was immeasurable difference between driving 100 meters of twisted AWG26 cable and 100 meters of RG59.

Conclusion
A lost cost alternative has been presented for distributing composite video signals. In fact, for about $5 plus a handful of 5% resistors, a significant cost savings can be realized using twisted wire in lieu of the traditional coaxial cables.
A Cost Effective Method for Transmitting Composite Video

\[ R_1 = R_2 = R_{10} = R_{11} = 100\Omega, \pm 5\% \]
\[ R_{f1} = R_{f2} = 560\Omega, \pm 5\% \]
\[ R_4 = R_5 = 220\Omega, \pm 5\% \]
\[ V_{CC} = V_{CC} = 5V \]

Figure 1
Doubling the Output Current to a Load with a Dual Op Amp

Introduction
Standard linear output current for high speed op amps is on the order of 30 mA–40 mA. When more is required, the next available options provide around 200 mA, but with a significant increase in cost and quiescent current. In these cases, it may be more cost efficient to configure a dual op amp to provide adequate output current.

Circuit Description
A common solution is shown in Figure 1. The overall gain is $1 + (R_2/R_1)$ and the output current is $I_1 + I_2$. This is only acceptable at low frequencies such as audio where the intrinsic delay of the op amp is negligible with respect to the wavelength of the input signal. At higher speeds, the output of $A_1$ will drive the load significantly before $A_2$ and the output drive will never reach twice the current.

In high frequency applications, the circuit in Figure 2 is preferable. Here the two op amps work in parallel. Since the dual package ensures the similar delay through each op amp, there will be no fighting at the output and twice the current will be delivered to the load. The overall gain is still $1 + (R_2/R_1)$.

Resistors $R_{bm1}$ and $R_{bm2}$ are back match resistors. When driving a transmission line, $R_{bm1}$ and $R_{bm2}$ should equal twice the characteristic impedance of the line to terminate it properly since they are driving it in parallel. If proper matching to a load is not necessary, then $R_{bm1}$ and $R_{bm2}$ simply isolate the outputs of $A_1$ and $A_2$, limiting the current from any output offsets. For example, if the offset voltage was 10 mV between the outputs of the two op amps, then $R_{bm1} = R_{bm2} = 5\, \Omega$ would limit the offset current to 1 mA, while allowing the maximum output voltage swing.

Conclusion
A low cost option for increasing the effective output current drive of an op amp has been presented. Twice the output current is achieved with minimal addition of complexity.
An HDSL 2B1Q Modulator Using a Multiplexed-Amplifier

by Barry Harvey

In HDSL telephony, a four-level analog modulation is used to represent two simultaneous bits of information per clock (hence 2B1Q). The levels must be accurate in voltage and have clean transitions. A 4:1 multiplexer switch is commonly used that switches between the voltage divisions between a positive and a negative reference according to code. Although the components are inexpensive, the realization requires a lot of devices. Here is the classic approach:

![Diagram of classic 2B1Q Modulator]

**Figure 1. Classic 2B1Q Modulator**
Here we need two op-amps, a quad analog switch, a 2:4 logic decoder, and a reference.

The clock rate is 2 MHz, and common analog switches do not switch quickly in this time scale, especially on ±5V supplies. The time delays can vary depending on the DC level of the divider. Further, CMOS analog switches generate large charge transients which are voltage-variable, making the received signal more difficult to decode.

Figure 2 shows the use of an EL4443 four-input multiplexed-amplifier to do the job. The logic inputs select one of four op-amp inputs which are wired for different gains to perform level selection. The gains of input stages A, B, C, D are -1, -1/3, +1/3, +1 respectively. The circuit is greatly simplified and switching transitions are over in 50 ns. The non-linearity of the circuit is around 0.2% for $R = 1 \text{k}\Omega$. Errors are caused by offset voltage and bias current of the input stages, as well as a limited open-loop voltage gain of 500.

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**Figure 2. EL4443 in Simple 2B1Q Modulator**
Figure 3 shows a similar modulator where these errors are all addressed. The resistors R1 and R2 balance feedback resistor errors caused by bias currents caused by the + inputs of the non-inverting stages. R3, R4, and R5 provide identical magnification of input offset voltages at each stage's closed-loop gain. Once the circuit sensitivities are so matched between stages, the inherent matching of offsets and bias currents bring overall nonlinearities down to 0.06%, as measured from four samples of EL4443.

The photograph shows the clean and fast transitions of Figure 3's output:
Frequency Doubling Through Full-Wave Rectification to 150 MHz

Introduction
Diode bridges are commonly utilized in full-wave rectification circuitry. However, they are incapable of handling small input signals or high frequencies. When precision and speed are desired, one must design with active devices.

Circuit Description
The circuit in Figure 1 utilizes the speed of a current feedback amplifier (EL2186) and the precision of a differential amplifier (EL2142) to provide full-wave rectification. The input signal is fed through the current feedback amplifier where only one of the two feedback paths is engaged each half-cycle. When the output is positive, current flows through D1 while D2 isolates the other feedback path. Conversely, when the output is negative, current can only flow through D2. Schottky diodes (HP 5082-2835) have been selected as D1 and D2 for their speed and low capacitance.

Each of these half-wave rectified signals is passed selectively into the high impedance differential amplifier, the positive half-cycles at its non-inverting input and the negative half-cycles at its inverting input. Since only one of the signals is active at any given time, the differential amplifier basically combines the signals. Full-wave rectification or frequency doubling is the result.

This circuit has been designed for unity gain. If more gain is desired, the gain setting resistor of the EL2186, Rgain, may be adjusted. The feedback ratio of the EL2142 could also be adjusted; but since its inherent bandwidth is smaller than the EL2186, this is not recommended for the highest operating speeds. For smaller signal inputs at midband frequencies, the gain could be split between the two stages. However, remember to limit the gain of the first stage so that it does not exceed the input voltage range of the second stage.

Conclusion
An option for full-wave rectification is presented that surpasses the limitations of standard diode bridges. High-speed active devices enable this high-frequency doubler to handle input voltages as small as 300 mV and output frequencies up to 150 MHz.
Introduction

Eight stand-alone applications of the EL4083 are presented in the parts’ datasheet. These are four quadrant multiplication, squaring, mixing, modulating, demodulating, frequency doubling, gain control and video switching. All of these are possible with either of the two basic applications schematics (see datasheet Figures 18 and 19). Also included in the sheet is a detailed discussion of the parts’ features and characteristics on a pin by pin basis in the general operating information section. This can be very useful in developing new applications or modifying the ones presented to perform a more specific task.

The applications presented in this note, except for the first divider circuit, are more elaborate designs that involve more than one multiplier or apply feedback around a multiplier. The examples chosen were either to demonstrate that the EL4083 can perform one of the classic four quadrant multiplier applications or to show some of the design’s unique capabilities. More applications are planned so contact Elantec if you want to be sure your revision of this note is the most current.

Division by Control of IZ

In Figure 1, the IZ pin is used as a denominator input to perform division. However, since the value of the current into the ZIN pin also determines the input impedance and frequency response of all the inputs as well as the supply current of the part, this considerably restricts the computational range and accuracy of this approach. It is presented for its simplicity and can produce acceptable results for a 30 dB (-30-1) range of IZ.

The key to this circuit is to run it from higher voltage supplies so that the input voltage ranges and the input resistors can be chosen large enough to minimize the input impedance modulation caused by a changing IZ. The maximum value of IZ is about 400 μA to stay within the power dissipation rating of the package. The frequency response of the denominator and the numerator inputs over a range of signal levels is shown in Figures 2 and 3 respectively. The circuit performs a multiplication as well as a division and obeys the transfer equation;

\[(I_{xy} - I_{xy}) = I_x X I_y / I_Z\]

See RMS #2 on page 8-154, and performance curves 10 and 11 in the datasheet for other hints on using the IZ pin as an input signal. A second divider circuit using feedback with a 40 dB to 50 dB denominator range and differential numerator inputs is presented at the end of this note.
Square Root operator

The circuit shown in Figure 4 calculates the function:

\[ V_{OUT} = \sqrt{V_{IP} - V_{IN}}, \quad V_{IP} - V_{IN} > 0; \]
\[ V_{OUT} = 0 \quad \text{for} \quad V_{IP} - V_{IN} < 0 \]

Like the feedback divider circuit below, it has differential inputs. An unused input in either application can simply be omitted with its series resistor. The bandwidth of this circuit is proportional to the square root of the instantaneous input signal value (see Figure 5). The Ccomp capacitors are required for loop stability and their value is chosen to be appropriate to the output op amp selected. As a rule, the faster the op amp, the smaller the value that Ccomp needs to be and the wider the bandwidth of the circuit. The critical condition for stability is at the largest input signal level since this is where the loop will have its highest bandwidth.

A square root circuit can be thought of performing a signal compression function in that the output changes 1 dB in amplitude for every 2 dB amplitude change at the input. The Figure 4 circuit can process an input referred dynamic range of about 50 dB with good accuracy. This is limited mostly by the output referred offset of the multiplier. If more dynamic range or better accuracy is required, the optional trim network shown on the figure can be used.
Wideband RMS Computing Circuit (RMS 
#1), Vector Addition-RMS Summing

Two EL4083s can be used to calculate the root-
mean-square of a wideband input signal (see Figure 6). The first multiplier calculates the mean
square of the input signal by squaring and then
averaging the output signal with capacitors. This
signal, which is differential, is then processed by
the square rooting circuit presented above. The
squarer acts as a dynamic range expander in that
its output changes 2 dB in level for every 1 dB
change at the inputs. Its low level output referred
errors limit the untrimmed system dynamic
range performance to 30 dB or 40 dB. An optional
trim network is shown in the applications fig-
ure.

The $I_Z$ bias current of the squaring multiplier
must be high enough so that the bandwidth of
the squarer will pass the highest frequency of in-
terest. The op amp in the square rooter need not
be particularly fast since the squarer's output is
immediately averaged by the capacitors. One
may also need to provide D.C. blocking capaci-
tors in front of the squarer to prevent offsets in
the input signal source from causing errors. Fig-
ure 7 shows the response of the circuit to a
10 MHz signal burst. The "lazy" tail of the decay
waveform is caused by the bandwidth of the
square root circuit contracting with signal level.
With the $I_Z$ of the squaring multiplier at its max-
imum of 1.6 mA, the system is accurate for input
frequencies up to 100 MHz.
The outputs of additional squaring multipliers can be summed into the averaging nodes which are inputs to the square root circuit. The value computed is:

\[ \text{Vvectsum} = \sqrt{\text{avg}(V_1 \times V_1) + (V_2 \times V_2) + \ldots + (V_n \times V_n)} \]

This is the RMS or vector sum of inputs \( V_1 \) to \( V_n \).

Note that the averaging function is provided by a capacitor at the noninverting current output which sources positive current only since the part is performing a squaring function. This point is then connected to the \( I_Z \) input through a resistor which completes the computing loop. The inverting current output is fed to the virtual ground input of an op amp where it is averaged and converted to a buffered voltage.

The fact that one is using a current output to drive the \( I_Z \) pin overcomes the problem that the voltage on the pin is not constant at low driving currents (see datasheet Figure 10). However, other problems associated with using the \( I_Z \) pin as a signal input, notably the bandwidth and multiplier input impedance dependence on \( I_Z \), remain.

The \( IZO \) resistor provides a default current into the \( I_Z \) pin to prevent the bandwidth from collapsing and the input impedances from becoming too high as the signal amplitude goes to zero. The value of this current is determined by the application as a trade off between dynamic range and accuracy on the one hand and bandwidth and input impedance modulation, which also affects accuracy, on the other.

Figure 8 shows the circuit's response to a signal burst. Note the effect of bandwidth modulation when the output is near zero. This circuit can be quite useful over about a 20 dB to 30 dB dynamic range given these limitations.
The major advantage of this circuit is the improvement in accuracy achieved by having the same inputs of the same multiplier do both the mean square and the square root computations. The gains are therefore identical and the effects of the offsets tend to cancel out. A high gain low offset op amp like the OP-77 is recommended at the output for the best results. Inexpensive switches such as the standard CMOS 4000 series can be used for input frequencies up to about 10 MHz. The Siliconix SD5000 series quad DMOS FET switches work well to over 200 MHz which is the maximum operating frequency of the EL4083.

An Overall detection bandwidth of 100 MHz and a dynamic range of over 40 dB can be achieved with this circuit without trimming.

Figure 10. Single Multiplier Switched RMS Circuit
RMS #3 (SW1-4 are Siliconix SD5000 Series Quad DFETS for F_{IN} > 10 MHz)
Polynomial Functions (CRT Focus and Geometry Correction)

The current inputs and differential current outputs of EL4083 lend this device extremely well to the computation of high frequency polynomial functions. Two practical examples, CRT focus and geometry correction, are shown in Figures 11 and 12. The final outputs can be used single ended or recovered differentially as discussed in the Basic Product Functions section of the datasheet. Since the seriesed EL4083 multiplier is a current mode device, very little bandwidth is lost through a complex signal chain. This idea can be expanded to arbitrary weighted sums of first order terms, squares, cubes, cross products and perhaps higher order functions.

Figure 11. CRT Focus Correction

Figure 12. CRT Geometry Correction
Wideband AGC Amplifier

The circuit in Figure 13 is a very wideband output regulating type AGC amplifier. It consists of a VCA (see datasheet Figure 23), a 100 MHz full wave rectifier/level detector and an op amp integrator. The level detector is built around the RCA CA3246 3 GHz Ft five transistor array. Transistors Q3 and Q1 rectify the positive portion of the output waveform while transistors Q4, Q5 and Q2 form an inverting amplifier which when connected to the output of Q1, completes the full wave rectifier. The Crn capacitor level shifts and D.C. blocks the signal into the input of the inverting amplifier. The Rbc resistor compensates for the effects of base currents. The 2N2222 acts as a negative clamp on the output of the inverting amplifier which enhances its speed. The Cav capacitor averages the rectified output and its value together with the value of the Rrt resistor determines the recovery time of the circuit to a signal level decrease. By connecting Rrt to the negative supply, bandwidth is maintained at low signal levels by keeping a D.C. standing current in Q1 and Q2. The nonzero value at DOUT with zero input due to current density mismatches can be compensated at the integrator input by choosing the value of Rdos such that:

\[ R_{dos} = V_{ee} \cdot R_{int} / V_{dos} \]

where \( V_{dos} \) is the zero input offset voltage.

The current source ISET, which can be fixed or variable, determines the output level to which the AGC will try to regulate. The feedback is such that a level detected above this point will cause the integrator to reduce the forward gain. The diode at the integrator output insures that only positive voltages can be presented to the control input of the multiplier. This together with Rgmin, whose value determines the minimum forward gain, prevents gain foldback around a control input of zero.

\[ V_{cc} = 5V \]

\[ V_{ee} = -5V \]

*NOTE: Low Leakage High Frequency Cap

Figure 13. Wideband AGC Circuit (Q1–Q5 are RCA CA3246 Array)
The maximum forward gain of the signal path is 15 dB with a -3 dB bandwidth of 115 MHz. One can trade off bandwidth for more gain in the EL2075 in the usual manner by scaling the RL and RF resistor values. The 500Ω input resistor is appropriate for a full scale input voltage swing of ±1V and maximizes the the gain of the multiplier for this signal level. Figure 14 shows the regulated output vs input signal level over a range of values of ISET.

![Figure 14. AGC Circuit Output Level Regulation vs Input Level at Several Values of ISET](image)

**Controlled Signal Summer/Multiplexer and Video Fader for HDTV**

A circuit that can produce the controlled sum or mix of two input signals is shown in Figure 15. This idea can be extended to any number of signal inputs if one keeps in mind that there will be some sacrifice of speed due to the summing of the device output capacitances. For producing either a final dual single ended or a differential recovered output, all the comments in the Basic Product Functions section of the datasheet apply.

A video cross fader function can be realized by a slightly modified version of the Figure 15 circuit shown in Figure 16. Note that the control voltage is common to both multipliers and one control input is offset by the current in a resistor connected to the negative supply. A control voltage moving from ground to some positive maximum value will cause the output mix to go continuously from signal 2 only to signal 1 only. The negative D.C. offset on the control input of second multiplier would invert signal 2's polarity in the sum if it's outputs were not cross connected with the first.

In Figure 17 a complementary current output DAC such as the DAC-08 or DAC-10 is used to provide the control currents for the cross fading function. Since the current outputs of the DAC are directly connected to the virtual ground inputs of the 4083s, the full current bandwidth of the DACs can be realized. The optional capacitor shown in the figure can be used to reduce switching transients if needed. The reference current for the DAC should be chosen to be equal to the full scale current selected for the multipliers. Note that the sense of both multiplier outputs have been flipped because of the negative only current sink outputs of the DAC.
Figure 16. Fader

Figure 17. Digitally Controlled Fader

*IOptional Transient Filter Capacitor*
Feedback Divider

The circuit of Figure 18 performs the function $V_{OUT} = (V_{ZP} - V_{ZN})/V_y$. This expression complies with the conventions established in the literature for such circuits and the Zs in the numerator should not be confused with the $Z_{IN}$ pin which, in this example, is run at a constant (bias) current. This type of circuit is called a feedback divider.

Figure 19 shows the frequency response of the Z(numerator) inputs as a function of amplitude with $I_Z = 1.6 \text{ mA}$ and the Y(denominator) input at its 2 mA maximum. The response is monotonic (no foldback) and has about a 50 dB to 60 dB range with good accuracy. The frequency response of the Y(denominator) input is shown in Figure 20. Note that the bandwidth is proportional to the value of the divider input. Since a division function has a singularity with the denominator at zero, a divider's performance will degrade as this value is approached. One can obtain about a 40 dB computational range with reasonable accuracy using an untrimmed part. If higher accuracy or greater range is required of this input, one can use the optional trim network shown in the figure.

The performance curves in Figures 19 and 20 are for $I_Z = 1.6 \text{ mA}$. For lower values of $I_Z$ the cutoff frequencies will be proportionally lower.

![Figure 18. Fast Feedback Divider (with Inverting and Non-inverting Inputs)](image-url)
Figure 19. Divider Frequency Response
(Denomination at Maximum, 10 dB Numerator Steps)

Figure 20. Divider Frequency Response
(Numerator at -40 dB of Full Scale, Denominator in 10 dB Steps)
Quality Programs
Forward
This document summarizes Elantec's philosophy and policies towards Quality Assurance and Reliability for both MIL-STD-883 and commercial products. It is intended as an overview only, to give the reader a quick visualization of Elantec's capabilities and standard procedures. Elantec's quality system is structured on and certified to ISO 9001.

Customers wishing more detail should refer to either "QRA-3, Elantec's 883B program for Hybrid Integrated Circuits", or contact us at the factory. Also available are "QRA-4 Hybrid S-Flow" and "QRA-5 Monolithic Class S Flow". Our facilities and process documentation are available for customer inspection at any time. We welcome you to visit us at your earliest convenience, as we believe our factory to be "our best salesman".

Philosophy
Elantec was founded on the principle of supplying Analog Integrated Circuits of advanced performance with quality levels beyond that normally available from the semiconductor industry. Our product range has been intentionally limited to service commercial, industrial and Military/Aerospace applications only. It is our firm belief that by placing quality and reliability over all other objectives, we will achieve our goal of providing our customers maximum cost-effectiveness and long term satisfaction.

Using both monolithic and hybrid technologies, Elantec provides leading edge Analog Integrated Circuit devices whose performance routinely exceeds that of most commercial manufacturers.

It is our policy to insure that each and every device is:
1) Designed to provide maximum long-term reliability.
2) Manufactured in strict compliance with thoroughly documented procedures in a tightly controlled environment.
3) Tested to insure that every device meets each parameter specified on the data sheet or customer specification.
4) Covered by a rigorous regularly scheduled Quality and Reliability Audit Program.

Commercial/Industrial Program Summary
Elantec:
- Provides the most thoroughly tested product available.
- Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.
- Performs 100% A.C. testing of critical performance parameters (see individual data sheets).
- Operates to extremely tight AQL sampling plans (see Table I).
- Provides 100% Temperature Cycling, Centrifuge, Fine and Gross Leak checks on all hermetic package commercial devices (see Table II).
- Uses superior manufacturing processes for microcircuit devices to eliminate failure modes inherent in conventional assembly techniques.
- Maintains traceability on production lots.
- Manufactures thick film substrates and performs final electrical testing of commercial devices 100% in our Milpitas, California facility.

Military/Aerospace Program Summary
Elantec:
- Provides product screened and quality performance tested in accordance with MIL-STD-883.
- Is an approved supplier to DESC/SMD drawing numbers:
  78013—similar to ELH0002H/883B
  80013—similar to ELH0032G/883B
  80014—similar to ELH0033G/883B
  85087—similar to ELH0041G/883B
  85088—similar to ELH00021K/883B
  85089—similar to ELH0101K/883B or ELH0101AK/883B
Maintains an on-going product qualification and reliability monitor program. Current quality conformance data is always available to support military product.

Manufactures MIL-STD-883 Hybrid products 100% in the United States in our facility in Milpitas, California.

Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.

Performs 100% A.C. testing of critical performance parameters (see individual data sheets).

Operates to extremely tight AQL sampling plans (see Table I).

Facilities have been surveyed and approved by major military/aerospace customers—names available upon request.

Maintains complete traceability and manufacturing history on each production lot.

Has been audited, certified, and qualified by DESC to MIL-STD-1772.

Maintains shelf stock of MIL-STD-883 product for rapid delivery at competitive prices.

 Welcomes customer Source Control Drawings, special selections and custom reliability processing.

Facility

The Milpitas factory has been certified by many customers to meet the requirements of MIL-I-45208. Defense Electronics Supply Center (DESC) has performed an audit and certified Elantec to the Hybrid Line Certification Specification, MIL-STD-1772.

All military hybrid product manufactured by Elantec is completely built in the U.S.A. at our factory in Milpitas, California, all testing is performed in Milpitas. Commercial product thick film processing and all electrical testing is done in Milpitas. Commercial assembly may be done either in Milpitas or offshore.

The factory has 46,000 square feet of space. 10,000 square feet is a Class 1000 clean room (Fed. Std 209) where wafer fabrication, assembly and electrical test are performed. All assembly operations are done under Class 100 laminar flow hoods. Temperature and humidity are monitored and controlled in accordance with MIL-STD-883. Gases are filtered at point of use. De-ionized water is filtered and bacteria controlled, and resistivity is continuously monitored. All semiconductor work-in-process is stored in nitrogen-purged desiccators.

A comprehensive ESD program is in effect. All work surfaces are either stainless steel or conductive laminate. Every work surface is grounded for Electrostatic Discharge protection in accordance with OSHA requirements. Shelving at all inventory locations is grounded. Floors in all manufacturing and inventory areas are covered with conductive tile attached with conductive tile cement. Conductive heel straps are worn by all operators. All product, commercial and military, is marked with an equalateral triangle to indicate static sensitivity in accordance with MIL-I-38535 and MIL-H-38534. Finished product is packaged in anti-static materials which are completely shielded by aluminum-lined boxes or conductive bags.

Elantec maintains complete in-house capability to 100% process devices to the requirements of MIL-STD-883 Class B. Additional in-house capability includes Particle Impact Noise Detection (PIND). All testing for initial product qualification and periodic quality conformance is performed in-house except for moisture resistance, internal water vapor, mechanical shock and vibration which are performed at DESC certified laboratories.

All manufacturing equipment is calibrated in accordance with MIL-STD-45662 as modified by MIL-I-38535 and MIL-H-38534.

Elantec maintains a complete Quality manual (QAP9000). The plan is available for review by customers at Elantec. Included within the Program Plan is a complete equipment and facilities list.
Quality System

All quality assurance functions at Elantec report to the President and are totally independent of the manufacturing organization. These functions include Incoming Quality Control, In-Process Quality Control, Product Qualification, Quality Conformance, Document Control, Customer Specification Review, Internal Quality Audit, and Failure Analysis.

Elantec's operation is controlled by a thorough documentation system. Peripheral support systems such as document control, calibration, customer specification review, the ESD program, and archives are fully documented as to procedure and responsibility. All manufacturing operations have specifications describing the equipment operation and procedures. Product manufacturing flow charts define precise operational sequences to insure each lot is built in conformance to Elantec and Military requirements. All raw materials are purchased to Elantec Procurement Documents. Military package materials and finishes are in accordance with MIL-I-38535 and MIL-H-38534.

Raw materials are inspected to rigorous requirements by Incoming Quality Control prior to release for manufacture. Minimum inspections for hybrid military products are those specified in MIL-STD-883 Method 5008 for Element Evaluation. Many of these tests are performed more often than required by the military standards. In addition, various other tests are performed to ensure the integrity of each raw material. Similar tests are performed on raw materials destined for commercial products.

Travelers used throughout Elantec are structured to maintain traceability of raw materials and operators to each manufacturing lot. Lots are shipped with accurate lot numbers on the containers to provide backward traceability should this ever be required.

In-line Quality Control gates monitor the process to insure critical manufacturing operations are under control. These include wire bond pull, die shear, die and preseal visual inspection, mark permanency, and electrical test.

Before release of any Elantec product, an exhaustive product qualification is performed. This includes life testing on multiple lots and various mechanical package tests. On-going Reliability Monitor testing is done on all Commercial product and package families. The reliability monitors include electrical and mechanical test as described in QAP0073 Military products subsequently receive complete Group A, B, C, and D per MIL-STD-883 testing prior to shipment of the first part. Military Quality Conformance testing is done in compliance with Method 5005 or Method 5008.

In Conclusion

It has been and continues to be Elantec's goal to provide product of the highest quality available. We believe the extra effort we have expended in the design, construction techniques, testing and quality control procedures results in a product which is observably superior in performance, consistently higher in quality, and provides greater reliability in the actual application. We also believe such product will provide the overall lowest cost and greatest long term satisfaction to the customer.
### Table I. QA Inspection Sampling Plan

<table>
<thead>
<tr>
<th>Test Type</th>
<th>Non-Military Lots</th>
<th>Military Lots</th>
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<td>LTPD (%)</td>
<td>Sample Size</td>
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<td>A.C. Bench Tests at Room Temp</td>
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</table>

**Note 1:** Computer tests are all D.C. tests plus A.C. on those products where A.C. can be tested on the enhanced LTX automatic tester.

**Note 2:** All military lots are Q.A. sampled at all temperatures.

**Note 3:** All non-military lots (E+, Prime, Commercial) are Q.A. sampled at room temperature (D.C.) Until adequate history is developed on these new products, each lot is sample tested at temperatures and on the bench. Non-military lots of mature products with adequate history are skip lot tested at temperatures or on the bench, e.g., they are Q.C. sampled every fourth or fifth lot. (This frequency may change with time as more product history is developed.)

**Note 4:** If a device which is in skip lot mode should suffer a lot failure, every lot is then tested until three lots in succession are passed before returning to skip lot mode.
Table II. Elantec Hybrid Metal Can Process Flow Summary

<table>
<thead>
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<th>Commercial</th>
<th>/883B(1)</th>
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<tbody>
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<td>Incoming QC</td>
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<tr>
<td>Die Evaluation</td>
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<td></td>
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<tr>
<td>Package Evaluation</td>
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<tr>
<td>Raw Material Evaluation</td>
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<td></td>
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<tr>
<td>Assembly</td>
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<td>Wire Bond Pull QC</td>
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<td></td>
</tr>
<tr>
<td>Die Shear QC</td>
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<td>Internal Visual</td>
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<tr>
<td>Seal</td>
<td>X</td>
<td></td>
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<tr>
<td>Stabilization Bake</td>
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<td></td>
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<td>TO-3, LCC (5KG)</td>
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<td></td>
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<td>TO-5 (30KG)</td>
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<tr>
<td>TO-8 (20KG)</td>
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<td>30KG</td>
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<td>Fine Leak</td>
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<tr>
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</tr>
<tr>
<td>TO-5 (5x10^8 cc/sec)</td>
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<tr>
<td>TO-8, LCC (5x10^8 cc/sec)</td>
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<td>Gross Leak</td>
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<td>Q.C. Hot(2)</td>
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Note 1: For complete details of Elantec's "/883B" military program see "QRA-3, Elantec's 883B Program for Hybrid Integrated Circuits."

Note 2: Electrical tests performed are as documented on the individual device data sheet.
Table III. Elantec Monolithic Process Flow Summary

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<tr>
<td>Raw Material Evaluation</td>
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<td>Assembly</td>
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<td>X</td>
</tr>
<tr>
<td>Die Shear QC</td>
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<td>Internal Visual</td>
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<td>Seal</td>
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<td>Temperature Cycling</td>
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<td>Constant Accel. (30KG)</td>
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<td>Fine Leak (5x10⁸ cc/sec)</td>
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<td>Gross Leak</td>
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<td>With Pressurization</td>
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<td>No Pressurization</td>
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<td>Class Test</td>
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<tr>
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<td>Q.C. Cold(¹)</td>
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<td>Group B, C, D Testing</td>
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</table>

Note 1: Electrical tests performed are as documented on the individual device data sheet.
All semiconductor devices are sensitive to Electro Static Discharge (ESD) to some degree. For this reason, Elantec treats all of our devices as sensitive. Customers are urged to use similar controls throughout their facilities. This will optimize yields, prevent latent reliability problems, and eliminate component quality complaints which are due to ESD. Even components which are returned to Elantec for analysis should be handled with proper ESD procedures.

**Device Design and Processing**
Wherever possible, ESD protection networks are used on device pins. Metal routing and oxide thicknesses are carefully considered for optimum ESD performance. Testing per MIL-STD-883 Method 3015 is used to determine device and process performance.

**Work Areas**
Floors are covered with conductive tiles, attached with conductive adhesive.

Operators wear non-static generating or static dissipative smocks. Heel straps are used to ground the operators. Heel straps are checked daily for effectiveness.

Work station surfaces are conductive laminates or stainless steel. These are tied to Earth ground through protective resistors. Grounds are routinely inspected. Air ionizers are used to neutralize charges in areas which may generate static.

Storage shelving is grounded through protective resistors.

**Handling**
All handling containers (boxes, bags, etc.) are conductive. Pink poly which depends on surface properties and may wear out is not used. Common plastics (such as polystyrene and polypropylene) which are nasty static generators are never used in the work area.

**Marking**
All devices are marked with an equalateral triangle to warn the user that they are ESD sensitive.

**Packaging**
Devices are packed in either antistatic materials which are surrounded by a conductive Faraday shield or directly in conductive materials. The shielded containers are labeled with a yellow ESD warning label. Only antistatic treated "popcorn" is used as filler material in shipping boxes.
Macromodel Information
The selected macromodels provided at the end of product datasheets are being supplied to users as an aid to circuit designs. While it reflects reasonably close similarity to the actual device in terms of performance, it is not suggested as a replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing.

Users should very carefully note the following factors regarding these models:

Model performance in general will reflect typical baseline specs for a given device, and certain aspects of performance may not be modeled fully to keep the model as simple as possible thus minimizing computer running time. For example, PSRR and CMRR effects, parametric variation with temperature, operation under output short circuit conditions, and input noise sources are not included in the models. The current mode feedback amplifiers are not slew rate limited and yield optimistic values for large signal pulse responses.

While reasonable care has been taken in their preparation, we cannot be responsible for correct application on any and all computer systems.

Model users are hereby notified that these models are supplied "as is", with no direct or implied responsibility on the part of Elantec, Inc. for their operation within a customer circuit or system. Further, Elantec, Inc. reserves the right to change these models without prior notice.

In all cases, the current data sheet information for a given real device is your final design guideline, and is the only actual performance guarantee. For further technical information, refer to individual device data sheets.

The Elantec engineering staff is in the process of improving these models, and we welcome your comments and feedback. Inquiries should be made to:

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"MACROMODELS ON DISK ARE AVAILABLE UPON REQUEST. CONTACT FACTORY OR LOCAL AREA REPRESENTATIVE.
Disks are 5½" Low Density for IBM PC Compatible Computers."
Glossary of Technical Terms
AC Coupled. AC coupling is a method of connecting a signal to any circuit in a way that removes the DC offset. The DC offset is the overall voltage level that the video signal “rides” on. One way to find the signal is to remove the DC offset by AC coupling, and then do a DC restore to add in a known DC offset (one that we selected). Another reason AC coupling is important is that it can remove harmful DC offsets.

Analog-to-Digital (A/D). This device is what all digital imaging systems use to get real-world pictures—from a TV camera, for example—into a computer. An A/D for digitizing video must be very fast, capable of sampling at clock rates of 10 to 30 million samples per second (MSPS).

Back Porch. The area of the composite video waveform following the horizontal sync pulse and right before the active video or before the terminating edge of horizontal blanking.

Bandwidth or 3 dB Bandwidth (BW, SSBW). A figure of merit of an amplifier or buffer which delineates the frequency at which the output is reduced to 0.707 (−3 dB) of the low frequency value when passing a small signal sine wave.

Black Burst. The video waveform without the active video part. Black burst is used to sync various video boxes together so that their video output is all aligned. Black burst tells the video gear the vertical sync, horizontal sync, and the chroma burst information.

Black Level. This level represents the darkest an image can get. This defines what black is for the particular image system. If for some reason the video dips below this level, it is referred to as blacker-than-black.

Blanking. On the screen, the scan line moves from the left edge to the right edge, jumps back to the left edge, and starts out all over again, on down the screen. When the scan line hits the righthand limit and is about to be brought back to the lefthand edge, the video signal is blanked so that one can’t “see” the return path of the scan beam from the right to the lefthand edge. To blank the video signal, the video level is brought down to the blanking level, which may or may not be the black level if a pedestal is used. The vertical retrace is also blanked between fields.

Blanking Level. That level of the video waveform defined by the system to be where blanking occurs. This could be the black level if a pedestal is not used or below the black level if a pedestal is used.

Breezeway. The portion of the video waveform that sits between the end of the horizontal sync and before the start of burst.

Brightness. This is the intensity of the video level and refers to how much light is emitted by the display.

Burst Gate. This is a signal that tells the systems where the color burst is located within the scan line (video waveform).

Channel Separation (CHSp, CS). A figure of merit applicable to a dual, triple, or quad amplifier which specifies the ratio of the (spurious) output voltage of an undriven amplifier to the output of a driven amplifier.

Chroma Bandpass. In an NTSC or PAL video source the luma (black and white) and chroma (color) information are combined together. If you want to display an NTSC or PAL source, the luma and chroma must be split apart. The chroma bandpass filter removes the luma information from the chroma information, leaving the chroma information relatively intact. The NTSC or PAL video signal is fed into the chroma bandpass filter, where only a certain portion of the video signal is let through the portion containing the chroma information. This works reasonably well except in certain images where the luma information and chroma information overlap, meaning that we have luma and chroma information at the same time.
Glossary of Terms

Chrominance. The NTSC or PAL video signal contains two pieces that make up what you see on the screen: the black-and-white part, and the color part. Chrominance is the color part—a.k.a. chroma.

Clamp. This is basically another name for the DC-restoration circuit. It can also refer to a switch used within the DC-restore circuit. When it means DC restoration, then it's usually used as "clamping." When it's the switch, then it's just "clamp."

Closed Loop Gain (Avcl, Av). The ratio of the output voltage to the input voltage for an amplifier which is established with feedback using one or more resistors. The non-inverting closed loop gain is given by:

\[ Av = \frac{R_f}{R_g} + 1 \]

where: 
- \( R_f \) = The feedback resistor (output to \( V_{IN-} \))
- \( R_g \) = The gain setting resistor (\( V_{IN-} \) to ground)

Inverting closed loop gain is given by:

\[ Av = \frac{R_f}{R_g} \]

Color Bars. This is a test pattern used to check whether a video system is calibrated correctly. A video system is calibrated correctly if the colors are the correct brightness, hue, and saturation. This can be checked with an oscilloscope and vector scope in the NTSC space, or by looking at the RGB levels in the RGB space.

Color Burst. Often referred to as "burst." That portion of the video waveform that sits between the breezeway and the start of active video. It tells the color decoder in the receiver how to decode the color information contained in the next line of active video. By looking at the burst, the receiver can determine what's blue, orange, or magenta. Essentially, the receiver figures out what the correct color is.

Color Decoder. This is the circuit in the video system that uses the chrominance portion of NTSC/PAL to derive the two color difference signals. The color decoder sits right after the Y/C split and before the color space convertor. The color decoder needs a 3.58 MHz signal that is accurately phase locked (PLL) to the burst. If it isn't locked well enough, then the color decoder can't figure out the right colors.

Color Encoder. The color encoder does the exact opposite of the color decoder. It takes the two color difference signals, such as I and Q in the NTSC system, and combines them into the chroma signal. The color encoder, or what may be referred to as the color modulator, uses the color subcarrier to do the encoding.

Common Mode Rejection Ratio (CMRR). A figure of merit of an amplifier or buffer which delineates the ratio of the change in input common mode voltage (peak to peak) to the change in input offset voltage (peak to peak) usually specified over the common mode range of the device.

Common Mode Range or Input Voltage Range (CMIR, CMR). A figure of merit of an amplifier, buffer, or comparator which delineates the range of the input common mode voltage relative to the power supply voltage beyond which the device will malfunction. This parameter is often "specified" implicitly by CMRR by use of a specific common mode voltage.

Common Mode Voltage (Vcm). The average of the voltages applied to the inputs of a differential input amplifier. In the case of an operational amplifier, the feedback loop strives to make the inverting input equal to the non-inverting input, and the common mode voltage is essentially equal to either input.
Composite Video. If a video system is to receive video correctly, it must have several pieces of the puzzle in place. It must have the picture that is to be displayed on the screen, and it must be displayed with the correct colors. This piece is called the active video. The video system also needs information that tells it where to put each pixel. This is called sync. The display needs to know when to shut off the electron beam so the viewer can’t see the spot retrace across the display. This piece of the video puzzle is called blanking. Now, each piece could be sent in parallel over three separate connections, and it would still be called video and would still look good on the screen. This is inefficient, however, because all three pieces can be combined together so that only one connection is needed. Composite video is a video stream that combines all of the pieces required for displaying an image into one signal, thus requiring only one connection. NTSC and PAL are examples of composite video. Both are made up of: active video, horizontal sync, horizontal blanking, vertical sync, vertical blanking, and burst. RGB is not an example of composite video, even though each red, green, and blue connection may contain composite sync, because all three connections are required to display the picture with the right colors.

Contrast. A video term referring to how far the whitest whites are from the blackest blacks in a video waveform. If the peak white is far away from the peak black, the image is said to have high contrast. With high contrast, the image is very stark and very “contrasty.” If the two are very close to each other, the image is said to have poor, or low, contrast. With poor contrast, an image may be referred to as being “washed out”—you can’t tell the difference between white and black, and the image looks gray.

Cross Conduction. A common problem in half bridge and full bridge topologies resulting in extra current flow between the upper and lower transistors during switching. This occurs when the turn-off of one transistor overlaps the turn-on of the alternate transistor.

Cross Talk (CT). See Channel Separation.

Current Feedback Amplifier (CFA). A type of operational amplifier wherein the inverting input impedance is low and is a buffered version of the voltage at the non-inverting input. A feedback resistor is always required (even when a CFA is used as voltage follower). CFA’s offer very high slew rates, high frequency linearity, and exhibit bandwidths which are substantially independent of closed loop gain.

dV/dT. The change in voltage relative to time.

di/dT. The change in current relative to time.

DAC. DAC is short for digital-to-analog converter.

DC Restoration. DC restoration is what you have to do to a video waveform after it has been AC coupled and has to be digitized. Since the video waveform has been AC coupled, we no longer know absolutely where it is. In fact, not only don’t we know where it is, it also changes over time, since the voltage level of the active video changes over time. Since the resistor ladder on the flash A/D is absolutely tied to a pair of voltage references, the video waveform needs to be referenced to some known DC level in order to digitize it correctly. DC restoration is essentially putting back the DC component that was removed to make an AC coupled signal. In trying to digitize video, the DC level that we DC restore to is such that the back porch, or the blanking level if a pedestal is present, is set to the A/D’s $-V_{REF}$ DC level. Therefore, when black is digitized it will be assigned the number zero and when peak white is digitized, it will be assigned the number 255, in an 8-bit system.
Decoder. The word “decoder” has several meanings:

- Color Decoder. See definition under Color Decoder.
- Image Compression Decoder. This is the part of an imaging system that takes the compressed image and restores it to look like the original.

Differential Gain (dG). A figure of merit of an amplifier or buffer that relates the incremental change in closed-loop gain resulting from a change in input and output voltage referenced to zero volts for a specific frequency. The gain of most amplifiers is not constant with varying DC offsets added to a constant frequency AC input signal. The parameter is most useful in applications of composite video signals and is usually expressed in percent. A standard measurement condition is for input offsets which are changed from zero to \( \pm 0.714 \text{V} \) with an input signal of 100 mV at 3.58 MHz for NTSC and 4.43 MHz for PAL.

Differential Phase (dP). A figure of merit of an amplifier or a buffer that relates the incremental change in closed-loop phase resulting from a change in input and output voltage referenced to zero volts for a specific frequency. The phase shift through an amplifier is not completely constant with varying DC offsets added to a constant frequency AC input signal. The parameter is most useful in applications of composite video signals and is usually expressed in degrees. A standard measurement condition is for input offsets which are changed from zero to \( \pm 0.714 \text{V} \) with an input signal 100 mV at 3.58 MHz for NTSC and 4.43 MHz for PAL.

Disable Time \((t_{\text{dis}}, t_{\text{off}})\). Some amplifiers provide a logic pin which enables and disables the amplifier. Usually, the supply current is reduced and the output stage is placed at a high impedance when disabled. Disable time is defined as the time from the edge of the disabling pulse to the time that the output of the amplifier falls to 50% of the pre-disabled value.

Enable Time \((t_{\text{dis}}, t_{\text{off}})\). Some amplifiers provide a logic pin which enables and disables the amplifier. Usually, the supply current is reduced and the output stage is placed at a high impedance when disabled. Enable Time is defined as the time from the edge of the enabling pulse to the time that the output of the amplifier has increased to 50% of its final (non-disabled) value.

Encoder. As with decoder, there are two meanings to this word:

- Color Encoder. See definition under Color Encoder.
- Image Compression Encoder. This is the part of the imaging system that takes the original image and squeezes out redundant information so that the image will take up less space than before.

Equalization Pulses. These are two groups of pulses, one that occurs before the serrated vertical sync and another group that occurs after. These pulses happen at twice the normal horizontal scan rate. The reason these pulses exist is to ensure the 2:1 interlacing of the NTSC or PAL systems. (See “field.”)

Fade. Fading is a method of switching from one video source to another video source.

Fall Time \((t_f)\). See Transient Response Time.

Field. A TV screen is made using two fields, each one containing half of the scan lines needed to make up one frame of video. One field contains the even-numbered scan lines while the other field is made up of the odd-numbered scan lines. Each field is displayed in its entirety—therefore, all of the odd-numbered scan lines are displayed, then the even, then the odd, and so on.

Fields only exist for interlaced scanning systems such as NTSC or PAL. So for NTSC, which has 525 lines per frame, a field has \(262\frac{1}{2} \) lines, and two fields make up a frame.
Filter. In general, a filter is used to remove unwanted information from the input signal. Every signal has a spectrum, which is the amount of different frequencies contained within the signal. Filtering lets you subtract or “filter” out certain frequencies. If you have some high-frequency information, such as noise, in with the signal that you really want, then a low-pass filter is used. A low-pass filter “passes” frequencies below a certain point and stops frequencies above that same point. A high-pass filter does just the opposite—it stops low frequencies and passes the high frequencies. A bandpass filter lets through frequencies within a certain range of “band,” but stops frequencies outside of the band.

Flash A/D. This is a really fast method for digitizing a signal. The signal to be digitized is provided as the source for one input of a whole bank of comparators. The other input is tied to a tap of a resistor ladder, with each comparator tied to its own tap. This way, when the input voltage is somewhere between the top and bottom voltages connected to the ladder, the comparators output a code. This means that all the comparators output a “yes” up to the input voltage and a “no” above that. The A/D then takes this string of Yes’s and No’s and converts them into a binary number which tells where the Yes’s turned into “No’s.” See the definition of resistor ladder for more details, if you’re interested.

Flicker. Flicker occurs when the frame rate of the video is too low.

Front Porch. This is the area of the video waveform that sits between the start of horizontal blank and the leading edge (start of) horizontal sync.

Full Bridge. Two half bridges. (See Half Bridge.)

Gain Bandwidth Product (GBW). The frequency where the open loop gain of a voltage feedback amplifier falls to one (0 dB). Sometimes the Gain is measured at a frequency lower than the one at which the gain is equal to unity. The product of the measured gain at the test frequency is then cited as GBW on the data sheet.

Gain Flatness (GFP, GFR). A figure of merit of an amplifier that delineates the closed loop deviation of the gain over a range of frequencies. It is an expression of how constant the response of an amplifier or network is over a specified range of frequencies.

Gate Oxide. The dielectric between the channel and control gate of an mos transistor.

Genlock. A video source provides all of the information necessary to view—or in the case of a computer, grab—the picture. This includes the information from the scene itself, color decoder information, and synchronization information so the receiver knows where to put the picture. When a computer is involved, it has its own sync signals that are running independently of the sync signals sent by the camera. Genlocking is the act of getting the computer’s sync signals to line up with the camera’s sync signals. The sync signals from the camera and the computer must be locked together if the picture from the camera is to be shown correctly on the computer’s screen. This is performed by a genlock circuit. A genlock circuit may employ several techniques to do its job, with the most popular being a phase locked loop.
**Glossary of Terms**

**Half Bridge.** A circuit topology consisting of an upper transistor going to VDD, a lower device going to VSS, and a common node in between.

**Horizontal Scan Rate.** This is how fast the scanning beam in a display or a camera is swept from side to side. In the NTSC system this rate is 63.556 μs, or 15.734 kHz.

**Horizontal Sync.** This is the portion of the composite video signal that tells the receiver where to place the image in the left-to-right dimension. The horizontal sync pulse tells the receiving system where the beginning of the new scan line is.

**Hysteresis.** Positive feedback applied to increase noise immunity by varying the switch point depending on which state the device is in.

**Input Bias Current (Ib, IJ, Ib+, Ib–).** A figure of merit of an amplifier, buffer, or comparator which delineates the input currents of the amplifier under linear (normal) operating conditions. Input bias current is often the average of the two input currents and may be sensitive to the common mode input voltage.

**Input Impedance (RIN).** A figure of merit of an amplifier, buffer, or comparator which delineates the ratio change in input voltage to the change in input current. In general, voltage feedback amplifiers and comparators exhibit high input impedance at both the inverting and non-inverting inputs, but current feedback amplifiers exhibit low input impedance at the inverting input by design. Users should be aware that the "Input Impedance" is a DC figure of merit and that, in general, there is an input capacitance as well in parallel with the input impedance. The inverting input of a Current Feedback Amplifier can also appear to be inductive.

Differential Input Impedance applies to amplifiers with differential inputs and is measured by applying a small differential voltage to the inputs while measuring the change in bias current.

**Input Noise Voltage (en).** A figure of merit of an amplifier, or buffer that delineates the average noise voltage referred to the input under specific operating conditions. Usually, a curve of the noise characteristics is presented in the typical performance curves of the data sheet. A simple way of thinking of noise is to consider it "AC" offset voltage which dictates the overall system accuracy and the minimum signal which can be resolved. The noise source is often modeled as noise generator in series with one of the (differential) inputs of the amplifier.

**Input Noise Current (in).** A figure of merit of an amplifier or buffer that delineates the average noise current at the inputs. Since the noise current usually flows through resistors in a typical application, it is converted to a noise voltage referred to the input. It is usually modeled as a current source from each input to ground.

**Input Offset Current (Ios).** A figure of merit of an amplifier or comparator which delineates the difference in the currents into or out of the input terminals when the output is zero for an amplifier or to a specified output voltage for a comparator.

**Input Offset Voltage (Vos).** A figure of merit of an amplifier or comparator which is the voltage that must be applied to the inputs of an amplifier to make the output zero or the output of the comparator a specified voltage.

**Input Resistance.** See Input Impedance.

**Large Signal Voltage Gain (AVOL).** An open loop figure of merit for an amplifier or comparator which is the ratio of the output voltage to the change in input voltage required to move the output from zero volts to the specified voltage.
Latch-up. Results from parasitic action of the scr in CMOS circuits.

Locked. When one signal is synchronized to another by feedback, usually using a PLL.

Loop Gain. The difference between the open loop gain and closed loop (noise gain) of the circuit.

Luminance. As mentioned in the definition of chrominance, the NTSC and PAL video systems use a signal that has two pieces: the black-and-white part, and the color part. The black-and-white part is the luminance. It was the luminance component that allowed color TV broadcasts to be picked up by black-and-white TVs and still remain viewable.

Monochrome. A monochrome signal is a video source having only one component of color.

NTSC. An abbreviation for National Television Standards Committee.

Open Loop Transimpedance (ROLT). A figure of merit for a Current Feedback Amplifier which delineates the ratio of the change in output voltage to the change in current of the inverting input. ROL is similar to Large Signal Voltage Gain, AVOL, of a voltage feedback operational amplifier and is usually expressed in megohms.

Output Current (IOUT). A figure of merit of an amplifier or buffer which delineates the current that can be sunked or sourced by the device under linear operating conditions.

Output Impedance (ROUT). A figure of merit for an amplifier for a buffer or an amplifier which delineates that ratio of the change in output voltage to the change in output current usually for a specific load (RL) and source (RS) resistance. In general, output impedance for an amplifier is not particularly meaningful since the open loop output impedance is reduced by the loop gain of the amplifier. The output impedance for an (open loop) buffer, on the other hand is very meaningful in that, to the first order, it dictates the voltage gain of the device for a given load resistance (RL).

Output Resistance. See Output Impedance.

Output Voltage Swing (VOUT). A figure of merit of an amplifier which delineates the voltage that can be obtained from the device under linear conditions without clipping.

Offset Voltage Drift (dVOS/dT or TCVOS). A figure of merit of an amplifier, buffer, or comparator which delineates the average change in input offset voltage due to thermal effects over the specified operating temperature range of the device. It is often expressed in μV per degree Centigrade.

Overshoot (OS). A figure of merit of an amplifier or buffer which delineates the departure from the output from the final value usually on the rising or falling edge under small signal closed loop conditions.

PAL. PAL stands for Phase Alternate Line and PAL is to Europe as NTSC is to North America and Japan. In other words, PAL is the video standard used in Europe and a few other countries. There are a few differences. PAL uses 625 lines per frame while NTSC has 525 lines. Therefore, PAL has higher resolution. The frame rate of NTSC is 60 fps while for PAL it is 50 fps. This means the update rate for NTSC is higher and therefore there is more flicker with PAL. PAL uses the YUV color space while NTSC uses YIQ. PAL alternates the phase of every line color. The color-phase sequence of the chrominance signal is periodically reversed to cancel out hue errors. It is becoming increasingly important for imaging systems suppliers to produce equipment that can be sold worldwide without many manufacturing difficulties.

Peak White. Peak white is the highest point in the video waveform that the video level can reach and still stay within spec. If for some reason the level does become greater than peak white, it's referred to as whiter-than-white.
Pedestal. Pedestal is an offset used to separate the active video from the blanking level. When a video system uses a pedestal, the black level is above the blanking level by a small amount. When a video system doesn't use a pedestal, the black and blanking levels are the same.

Phase Margin. A figure of merit of an amplifier that delineates the difference between the phase of the output voltage and 180 degrees when the gain is one.

Pixel Clock. The pixel clock is used to divide the incoming horizontal video into pixels. This pixel clock has to be stable (a very small amount of jitter) relative to the incoming video or the picture will not be stored correctly. The higher the frequency of the pixel clock, the more pixels that will appear across the screen.

Power Supply Rejection Ratio (PSRR). A figure of merit of an amplifier, buffer, or comparator that delineates the ratio of the change in input offset voltage to the change in power supply voltage producing it.

Rails. Refers to the positive and negative supplies.

Response Time (tpd). A figure of merit of a comparator that delineates the time between the application of input step and the time that the output crosses a specified logic threshold.

Retrace. Retrace is what the electron beam does when it gets to the righthand edge of the display to get back to the lefthand edge. Retrace happens during the blanking time.

Rise Time (tr). See Transient Response Time.

S-VHS. S-VHS is an enhancement to regular VHS. S-VHS provides better resolution and less noise than VHS. S-VHS requires the luma and chroma components to be separate inputs to the VCR, while standard VHS only requires the composite NTSC signal. That's one of the reasons for the improved quality. S-VHS doesn't combine the luma and chroma so they don't have to be split apart. In the world of electronics, any time you combine two signals together, generally the two signals are degraded somewhat after you split them back out.

Saturation. Saturation is the amount of color present. For example, a lightly saturated red looks like pink, while a fully saturated red looks like the color of a red crayon. Saturation does not mean the brightness of the color, just how much "pigment" is used to make the color. The more "pigment," the more saturated the color is.

Scan Line. A scan line is an individual sweep across the face of the display by the electron beam that makes the picture.

Secam. This is another TV format similar to PAL. The difference between the two is that in Secam, the chrominance if FM modulated.

Serration Pulses. Serration pulses appear in the broad vertical sync pulse interval at a 2H line rate in order to maintain H-lock during vertical retrace.

Settling Time (ts). A figure of merit of an amplifier or buffer that relates the time between the initiation of an input step to the time that the output voltage has settled to a specified error band. If the output is ringing, the last reentry into the settling bound is defined as the end of the settling event. Settling time is usually a function of the input step size.
Shoot-Thru. Same as Cross Conduction.

Skew (clock). When two complementary signals have unbalanced delay.

Slew Rate (SR). A figure of merit of an amplifier or buffer which delineates the ability of the amplifier to accurately follow a large input step voltage. It is usually measured from the 20% to 80% point (and vice versa) of the output waveform.

Super Invertor. A circuit configuration which minimizes cross conduction.

Supply Current (Is, ICC, IEE, Is+, Is−). A figure of merit of an amplifier, buffer, or comparator that delineates the current required from the power supplies to operate the device with no load and the output at zero volts.

Sync. Sync is a fundamental piece of information for displaying any type of video. Essentially, the SYNC signal tells the display where to put the picture. The horizontal sync, or HSYNC for short, tells the display where to put the picture in the left-to-right dimension, while the vertical sync (VSYNC) tells the display where to put the picture from top to bottom.

Sync Generator. A sync generator is a circuit that provides sync signals. A sync generator may have a genlock input, or may not.

Sync Noise Gate. The sync noise gate is used right before the sync stripper to define an area within the video waveform where the sync stripper is to look for the HSYNC pulse. Anything outside of this defined window will be rejected by the sync noise gate and won’t be passed on to the sync stripper.

The main purpose of the sync noise gate is to make sure that the output of the sync stripper is nice, clean, and correct.

Sync Stripper. A composite video such as RS-170, NTSC or PAL contains the video information, which is the picture to be displayed, and information that tells the receiver where to put this video information on the display. The latter piece of information is called sync. A sync stripper pulls out the sync information from the composite video waveform and throws the rest away.

Transient Response Time (tr, tf). A figure of merit of an amplifier or buffer that delineates the closed loop response of the output of an amplifier in response to a small signal step input. Rise Time (tr) is usually specified from the 10% to the 90% point of the output and refers to the positive going edge; whereas Fall Time (tf) refers to the negative going edge of the output (or from 90% to 10%).

Unity Gain Bandwidth. A figure of merit of an amplifier that delineates the frequency where the amplifiers Large Signal Voltage Gain, AVOL, has rolled off to unity. For amplifiers that are unity gain stable, the unity gain bandwidth and Gain Bandwidth product are identical, but decompensated amplifiers often specify Gain Bandwidth Product at frequencies that are below the point where the amplifier’s AVOL is one.

Vertical Sync. This is the portion of the composite video signal that tells the receiver where the top of the picture is.

Video Mixing. Video mixing is taking two independent video sources and editing them together to create a new, third video source. This can be done by fading from a one source to the other.
**Video Waveform.** The video waveform is what the signal "looks" like to the receiver or TV. The video waveform is made up of several parts that are all required to make up a TV picture that can be accurately displayed. Each component is necessary.

**White Level.** This level represents the lightest an image can get, and defines what white is for the particular image system. By calibration, this is the highest video level allowed in the system. If for some reason the video goes above this level, it is referred to as "whiter-than-white."

**Y/C.** The Y/C designation is shorthand for luminance and chrominance. You will also see this term used in the description of the S-VHS video tape format. The S-VHS format records the luma and chroma separately while standard VHS records them together.

**Y/C Split.** A Y/C splitter circuit is what's used in a TV set or imaging device to pull the luminance and chrominance apart in an NTSC or PAL system. This is the first thing that any NTSC or PAL receiver must do. The composite video signal is first fed to the Y/C splitter so that the luma and chroma can then be decoded further. The two popular methods for implementing a Y/C split are a chroma bandpass/chroma trap combo or a comb filter arrangement.

**YIQ.** YIQ is the color space used in the NTSC color system. The Y component is the black-and-white, (luma) portion of the image. The I and Q parts are the color components placed over the black-and-white, or luma, component.

**YUV.** YUV is the color space used by the PAL color system. As with the YIQ colorspace, the Y is the luma component while the U and V are the color components.
Package Outlines

Élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
Soldering Packages to PC Boards

DIP Packages
Wave soldering is recommended for DIP packages. Solder plated boards are recommended. Rosin mildly activated (RMA) flux is needed. Wave soldering using a dual wave system at 250°C ± 10°C for two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Hand soldering, Elantec’s DIP packages will survive a peak temperature of 300°C (at leads) for a maximum period of 10 seconds.

Surface Mount Packages
Wave soldering and vapor phase or infrared (IR) reflow can be used for soldering surface mount packages to PC boards. Solder plated boards are recommended for wave soldering and vapor phase or IR reflow methods.

Wave Soldering: Adhesive is used to hold components on the boards during wave soldering. Place components on the board and cure adhesive before wave soldering. Rosin mildly activated (RMA) flux or organic flux is needed. Wave soldering using a dual wave system at 250°C ± 10°C for a maximum of two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Reflow Soldering: Screen solder paste on board and attach components to board. Solder paste with RMA flux is recommended. Bake boards at 65°C–90°C for 15 minutes. Preheat boards to within 60°C–70°C of the solder temperature. To reflow solder paste with vapor phase method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 215°C. For the IR reflow method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 220°C. The temperature/time ramp-up during vapor phase or IR reflow shall be no greater than 2°C/sec.

Hand soldering, Elantec’s surface mount packages will survive a peak temperature of 260°C (at leads) for a maximum period of 10 seconds.
### Package Outlines

**MDP0016 Rev. B**  
CerDIP Package  
Lead Finish (Coml)—Tin Plate or Hot Solder DIP  
Lead Finish (Mil)—Hot Solder DIP

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Note 1: These dimensions do not include mold flash or protrusions. Mold flash protrusion shall not exceed .006" on any side.
Note 2: SO-8, SO-14, SO-16 packages are narrow body (0.150").
Note 3: Dimensions and tolerancing per ANSI Y14.5M-1982.
Note 4: Flat area of lead foot.
Note 5: SOL-24T2 (thermal package) has 2 fused leads on each side of package.
Note 6: SOL-20T (thermal package) has 4 fused leads on each side of package.
Note 7: SOL-28T contains a thermal metal slug.

**MDP0027 Rev. C**
Package Outline—SOIC
Lead Finish—Solder Plate

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**Package Outlines**
MDP0028 Rev. A
5-Lead TO-220
Lead Finish—Solder Plate
**MDP0031 Rev. A**  
Plastic Package  
Lead Finish—Hot Solder DIP

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Note: Package outline exclusive of any mold flashes. Mold flash protrusion shall not exceed 0.006" on any side.
Ordering Information
In North America, Elantec has three levels of sales support. Regional Sales Managers are located in the Boston and San Jose areas. Field Applications Engineers are located in the Boston and San Jose offices. Elantec also maintains a network of sales representatives covering the United States and Canada. Finally, major nationwide and regional distributors provide local stock. Elantec maintains an up-to-date distributor inventory status and provides an inventory referral service through Distribution Sales in San Jose. Orders may be placed through the sales representatives or distributors. A list of sales representatives and distributors is included in this databook, or please contact any of the regional sales offices.

The application specific products listed below are not generally available through U.S. Distribution channels. For information regarding price and availability, please contact your local Elantec representative or regional sales office.

- EL6251C Laser Diode Driver
- EL7556C Adjustable CPU Power Supply Unit
- EL7560C Programmable CPU Power Supply Unit
- EL7561C Programmable CPU Power Supply Unit
- EL7571C Programmable DC:DC Controller

In Europe, Elantec has a Regional Sales Office in London. Local sales support is provided through stocking representatives in all of the major countries. A current list of representatives and distributors may be obtained from the London office.

Elantec has stocking agents in all Pacific Rim Countries, Australia, and New Zealand. A list may be obtained from Elantec's headquarters in Milpitas, California.

In Asia, local sales support is provided through stocking representatives in all of the major countries. A current list of representatives is included in this databook or contact the factory.

Elantec Product Alpha/Numeric Description

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SOT Marking Specifications

eYW? e-Elantec
Y-Year code: last digit of year
W-Bi-weekly code: alpha only,
example: A = ww1-2

?-Part Code: A = EL2150CW
B = EL2170CW
C = EL2180CW
Applications Assistance / Sample Ordering Information
Elantec's Policy
Elantec receives many applications inquiries every day which vary widely in nature. We believe that Application assistance is as inherently important to our customers as the performance and quality of our products. To assist our customers in getting the best and fastest support possible, the following information is provided.

Sample and Literature Requests
If you know what product sample or literature you need, probably the best and fastest way to obtain them is to call Elantec's local sales office, sales representative, or distributor. A complete listing is on pages 11-3 through 11-15 of this book. If you are not sure what you need, call our Applications hot line 1 (800) 333-6314. For literature only, touch or request extension 234. For applications assistance, touch or request extension 311.

New Applications Assistance
Technical assistance for a new application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit needs to do. What we mean by that is the cost and performance objectives of the circuit or system. If you have a preliminary topology or schematic, feel free to FAX that to the Factory at 1 (408) 945-9305 in confidence. The following is a check list which will expedite our assistance to you:

- What does the circuit need to do?
- What power supply voltages are available?
- What is the temperature range?
- What is the load?
- What are the key specs: bandwidth, slew rate, settling time, noise, output voltage, etc. and what are your expectations?

Problems with an Existing Circuit and Other Issues
Applications assistance for an existing application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit is doing or not doing. The following is a check list which will expedite our assistance to you:

- What is the part number?
- What is the device's date code?
- What are the symptoms?
- Are scope photos or frequency plots available?
- How many devices are involved?

Unreleased Product
As a general rule, Elantec does not sample new devices that have not completed our rigorous formal release cycle. However, occasionally we will "beta" site customers with advanced Engineering samples. We view this as a productive exchange between our Factory and customer Engineering teams to pinpoint problems and issues. In all instances, these devices will be marked "Engineering Sample." If you are interested in such a device, call your nearest Elantec sales office, local sales representative, or the Factory at 1 (800) 333-6314 and touch or request extension 252.

Demo Boards
Contact factory applications for demo board availability.

Quality or Reliability Issues
On the rare occasion that you experience what may be a Reliability or Quality issue, please contact the nearest Elantec sales office, local sales representative, or distributor. You may choose to call the Factory directly at 1 (800) 333-6314, and touch or request extension 310 or 279.

Price Quotes/Delivery Status
For pricing and delivery information, please contact the appropriate full service representative or local Elantec franchised distributor as listed on page 11-6. For additional information you may contact the Elantec Customer Service Department @ 1 (800) 333-6314.
Terms and Conditions of Sale
ELANTEC, INCORPORATED ("SELLER")

TERMS AND CONDITIONS OF SALE

1. ACCEPTANCE OF ORDER
THIS ACKNOWLEDGEMENT AND ACCEPTANCE IS EXPRESSLY LIMITED TO AND MADE CONDITIONAL UPON THE TERMS AND CONDITIONS CONTAINED HEREIN AND ANY OF THE BUYER'S TERMS AND CONDITIONS WHICH ARE IN ADDITION TO OR DIFFERENT FROM THOSE CONTAIN HEREIN WHICH ARE NOT SEPARATELY AND SPECIFICALLY AGREED TO IN WRITING ARE HEREBY OBJECTED TO AND SHALL BE OF NO EFFECT.

Only those orders accepted by Seller as its home office in Milpitas, California shall be binding upon Seller.

2. PRICES
Irrespective of any prices quoted by Seller or listed on Buyer's order, Seller's acceptance of any order is subject to the prices shown on Seller's acknowledgment. Said prices are firm and are not subject to adjustment other than "precious metals adjustments" or "precious metals surcharges" at Seller's option to cover Seller's cost of fluctuations in the price of precious metals utilized in the manufacture of Seller's products.

3. TAXES
All prices are exclusive of all federal, state and local excise, sales, use and similar taxes. Such taxes shall be paid by Buyer, or in lieu thereof Buyer shall provide Seller with a tax exemption certificate acceptable to the taxing authorities. When applicable, such taxes will appear as separate additional items on the invoice unless Seller receives a proper tax-exemption certificate from Buyer prior to shipment.

4. PAYMENT
Unless Seller has extended credit to Buyer as described below, Buyer shall pay Seller, at Seller's option either by: Cash with Order, C.O.D., Letter of Credit or Sight Draft.

Should Seller elect to extend credit to Buyer, payment shall be made in full within thirty (30) days of the date of Seller's invoice. Seller reserves the right at any time to change the amount of or to withdraw any credit extended to Buyer.

Any payments made in excess of thirty (30) days may be subject to late charges.

5. TITLE AND DELIVERY
Seller shall deliver products sold hereunder to Buyer F.O.B. Seller's factory. Partial deliveries shall be permitted. Upon such delivery to a carrier at Seller's factory, title to the products and all risk of loss or damage shall pass to Buyer.

6. SHIPMENT
All shipping charges and expenses shall be paid by Buyer. Seller will not insure the products sold hereunder unless requested by Buyer in which case Buyer will pay for such insurance.

Shipments will be made, at Seller's option, either by Parcel Post, Railway Express, Air Express, Air Freight, or as otherwise determined by Seller.

Shipping dates are approximate and are dependent upon Seller's prompt receipt of all necessary information from Buyer.

7. PATENTS
With respect to products manufactured solely to Seller's designs and specifications, Seller shall defend any suit or proceeding brought against Buyer insofar as such suit or proceeding is based on a claim that any such products furnished hereunder infringe any patent of the United States. If Seller is notified promptly in writing of such suit or proceeding and given full and complete authority, information, and assistance by Buyer for such defense, Seller shall pay all damages and costs finally awarded against Buyer in any such suit or proceeding, but Seller shall not be responsible for any compromise thereof made by Buyer without the written consent of Seller. In the event that such products are held in such suit or proceeding to infringe a patent of the United States and their use is enjoined, or if in the opin-
ion of Seller such products are likely to become the subject of a claim of infringement of a patent of the United States, Seller, in its sole discretion and at its own expense, may either: (a) procedure for Buyer the right to continue using such products with noninfringing products; or (b) modify such products so that they become noninfringing; or (c) replace such products with noninfringing products; or (d) accept the return of such products, granting Buyer a refund therefor equal to the depreciated value thereof.

Seller shall have no liability to Buyer under any provision hereof if any patent infringement or claim thereof is based upon (a) a modification of the products not introduced by or approved by Seller; or (b) the interconnection or use of the products in combination with products with other devices not made by Seller; or (c) the use of the products in other than an application recommended by Seller.

The foregoing states the entire liability of Seller for infringement of patents by Seller's products or any part(s) thereof.

8. INDEMNITY
Buyer shall indemnify, defend, and hold Seller harmless from and against any and all liability, damages, expenses, costs or losses resulting from any suit or proceeding brought for infringement of a patent(s), copyright(s), or trademark(s), or for a misappropriation of use of any trade secret(s), or for unfair competition arising from Seller's compliance with Buyer's design, specifications or instructions.

9. SECURITY INTEREST
Notwithstanding passage of title of products sold hereunder to Buyer F.O.B. Seller's factory, Seller shall retain a security interest in the products until payment has been made in full by Buyer for such products. Buyer shall perform all acts necessary to perfect and maintain such security interest.

10. WARRANTIES
Seller warrants to Buyer that Seller's standard products sold hereunder (and any services furnished therewith) which are not used in any medical or life support application shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of one year from the date of shipment. For products which are not standard products of Seller, such as dice and developmental or custom designed products. Seller warrants to Buyer that such products sold hereunder (and any services furnished therewith) shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of thirty (30) days from the date of shipment.

Should products sold hereunder fail to meet the above applicable warranty, Seller, at its option, shall repair or replace such products or issue Buyer a credit provided that (a) Seller is notified in writing by Buyer within thirty (30) days after discovery of such failure; (b) Buyer obtains a Return Material Authorization from Seller prior to returning any defective products to Seller; (c) the defective products are returned to Seller, transportation charges prepaid by Buyer; (d) the defective products are received by Seller for adjustment no later than four (4) weeks following the last day of the warranty period, and (e) Seller's examination of such products shall disclose, to its satisfaction, that such failures have not been caused by misuse, abuse, neglect, improper installation or application repair, alteration, accident or negligence in use, storage, transportation or handling.

In the event of failure to meet the above applicable warranty with respect to products sold hereunder cannot be corrected by Seller's reasonable efforts, the Seller and Buyer shall negotiate an equitable adjustment in price.

The foregoing warranty provisions set forth the Seller's sole liability and the Buyer's exclusive remedies for claims (except as to title) based on defects in or failure of any products sold hereunder or services furnished hereunder whether the claim is based in contract, tort, (including negligence), warranty or otherwise and however instituted. Upon the expiration of the applicable warranty for any products sold hereunder, all such liability shall terminate.
The above warranty periods shall not be extended by the repair or replacement of products pursuant to any of the above warranties. The above warranties shall apply only to Buyer and shall not apply to Buyer’s customers or any other third parties.

SELLER PRODUCTS ARE NOT DESIGNED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS WITHOUT THE SPECIFIC WRITTEN CONSENT OF THE PRESIDENT OF ELANTEC. LIFE SUPPORT SYSTEMS ARE EQUIPMENT INTENDED TO SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS PROVIDED CAN BE REASONABLY EXPECTED TO RESULT IN SIGNIFICANT PERSONAL INJURY OR DEATH. USERS CONTEMPLATING APPLICATION OF SELLER PRODUCTS IN LIFE SUPPORT SYSTEMS ARE REQUESTED TO CONTACT SELLER FACTORY HEADQUARTERS TO ESTABLISH SUITABLE TERMS AND CONDITIONS FOR THESE APPLICATIONS. SELLER’S WARRANTY IS LIMITED TO REPLACEMENT OF DEFECTIVE COMPONENTS AND DOES NOT COVER INJURY TO PERSONS OR PROPERTY OR OTHER CONSEQUENTIAL DAMAGES.

11. LIMITATION OF LIABILITY

In no event, whether as a result of breach of contract, warranty or tort (including negligence) or otherwise shall Seller be liable for any special, consequential, incidental or penal damages, including but not limited to, loss of profit or revenues, loss of the product or any associated equipment, damaged to associated equipment, cost of capital, cost of substitute products, facilities, service or replacement power, down time costs or claims of Buyer's customers for such damages. If Buyer transfers title to or leases products sold hereunder to any third party, Buyer shall obtain from such third party a provision affording the Seller the protection of the preceding sentence.

Except as provided in the above “Patents” article, whether a claim is based in contract, tort (including negligence) or otherwise, the Seller's liability for any loss or damage arising out of, or resulting from any products sold hereunder or services furnished hereunder shall in no case exceed the price of the specific product(s) or service(s) which gives rise to the claim. Except as to title, any such liability shall terminate upon the expiration of the applicable warranty period specified in the above “Warranties” article.

12. U.S. GOVERNMENT CONTRACTS

If the products to be furnished hereunder are to be used in the performance of a U.S. Government contract or subcontract, no Government requirements or regulations shall be binding upon Seller unless specifically agreed to by Seller in writing.

If the Government terminates such a contract or subcontract in whole or in part through no fault of or failure to perform by Buyer, this order may be canceled in writing in the same proportion, and the liability of Buyer for termination allowances shall be determined by the then applicable regulations of the Government regarding termination of contracts.

13. EXCUSABLE DELAYS

Seller shall not be liable for delays in delivery or performance due to any cause beyond its reasonable control, including, without limitation, acts of God, acts of Buyer, strikes or other labor disturbances, inability to obtain necessary materials, components, services or facilities.

14. CANCELLATIONS OF STANDARD PRODUCTS

Should Buyer terminate any order accepted hereunder or should Seller terminate any order accepted hereunder due to Buyer's nonperformance of its obligations hereunder, then Buyer shall pay Seller its reasonable termination charges within fifteen (15) days from the date of invoice of same.

Buyer may request rescheduling or cancellation by providing thirty (30) days written notice to Elantec provided however, that Elantec is not obligated to accept such notice, but if such notice is given and accepted by Elantec, then Elantec has the right to deliver and be paid by Buyer for:

1. 100% of quantity of devices scheduled for delivery within thirty (30) days following receipt of said notice.
2. 50% of quantity of devices scheduled for delivery within 30–60 days following receipt of said notice.

15. CANCELLATION OF PRODUCTS MANUFACTURED TO BUYER’S DESIGN/SPECIFICATIONS INCLUDING ALL NON-STANDARD AND DISK DRIVE PRODUCTS
Charge for engineering, design, generation of data, lot charges or any other special charges that are not for product are non-cancelable except with prior written permission from Seller.

Buyer may request rescheduling or cancellation of product by providing 60 day notice to Elantec provided, however, that Elantec is not obligated to accept such notice but if such notice is given and is accepted by Elantec, then Elantec has the right to deliver and be paid by the Buyer for:
1. 100% quantity within 60 days following written receipt of said notice;
2. All additional work in progress scheduled within the 16 week delivery time period shall be paid for by Buyer at a price based on the percentage of completion of such inventory applied to the price for the finished product. Buyer shall also promptly pay to Elantec; (a) costs of settling and paying claims arising out of termination of work under Elantec’s subcontracts or vendors; (b) reasonable costs of settlement, including engineering, development, accounting, legal and clerical costs; (c) twenty percent (20%) of the purchase price of the purchase order to be canceled.

16. ASSIGNMENT
Any assignment by Buyer of this order or of any rights or obligations in connection therewith shall be void without the written prior consent of the Seller.

17. EXPORT TO NON-APPROVED COUNTRIES
Buyer agrees to take all reasonable and necessary precautions to prevent ultimate exportation of Elantec products to countries prohibited by rules or regulations of the United States Government, and to obtain all export licenses and other governmental approvals necessary prior to the export of any Elantec products.

18. MISCELLANEOUS
The validity, performance and construction of these terms and conditions of sale and any sale hereunder shall be governed by the laws of the state of California.

The invalidity, in whole or in part, of a provision herein shall not affect the validity or enforce ability of any other provision herein.

Any representation, warranty, course of dealing or trade usage not contained or referenced herein shall not be binding on Seller.

No modification, amendment, recision, waiver or other change in these terms and conditions shall be binding on Seller unless assented to in writing by Seller’s duly authorized representative.

Seller reserves the right to manufacture and/or assemble its products in any of its worldwide facilities unless otherwise agreed to in writing with Buyer.
Sales Representatives and Distributors
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<th>District</th>
<th>Company Name</th>
<th>Address</th>
<th>City, State, Zip</th>
<th>Phone</th>
<th>Fax</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IDAHO, NORTH</strong></td>
<td></td>
<td>Electronics Solutions</td>
<td>P.O. Box 91428</td>
<td>Portland, OR 97291</td>
<td>PHONE 503-292-8204</td>
<td>FAX 503-423-8005</td>
</tr>
<tr>
<td><strong>IDAHO, SOUTH</strong></td>
<td></td>
<td>First Source</td>
<td>10451 W. Garverdale Ct #209</td>
<td>Boise, ID 83704</td>
<td>PHONE 208-378-4680</td>
<td>FAX 208-323-9386</td>
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<tr>
<td><strong>ILLINOIS, NORTH</strong></td>
<td></td>
<td>High Technology Sales</td>
<td>Zurich Towers 1450 E. American Ln., Ste. 1400</td>
<td>Schaumburg, IL 60173</td>
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<tr>
<td><strong>ILLINOIS, SOUTH</strong></td>
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<td>Midtec Associates, Inc</td>
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<td>FAX 314-275-8859</td>
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<tr>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>IOWA</strong></td>
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</tr>
<tr>
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</tr>
<tr>
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<tr>
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</tr>
<tr>
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</tr>
<tr>
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<thead>
<tr>
<th>Location</th>
<th>Company Name</th>
<th>Address</th>
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<td>Nu Horizons</td>
<td>107 Audubon Rd Bldg 1</td>
<td>617-246-4442</td>
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<tr>
<td>MARYLAND</td>
<td>Nu Horizons</td>
<td>8975 Guilford Rd #120</td>
<td>617-995-6330</td>
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<td>25 Upton Dr</td>
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<td>508-694-2199</td>
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<td>Insight Electronics</td>
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<td>617-270-9400</td>
<td>617-270-3279</td>
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