

CAT28C17A

16K-Bit CMOS PARALLEL EEPROM



FEATURES

- Fast Read Access Times: 200 ns■ Low Power CMOS Dissipation:
 - -Active: 25 mA Max. -Standby: 100 μA Max.
- **■** Simple Write Operation:
 - -On-Chip Address and Data Latches
 -Self-Timed Write Cycle with Auto-Clear
- Fast Write Cycle Time: 10ms Max

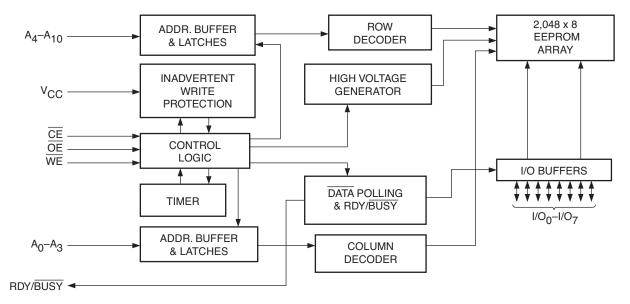
- End of Write Detection:
 - -DATA Polling
 - -RDY/BSY Pin
- Hardware Write Protection
- CMOS and TTL Compatible I/O
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Commercial,Industrial and Automotive Temperature Ranges

DESCRIPTION

The CAT28C17A is a fast, low power, 5V-only CMOS parallel EEPROM organized as 2K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. \overline{DATA} Polling and a RDY/ \overline{BSY} pin signal the start and end of the self-timed write cycle. Additionally, the CAT28C17A features hardware write protection.

The CAT28C17A is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 28-pin DIP and SOIC or 32-pin PLCC packages.

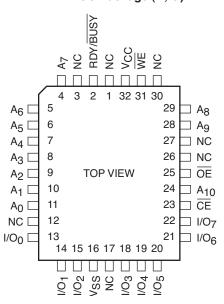
BLOCK DIAGRAM



PIN CONFIGURATION

DIP Package (P, L) SOIC Package (J,W) (K, X) RDY/BUSY □ 28 RDY/BUSY [□ Vcc 28 □ Vcc NC □ □ WE NC 🗀 2 27 27 □ WE 🗅 ис A₇ □ 3 26 □ NC 3 26 A₆ □ 25 _ A8 4 25 □ A₈ A₆ Ľ 4 5 □ A₉ 5 24 □ A₉ A₅ □ 24 A₄ □ 6 23 □ ис 6 23 р ис A₃ □ 7 占쥲 22 7 22 □ A₁₀ 8 21 21 A2 [8 ☐ A₁₀ 20 ₽ Œ 9 20 □ CE 9 A₁ \square A₀ □ 10 19 □ 1/O₇ 10 19 □ 1/07 1/00 □ I/O₀ 🗀 11 18 □ I/O₆ 11 18 □ 1/O₆ I/O₁ 🗀 I/O₁ \Box 17 17 ☐ I/O₅ 12 □ I/O₅ 12 1/02 □ □ 1/04 13 16 □ I/O₄ I/O₂ 🗀 13 16

PLCC Package (N, G)



PIN FUNCTIONS

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V_{SS} □

Pin Name	Function
A ₀ -A ₁₀	Address Inputs
I/O ₀ –I/O ₇	Data Inputs/Outputs
RDY/BUSY	Ready/BUSY Status
CE	Chip Enable
ŌĒ	Output Enable
WE	Write Enable
V _{CC}	5V Supply
V _{SS}	Ground
NC	No Connect

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□ I/O₃

MODE SELECTION

Mode	CE	WE	ŌĒ	I/O	Power
Read	L	Н	L	Douт	ACTIVE
Byte Write (WE Controlled)	L		Н	DIN	ACTIVE
Byte Write (CE Controlled)		L	Н	DIN	ACTIVE
Standby, and Write Inhibit	Н	X	Х	High-Z	STANDBY
Read and Write Inhibit	Х	Н	Н	High-Z	ACTIVE

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Vss □

14

□ 1/O₃

CAPACITANCE $T_A = 25^{\circ}C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
C _{I/O} ⁽¹⁾ Input/Output Capacitance		10	pF	$V_{I/O} = 0V$
C _{IN} ⁽¹⁾ Input Capacitance		6	pF	$V_{IN} = 0V$

Note:

⁽¹⁾ This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias –55°C to +125°C
Storage Temperature –65°C to +150°C
Voltage on Any Pin with Respect to Ground ⁽²⁾ $-2.0V$ to $+V_{CC} + 2.0V$
V _{CC} with Respect to Ground –2.0V to +7.0V Package Power Dissipation Capability (Ta = 25°C)
, , , , , , , , , , , , , , , , , , , ,
Lead Soldering Temperature (10 secs) 300°C
Output Short Circuit Current ⁽³⁾ 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N _{END} ⁽¹⁾	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽¹⁾	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽¹⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽¹⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

 $V_{CC} = 5V \pm 10\%$, unless otherwise specified.

			Limits			
Symbol	Parameter	Min.	Min. Typ. Max.		Units	Test Conditions
Icc	V _{CC} Current (Operating, TTL)			35	mA	$\overline{CE} = \overline{OE} = V_{IL},$ f = 1/t _{RC} min, All I/O's Open
I _{CCC} ⁽⁵⁾	V _{CC} Current (Operating, CMOS)			25	mA	$\overline{CE} = \overline{OE} = V_{ILC},$ f = 1/t _{RC} min, All I/O's Open
I _{SB}	V _{CC} Current (Standby, TTL)			1	mA	CE = V _{IH} , All I/O's Open
I _{SBC} ⁽⁶⁾	V _{CC} Current (Standby, CMOS)			100	μА	CE = V _{IHC} , All I/O's Open
ILI	Input Leakage Current	-10		10	μΑ	V_{IN} = GND to V_{CC}
I _{LO}	Output Leakage Current	-10		10	μА	$V_{OUT} = GND \text{ to } V_{CC},$ $\overline{CE} = V_{IH}$
V _{IH} ⁽⁶⁾	High Level Input Voltage	2		V _{CC} +0.3	V	
V _{IL} (5)	Low Level Input Voltage	-0.3		0.8	V	
V _{OH}	High Level Output Voltage	2.4			V	I _{OH} = -400μA
V _{OL}	Low Level Output Voltage			0.4	V	I _{OL} = 2.1mA
V _{WI}	Write Inhibit Voltage	3.0			V	

Note

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.

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- (3) Output shorted for no more than one second. No more than one output shorted at a time.
- (4) Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V_{CC} +1V.
- (5) $V_{ILC} = -0.3V$ to +0.3V.
- (6) $V_{IHC} = V_{CC} 0.3V$ to $V_{CC} + 0.3V$.

A.C. CHARACTERISTICS, Read Cycle

 $V_{CC} = 5V \pm 10\%$, unless otherwise specified.

		28C17A-20		
Symbol	Parameter Min. Max.		Units	
t _{RC}	Read Cycle Time	200		ns
t _{CE}	CE Access Time		200	ns
t _{AA}	Address Access Time		200	ns
t _{OE}	OE Access Time		80	ns
t _{LZ} (1)	CE Low to Active Output	0		ns
t _{OLZ} (1)	OE Low to Active Output	0		ns
t _{HZ} (1)(2)	CE High to High-Z Output		55	ns
t _{OHZ} (1)(2)	OE High to High-Z Output		55	ns
t _{OH} ⁽¹⁾	Output Hold from Address Change 0		ns	

Figure 1. A.C. Testing Input/Output Waveform(3)

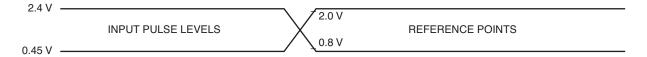
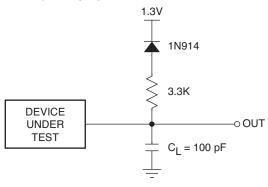


Figure 2. A.C. Testing Load Circuit (example)



CI INCLUDES JIG CAPACITANCE

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
- (3) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

 V_{CC} = 5V $\pm 10\%,$ unless otherwise specified.

	28C		7A-20	
Symbol	Parameter	Min.	Max.	Units
t _{WC}	Write Cycle Time		10	ms
t _{AS}	Address Setup Time	10		ns
t _{AH}	Address Hold Time	100		ns
t _{CS}	CE Setup Time	0		ns
t _{CH}	CE Hold Time 0			
t _{CW} ⁽²⁾	CE Pulse Time 150		ns	
toes	OE Setup Time 15		ns	
toeh	OE Hold Time 15		ns	
t _{WP} ⁽²⁾	WE Pulse Width 150		ns	
t _{DS}	Data Setup Time	50		ns
t _{DH}	Data Hold Time	10		ns
t _{DL}	Data Latch Time	50 ns		ns
t _{INIT} (1)	Write Inhibit Period After Power-up	5 20 ms		ms
t _{DB}	Time to Device Busy	80		ns

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
 (2) A write pulse of less than 20ns duration will not initiate a write cycle.

DEVICE OPERATION

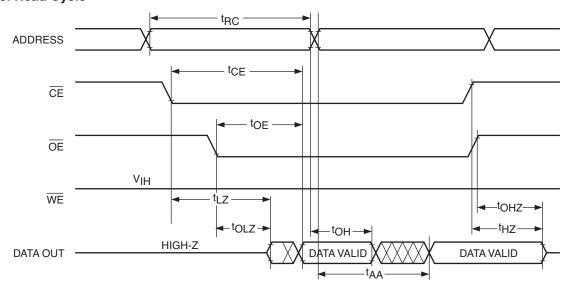
Read

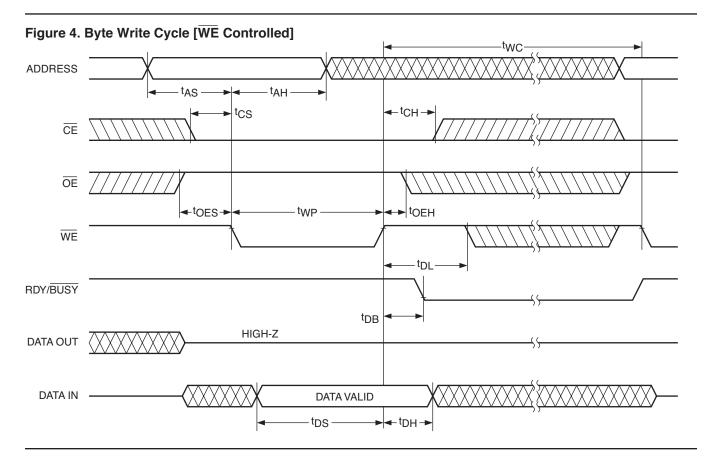
Data stored in the CAT28C17A is transferred to the data bus when \overline{WE} is held high, and both \overline{OE} and \overline{CE} are held low. The data bus is set to a high impedance state when either \overline{CE} or \overline{OE} goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Ready/BUSY (RDY/BUSY)

The RDY/BUSY pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/BUSY line.

Figure 3. Read Cycle





Byte Write

A write cycle is executed when both \overline{CE} and \overline{WE} are low, and \overline{OE} is high. Write cycles can be initiated using either \overline{WE} or \overline{CE} , with the address input being latched on the falling edge of \overline{WE} or \overline{CE} , whichever occurs last. Data, conversely, is latched on the rising edge of \overline{WE} or \overline{CE} , whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

DATA Polling

DATA polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O₇ (I/O₀–I/O₆ are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

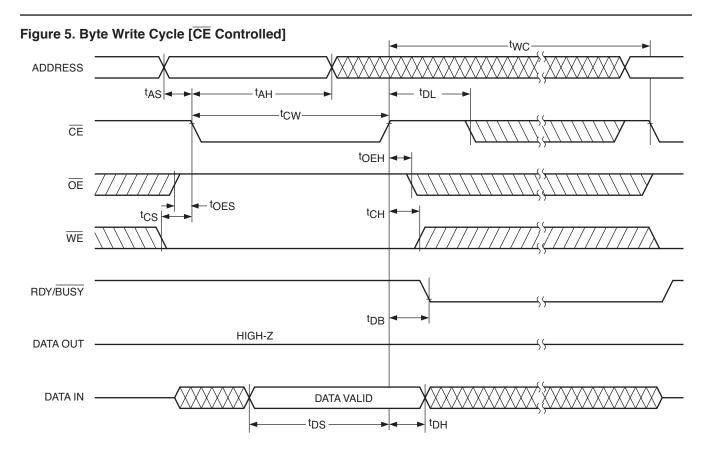
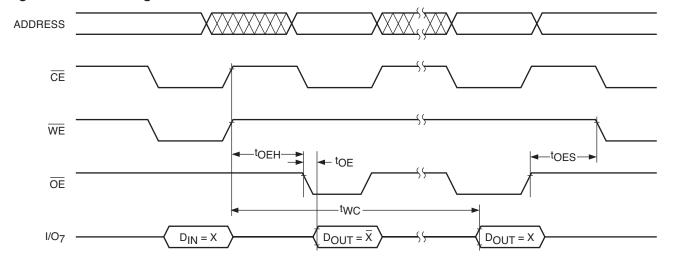


Figure 6. DATA Polling

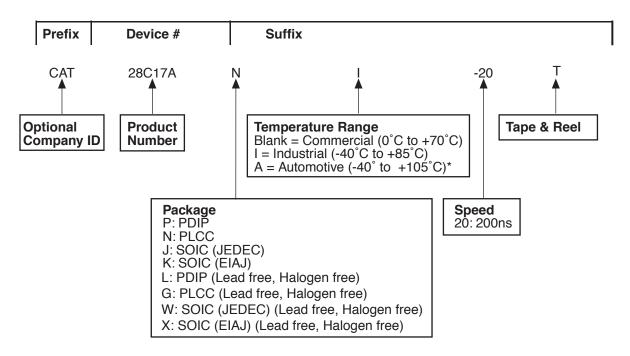


HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C17A.

- (1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.
- (2) A power on delay mechanism, t_{INIT} (see AC charac-
- teristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.
- (3) Write inhibit is activated by holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high.
- (4) Noise pulses of less than 20 ns on the WE or CE inputs will not result in a write cycle.

ORDERING INFORMATION



* -40°C to +125°C is available upon request

Notes:

(1) The device used in the above example is a CAT28C17ANI-20T (PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).

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REVISION HISTORY

Date	Revision	Comments	
3/29/2004	Α	Added Green packages in all areas	
04/19/04	В	B Delete data sheet designation	
		Update Block Diagram	
		Update Ordering Information	
		Update Revision History	
		Update Rev Number	

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