TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

256-MBIT (32M x 8 BITS/16M x 16BITS) CMOS NAND E²PROM

DESCRIPTION

The TC58DxM82x1xxxx is a 256-Mbit (276,824,064) bit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) organized as 528 bytes/264 words x 32 pages x 1048 blocks. The device uses dual power supplies (2.7 V to 3.6 V for VCC and 1.65 V to 1.95 V for VCCQ). The device has a 528-byte/264-words static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte/256-words increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes x 32 pages/8K words + 256 words: 264 words x 32 pages).

The TC58DxM82x1xxxx is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- **Organization**
  - Memory cell array: 528 x 64K x 8
  - Register: 528 x 8
  - Page size: 528 bytes
  - Block size: (16K + 512) bytes

- **Modes**
  - Read, Reset, Auto Page Program
  - Auto Block Erase, Status Read

- **Mode control**
  - Serial input/output
  - Command control

- **Power supply**
  - VCC: 2.7V to 3.6V
  - VCCQ: 1.65V to 1.95V

- **Program/Erase Cycles**
  - 1E5 cycle (with ECC)

- **Access time**
  - Cell array to register: 25 µs max
  - Serial Read Cycle: 50 ns min

- **Operating current**
  - Read (50 ns cycle): 10 mA typ.
  - Program (avg.): 10 mA typ.
  - Erase (avg.): 10 mA typ.
  - Standby: 50 µA max.

- **Package**
  - TSOP I 48-P-1220-0.50 (Weight: 0.53g typ)

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PIN ASSIGNMENT (TOP VIEW)

TC58DVM82A1FT00 / TC58DAM82A1FT00

TC58DVM82F1FT00 / TC58DAM82F1FT00

PINNAMES

<table>
<thead>
<tr>
<th>I/O1 to I/O8</th>
<th>I/O port</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O9 to I/O16</td>
<td>I/O port (x16)</td>
</tr>
<tr>
<td>CE</td>
<td>Chip enable</td>
</tr>
<tr>
<td>WE</td>
<td>Write enable</td>
</tr>
<tr>
<td>RE</td>
<td>Read enable</td>
</tr>
<tr>
<td>CLE</td>
<td>Command latch enable</td>
</tr>
<tr>
<td>ALE</td>
<td>Address latch enable</td>
</tr>
<tr>
<td>WP</td>
<td>Write protect</td>
</tr>
<tr>
<td>RY/BUY</td>
<td>Ready/Busy</td>
</tr>
<tr>
<td>GND</td>
<td>Ground input</td>
</tr>
<tr>
<td>VCC</td>
<td>Power supply</td>
</tr>
<tr>
<td>VCCQ</td>
<td>I/O port Power supply</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
</tr>
</tbody>
</table>
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>RATING</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Power Supply Voltage</td>
<td>-0.6~4.6</td>
<td>V</td>
</tr>
<tr>
<td>VCCQ</td>
<td>I/O port Power Supply Voltage</td>
<td>-0.6~4.6</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Input Voltage for Control pins</td>
<td>-0.6~4.6</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>Input/Output Voltage for I/O pins</td>
<td>-0.6 V~VCCQ + 0.3 V (≤ 4.6 V)</td>
<td>V</td>
</tr>
<tr>
<td>PD</td>
<td>Power Dissipation</td>
<td>0.3</td>
<td>W</td>
</tr>
<tr>
<td>Tsolder</td>
<td>Soldering Temperature (10s)</td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature</td>
<td>-55~150</td>
<td>°C</td>
</tr>
<tr>
<td>Topr</td>
<td>Operating Temperature</td>
<td>0~70</td>
<td>°C</td>
</tr>
</tbody>
</table>

**CAPACITANCE *(Ta =25°C, f = 1 MHz)*

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input</td>
<td>VIN = 0 V</td>
<td>—</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output</td>
<td>VOUT = 0 V</td>
<td>—</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

* This parameter is periodically sampled and is not tested for every device.
## VALID BLOCKS (1)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>NVB</td>
<td>Number of Valid Blocks</td>
<td>2008</td>
<td></td>
<td>2048</td>
<td>Blocks</td>
</tr>
</tbody>
</table>

1. The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
2. The first block (block address #00) is guaranteed to be a valid block at the time of shipment.

## RECOMMENDED DC OPERATING CONDITIONS

### TC58DVM82A1xxxx, TC58DVM82F1xxxx

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Power Supply Voltage</td>
<td>2.7</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VCCQ</td>
<td>I/O Port Power Supply Voltage</td>
<td>2.7</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td>-0.3*</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

* -2 V (pulse width lower than 20 ns)

### TC58DAM82A1xxxx, TC58DAM82F1xxxx

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Power Supply Voltage</td>
<td>2.7</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VCCQ</td>
<td>I/O Port Power Supply Voltage</td>
<td>1.65</td>
<td>1.8</td>
<td>1.95</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td>-0.3*</td>
<td>—</td>
<td>VCCQ X 0.22</td>
<td>V</td>
</tr>
</tbody>
</table>

* -2 V (pulse width lower than 20 ns)

## DC CHARACTERISTICS (Ta = 0° to 70°C, VCC = 2.7 V to 3.6 V)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IL</td>
<td>Input Leakage Current</td>
<td>VIN = 0 V to VCCQ</td>
<td>—</td>
<td>—</td>
<td>±10</td>
<td>μA</td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td>VOUT = 0 V to VCCQ</td>
<td>—</td>
<td>—</td>
<td>±10</td>
<td>μA</td>
</tr>
<tr>
<td>ICCO1</td>
<td>Operating Current (Serial Read)</td>
<td>CE = VIL, IOUT = 0 mA, tcycle = 50 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO3</td>
<td>Operating Current (Command Input)</td>
<td>tcycle = 50 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO4</td>
<td>Operating Current (Data Input)</td>
<td>tcycle = 50 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO5</td>
<td>Operating Current (Address Input)</td>
<td>tcycle = 50 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO7</td>
<td>Programming Current</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>ICCO8</td>
<td>Erasing Current</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>ICCS1</td>
<td>Standby Current</td>
<td>CE = VIH, WP = 0 V/VCCQ</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>ICCS2</td>
<td>Standby Current</td>
<td>CE = VCCQ - 0.2 V. WP = 0 V/VCCQ</td>
<td>—</td>
<td>10</td>
<td>50</td>
<td>μA</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>IOH = -0.5 mA</td>
<td>VCCQ -0.5</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>IOL = 2.1 mA</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>IOL (RY/RBY)</td>
<td>Output Current of RY/RBY pin</td>
<td>VOL = 0.4 V</td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>mA</td>
</tr>
</tbody>
</table>
## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS
(Ta = 0° to 70°C, VCC = 2.7 V to 3.6 V)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCLS</td>
<td>CLE Setup Time</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCLH</td>
<td>CLE Hold Time</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCS</td>
<td>CE Setup Time</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCH</td>
<td>CE Hold Time</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWP</td>
<td>Write Pulse Width</td>
<td>25</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tALS</td>
<td>ALE Setup Time</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tALH</td>
<td>ALE Hold Time</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup Time</td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWH</td>
<td>WE High Hold Time</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWW</td>
<td>WP High to WE Low</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRR</td>
<td>Ready to RE Falling Edge</td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRP</td>
<td>Read Pulse Width</td>
<td>35</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tREA</td>
<td>RE Access Time (Serial Data Access)</td>
<td>—</td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCEA</td>
<td>CE Access Time (Serial Data Access, ID Read)</td>
<td>—</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tALEA</td>
<td>ALE Access Time (ID Read)</td>
<td>—</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tREAD</td>
<td>RE Access Time (ID Read)</td>
<td>—</td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tOH</td>
<td>Data Output Hold Time</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tOHZ</td>
<td>RE High to Output High Impedance</td>
<td>—</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCHZ</td>
<td>CE High to Output High Impedance</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tREH</td>
<td>High Hold Time</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tR</td>
<td>Output-High-impedance-to-RE Falling Edge</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRSTO</td>
<td>RE Access Time (Status Read)</td>
<td>—</td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCSTO</td>
<td>CE Access Time (Status Read)</td>
<td>—</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRW</td>
<td>WE High to Low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWHC</td>
<td>WE High to CE Low</td>
<td>30</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWHR</td>
<td>WE High to Low</td>
<td>30</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tL</td>
<td>Memory Cell Array to Starting Address</td>
<td>—</td>
<td>25</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>tWB</td>
<td>WE High to Busy</td>
<td>—</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAR2</td>
<td>ALE Low to RE Low (Read Cycle)</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRB</td>
<td>RE Last Clock Rising Edge to Busy (in Sequential Read)</td>
<td>—</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCRY</td>
<td>CE High to Ready (When interrupted by CE in Read Mode)</td>
<td>—</td>
<td>$1 + t_r (R_Y/B_Y)$</td>
<td>µs</td>
<td>(1)(2)</td>
</tr>
<tr>
<td>tRST</td>
<td>Device Reset Time (Read/Program/Erase)</td>
<td>—</td>
<td>6/10/500</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

### AC TEST CONDITIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TC58DVxxxxx</td>
</tr>
<tr>
<td>Input level</td>
<td>2.4 V, 0.4 V</td>
</tr>
<tr>
<td>Input pulse rise and fall time</td>
<td>3 ns</td>
</tr>
<tr>
<td>Input comparison level</td>
<td>1.5 V, 1.5 V</td>
</tr>
<tr>
<td>Output data comparison level</td>
<td>1.5 V, 1.5 V</td>
</tr>
<tr>
<td>Output load</td>
<td>$C_L (100 \text{ pF}) + 1 \text{ TTL}$</td>
</tr>
</tbody>
</table>
Note: (1) **CE** High to Ready time depends on the pull-up resistor tied to the **RY/RY** pin. (Refer to Application Note (9) toward the end of this document.)

(2) Sequential Read is terminated when \( t_{CEH} \) is greater than or equal to 100 ns. If the **RE** to **CE** delay is less than 30 ns, **RY/RY** signal stays Ready.

### PROGRAMMING AND ERASING CHARACTERISTICS

(\( Ta = 0^\circ \text{ to } 70^\circ \text{C, } V_{CC} = 2.7 \text{ V to } 3.6 \text{ V} \))

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PROG} )</td>
<td>Programming Time</td>
<td>—</td>
<td>200</td>
<td>1000</td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>( N )</td>
<td>Number of Programming Cycles on Same Page</td>
<td>—</td>
<td>—</td>
<td>3</td>
<td></td>
<td>(1)</td>
</tr>
<tr>
<td>( t_{ERASE} )</td>
<td>Block Erasing Time</td>
<td>—</td>
<td>2</td>
<td>10</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

(1): Refer to Application Note (12) toward the end of this document.
TIMING DIAGRAMS

Latch Timing Diagram for Command/Address/Data

Command Input Cycle Timing Diagram

\[
\begin{array}{c}
\text{CLE} \\
\text{CE} \\
\text{WE} \\
\text{ALE} \\
\text{I/O1 to I/O8}
\end{array}
\]

\[
\begin{array}{c}
t_{DS} \\
t_{DH}
\end{array}
\]

\[
\begin{array}{c}
t_{CS} \\
t_{WP} \\
t_{ALS} \\
t_{ALH} \\
t_{DS} \\
t_{DH}
\end{array}
\]

\[
\begin{array}{c}
\text{V}_{IH} \text{ or } \text{V}_{IL}
\end{array}
\]
Address Input Cycle Timing Diagram

Data Input Cycle Timing Diagram

: \( V_{IH} \) or \( V_{IL} \)
Serial Read Cycle Timing Diagram

Status Read Cycle Timing Diagram

* 70H represents the hexadecimal number

: $V_{IH}$ or $V_{IL}$
Read Cycle (1) Timing Diagram

Read Cycle (1) Timing Diagram: When Interrupted by \text{CE}

* Read Operation using 00H Command  \( N: 0 \) to 255

\( \square \) : \( \text{VIH or VIL} \)
Read Cycle (2) Timing Diagram

Read Cycle (3) Timing Diagram

* Read Operation using 01H Command  N: 0 to 255

* Read Operation using 50H Command  N: 0 to 15

: VIH or VIL
Sequential Read (1) Timing Diagram

CLE

CE

WE

ALE

RE

RY/BY

Column address
Page address
N
M

Page M access
Page M + 1 access

00H

A0 to A7

A9 to A16

A17 to A24

N

N + 1

N + 2

527

0

1

2

527

: $V_{IH}$ or $V_{IL}$

Sequential Read (2) Timing Diagram

CLE

CE

WE

ALE

RE

RY/BY

Column address
Page address
N
M

Page M access
Page M + 1 access

01H

A0 to A7

A9 to A16

A17 to A24

N

256 + N

256 + N + 1

527

0

1

2

527

: $V_{IH}$ or $V_{IL}$
Sequential Read (3) Timing Diagram

- CLE
- CE
- WE
- ALE
- RE
- Column address: N
- Page address: M
- Page M access
- Page M + 1 access

- I/O1 to I/O8
- RY/BY

: $V_{IH}$ or $V_{IL}$
Auto-Program Operation Timing Diagram

- CLE
- CE
- WE
- ALE
- RE
- I/O1 to I/O8
- RY/BY

Auto Block Erase Timing Diagram

- CLE
- CE
- WE
- ALE
- RE
- I/O1 to I/O8
- RY/BY

: $V_H$ or $V_L$
: Do not input data while data is being output.
PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pinouts are configured as shown in Figure 1.

**Command Latch Enable: CLE**

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WE signal while CLE is High.

**Address Latch Enable: ALE**

The ALE signal is used to control loading of either address information or input data into the internal address/data register.

Address information is latched on the rising edge of WE if ALE is High.

Input data is latched if ALE is Low.

**Chip Enable: CE**

The device goes into a low-power Standby mode when CE goes High during a Read operation. The CE signal is ignored when device is in Busy state (RY/RY = L), such as during a Program or Erase operation, and will not enter Standby mode even if the CE input goes High. The CE signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register.

**Write Enable: WE**

The WE signal is used to control the acquisition of data from the I/O port.

**Read Enable: RE**

The RE signal controls serial data output. Data is available after the falling edge of RE.

The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

**I/O Port: I/O1 to 8**

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

**I/O Port: I/O9 to 16**

The I/O9 to 16 pins are used as a port for input/output data to and from the device. The I/O9 to 16 pins are low level (VIL) when address and command are asserted.

**Write Protect: WP**

The WP signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when WP is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

**Ready/Busy: RY/RY**

The RY/RY output signal is used to indicate the operating condition of the device. The RY/RY signal is in Busy state (RY/RY = L) during the Program, Erase and Read operations and will return to Ready state (RY/RY = H) after completion of the operation. The output buffer for this signal is an open drain.
Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes
1 block = 528 bytes × 32 pages = (16K + 512) bytes
Capacity = 528 bytes × 32 pages × 2048 blocks

A page consists of 264 words in which 256 words are used for main memory storage and 8 words are for redundancy or for other uses.

1 page = 264 words
1 block = 264 words × 32 pages = (8K + 256) words
Capacity = 264 words × 32 pages × 2048 blocks

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

<table>
<thead>
<tr>
<th>I/O8</th>
<th>I/O5</th>
<th>I/O6</th>
<th>I/O4</th>
<th>I/O3</th>
<th>I/O2</th>
<th>I/O1</th>
</tr>
</thead>
<tbody>
<tr>
<td>A7</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
</tr>
<tr>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
<td>A11</td>
<td>A10</td>
</tr>
<tr>
<td>A24</td>
<td>A23</td>
<td>A22</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
</tr>
</tbody>
</table>

A0~A7: Column address
A9~A13: NAND address in block
A14~A24: Block address
A8 is automatically set to Low or High by a 00H command or a 01H command.

I/O9-16 should be low when address is input.
Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the ten different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, CE, WE, RE and WP signals, as shown in Table 2.

Table 2. Logic table

<table>
<thead>
<tr>
<th></th>
<th>CLE</th>
<th>ALE</th>
<th>CE</th>
<th>WE</th>
<th>RE</th>
<th>WP*1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command Input</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address Input</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Input</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial Data Output</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>During Read (Busy)</td>
<td>*</td>
<td>*</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td></td>
<td>*</td>
<td>*</td>
<td>H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>During Programming (Busy)</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>H</td>
</tr>
<tr>
<td>During Erasing (Busy)</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>H</td>
</tr>
<tr>
<td>Program, Erase Inhibit</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>L</td>
</tr>
<tr>
<td>Standby</td>
<td>*</td>
<td>*</td>
<td>H</td>
<td>*</td>
<td>*</td>
<td>0 V/Vcc</td>
</tr>
</tbody>
</table>

H: VIH, L: VIL, *: VIH or VIL

*1: Refer to Application Note (10) toward the end of this document regarding the WP signal when Program or Erase Inhibit

Table 3. Command table (HEX)

<table>
<thead>
<tr>
<th></th>
<th>First Cycle</th>
<th>Second Cycle</th>
<th>Acceptable while Busy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial Data Input</td>
<td>80</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Read Mode (1)</td>
<td>00</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Read Mode (2)</td>
<td>01</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Read Mode (3)</td>
<td>50</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Reset</td>
<td>FF</td>
<td>—</td>
<td>O</td>
</tr>
<tr>
<td>Auto Program</td>
<td>10</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Auto Block Erase</td>
<td>60</td>
<td>D0</td>
<td></td>
</tr>
<tr>
<td>Status Read</td>
<td>70</td>
<td>—</td>
<td>O</td>
</tr>
<tr>
<td>ID Read</td>
<td>90</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

01 command isn't implemented by x16.

Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

<table>
<thead>
<tr>
<th></th>
<th>CLE</th>
<th>ALE</th>
<th>CE</th>
<th>WE</th>
<th>RE</th>
<th>I/O1~I/O16</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Select</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Data output</td>
<td>Active</td>
</tr>
<tr>
<td>Output Deselect</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>High impedance</td>
<td>Active</td>
</tr>
</tbody>
</table>

H: VIH, L: VIL, *: VIH or VIL

2003_01_29  18/34
DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00H command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.

A data transfer operation from the cell array to the register starts on the rising edge of WE in the third cycle (after the address information has been latched). The device will be in Busy state during this transfer period. The CE signal must stay Low after the third address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the RE clock from the start pointer designated in the address input cycle.

Read Mode (2)  x8 only

The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).
Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

Address bits A0-A3 are used to set the start pointer for the redundant memory cells, while A4-A7 are ignored. Once a 50H command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4-to-A7 address. (An 00H command is necessary to move the pointer back to the 0-to-511 main memory cell location.)

Sequential Read(1)(2)(3)
This mode allows the sequential reading of pages without additional address input.

Sequential Read modes (1) and (2) output the contents of addresses 0~m as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address ** on each RE clock signal.

X8:  m=527, n=512
X16: m=263, n=256
The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the RE clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

<table>
<thead>
<tr>
<th>STATUS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O1 Pass/Fail</td>
<td>Pass: 0 Fail: 1</td>
</tr>
<tr>
<td>I/O2 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O3 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O4 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O5 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O6 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O7 Ready/Busy</td>
<td>Ready: 1 Busy: 0</td>
</tr>
<tr>
<td>I/O8 Write Protect</td>
<td>Protect: 0 Not Protected: 1</td>
</tr>
<tr>
<td>I/O9 to I/O16 Not Used</td>
<td>0</td>
</tr>
</tbody>
</table>

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

System Design Note: If the BY/RY pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.
Auto Page Program

The device carries out an Automatic Page Program operation when it receives a “10H” Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of WE after the Erase Start command “D0H” which follows the Erase Setup command “60H”. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.
The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an “FFH” Reset command input during the various device operations is as follows:

**When a Reset (FFH) command is input during programming**

![Diagram 8](image8)

**When a Reset (FFH) command is input during erasing**

![Diagram 9](image9)

**When a Reset (FFH) command is input during Read operation**

![Diagram 10](image10)

**When a Status Read command (70H) is input after a Reset**

![Diagram 11](image11)

**When two or more Reset commands are input in succession**

![Diagram 12](image12)

The second FF command is invalid, but the third FF command is valid.
The device contains ID codes which identify the device type and the manufacturer.
The ID codes can be read out under the following timing conditions:

**Table 6. ID Codes read out by ID read command 90H**

<table>
<thead>
<tr>
<th></th>
<th>I/O8</th>
<th>I/O7</th>
<th>I/O6</th>
<th>I/O5</th>
<th>I/O4</th>
<th>I/O3</th>
<th>I/O2</th>
<th>I/O1</th>
<th>Hex Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maker code</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>98H</td>
</tr>
<tr>
<td>Device code</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>75H</td>
</tr>
</tbody>
</table>

I/O9 to I/O16 are “0”.

For the specifications of the access times tREAI, tCEA and tALEA refer to the AC Characteristics.

Figure 13. ID Read timing
APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The WP signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The WP signal may be negated any time after the VCC reaches 2.5 V and CE signal is kept high in power up sequence.

![Power-on/off Sequence Diagram]

In order to operate this device stably, after VCC becomes 2.5 V and VCCQ becomes 1.5V, it recommends starting access after about 200 μs.

(2) Status after power-on:

The following sequence is necessary because some input signals may not be stable at power-on.

![Power-on/off Sequence Diagram]

(3) Prohibition of unspecified commands:

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of command while Busy state:

During Busy state, do not input any command except 70H and FFH.

(5) Acceptable commands after Serial Input command “80H”:

Once the Serial Input command “80H” has been input, do not input any command other than the Program Execution command “10H” or the Reset command “FFH”.

If a command other than “10H” or “FFH” is input, the Program operation is not performed.

![Command Diagram]
(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

![Diagram of page programming within a block](image)

Figure 17. Page programming within a block

(7) Status Read during a Read operation

![Diagram of command timing](image)

Figure 18.

The device status can be read out by inputting the Status Read command “70H” in Read mode. Once the device has been set to Status Read mode by a “70H” command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited. However, when the Read command “00H” is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.
(8) Pointer control for "00H", "01H" and "50H"

The device has three Read modes which set the destination of the pointer. Table 8 shows the destination of the pointer, and Figure 19 is a block diagram of their operations.

Table 8. Pointer Destination

<table>
<thead>
<tr>
<th>Read Mode</th>
<th>Command</th>
<th>Pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(x8)</td>
<td>(x16)</td>
</tr>
<tr>
<td>(1)</td>
<td>00H</td>
<td>0~255</td>
</tr>
<tr>
<td>(2)</td>
<td>01H</td>
<td>256~511</td>
</tr>
<tr>
<td>(3)</td>
<td>50H</td>
<td>512~527</td>
</tr>
</tbody>
</table>

The pointer is set to region A by the “00H” command, to region B by the “01H” command, and to region C by the “50H” command.

(Example)

The “00H” command must be input to set the pointer back to region A when the pointer is pointing to region C.

To program region C only, set the start point to region C using the 50H command.

Figure 20. Example of How to Set the Pointer
(9) **RY/BY**: termination for the Ready/Busy pin (RY/BY)

A pull-up resistor needs to be used for termination because the RY/BY buffer consists of an open drain circuit.

This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.
(10) Note regarding the \text{WP} signal

The Erase and Program operations are automatically reset when \text{WP} goes Low. The operations are enabled and disabled as follows:

\textbf{Enable Programming}

\begin{center}
\begin{tabular}{c c c c c}
\hline
\text{WE} & & & & \\
\hline
\text{DIN} & 80 & 10 & & \\
\hline
\text{WP} & & & & \\
\hline
\text{RY/RY} & & & & \\
\hline
\text{t}_{WW} \ (100 \ \text{ns min}) & & & & \\
\hline
\end{tabular}
\end{center}

\textbf{Disable Programming}

\begin{center}
\begin{tabular}{c c c c c}
\hline
\text{WE} & & & & \\
\hline
\text{DIN} & 80 & 10 & & \\
\hline
\text{WP} & & & & \\
\hline
\text{RY/RY} & & & & \\
\hline
\text{t}_{WW} \ (100 \ \text{ns min}) & & & & \\
\hline
\end{tabular}
\end{center}

\textbf{Enable Erasing}

\begin{center}
\begin{tabular}{c c c c c}
\hline
\text{WE} & & & & \\
\hline
\text{DIN} & 60 & D0 & & \\
\hline
\text{WP} & & & & \\
\hline
\text{RY/RY} & & & & \\
\hline
\text{t}_{WW} \ (100 \ \text{ns min}) & & & & \\
\hline
\end{tabular}
\end{center}

\textbf{Disable Erasing}

\begin{center}
\begin{tabular}{c c c c c}
\hline
\text{WE} & & & & \\
\hline
\text{DIN} & 60 & D0 & & \\
\hline
\text{WP} & & & & \\
\hline
\text{RY/RY} & & & & \\
\hline
\text{t}_{WW} \ (100 \ \text{ns min}) & & & & \\
\hline
\end{tabular}
\end{center}
(11) When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

Read operation

![Diagram of Read operation](image)

Program operation

![Diagram of Program operation](image)
(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 3 segments. Each segment can be programmed individually as follows:

<table>
<thead>
<tr>
<th>1st programming</th>
<th>Data Pattern 1</th>
<th>All 1s</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd programming</td>
<td>All 1s</td>
<td>Data Pattern 2</td>
</tr>
<tr>
<td>3rd programming</td>
<td>All 1s</td>
<td>Data Pattern 3</td>
</tr>
</tbody>
</table>

Result:

| Data Pattern 1 | Data Pattern 2 | Data Pattern 3 |

Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be “1”
(13) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.

At the time of shipment, all data bytes in a Valid Block are FFh(x8) or FFFFh(x16). For Bad Block, all bytes are not in the FFh state(x8) or FFFFh state(x16). Please don’t perform erase operation to Bad Block.

Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate.

The number of valid blocks at the time of shipment is as follows:

<table>
<thead>
<tr>
<th>Valid (Good) Block Number</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2008</td>
<td></td>
<td>2048</td>
<td>Block</td>
</tr>
</tbody>
</table>

Bad Block Test Flow

Start

Block No = 1

Read Check

Yes

Block No = 2048

End

No

Block No = Block No + 1

Pass

Bad Block *1

Fail

*1: No erase operation is allowed to detected bad blocks

Figure 27
(14) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.

<table>
<thead>
<tr>
<th>FAILURE MODE</th>
<th>DETECTION AND COUNTERMEASURE SEQUENCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block</td>
<td>Erase Failure</td>
</tr>
<tr>
<td></td>
<td>Status Read after Erase → Block Replacement</td>
</tr>
<tr>
<td>Page</td>
<td>Programming Failure</td>
</tr>
<tr>
<td></td>
<td>Status Read after Program → Block Replacement</td>
</tr>
<tr>
<td>Single Bit</td>
<td>Programming Failure</td>
</tr>
<tr>
<td></td>
<td>1 → 0</td>
</tr>
<tr>
<td></td>
<td>(1) Block Verify after Program → Retry</td>
</tr>
<tr>
<td></td>
<td>(2) ECC</td>
</tr>
</tbody>
</table>

- ECC: Error Correction Code
- Block Replacement

**Program**

When an error occurs in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

**Erase**

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.
Weight: 0.53g (typ.)